Design and optimisation of a universal battery management system in a photovoltaic application

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DECLARATION

I, Emmanuel Oluwafemi Ogunniyi, hereby declare that the following research information is my own work. This is submitted in fulfilment of the requirements for the Magister Technologiae: Engineering: Electrical to the Department of Electronic Engineering at the Vaal University of Technology, Vanderbijlpark. This dissertation has never been submitted for evaluation to any educational institution neither has the work therein been previously accepted in substance for any degree.

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DEDICATION

This dissertation is dedicated to God for providing me with the wherewithal to carry out this research. He is also the giver of wisdom, knowledge and understanding.

ABSTRACT

Due to the fickle nature of weather upon which renewable energy sources mostly depend, a shift towards a sustainable renewable energy system should be accompanied with a good intermediate energy storage system, such as a battery bank, set up to store the excess supply from renewable sources during their peak periods. The stored energy can later be utilised to supply a regulated and steady power supply for use during the off-peak periods of these renewable energy sources.

Battery banks, however, are often faced with the challenge of charge imbalance due to the disparities that occur in the operating characteristics of the batteries that constitute a bank. When a battery bank with charge imbalance is repeatedly used in applications without an effective battery management system (BMS) through active charge equalisation, there could be an early degradation, loss of efficiency and reduction of service life of the entire batteries in the bank.

In this research, a universal battery management system (BMS) in stand-alone photovoltaic application was proposed and designed. The BMS consists majorly of a switched capacitor (SC) active charge equaliser, designed with a unique configuration of high capacitance and relatively low switching frequency, which can be applicable to common battery types used in stand-alone photovoltaic application. The circuit was mathematically optimised to minimise losses attributed to impulsive charging and tested with lead acid, silver calcium, lead calcium and lithium ion batteries being commonly used in stand-alone photovoltaic application. The SC design was verified by comparing its simulation results to the digital oscilloscope results, and with both results showing similar values and graphs, the design configuration was validated.

The design introduced a simple control strategy and less complicated circuit configuration process, which can allow an easy setup for local usage. The benefit of its multiple usage with different stand-alone photovoltaic battery types saves the cost of purchasing a different charger and balancer for different battery types. More so, the design is solar energy dependent. This could provide an additional benefit for usage in areas where energy dependence is off-grid.

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GLOSSARY OF ABBREVIATIONS AND SYMBOLS

A
AC – Alternating Current
AGM – Absorbent Glass Mat
Ah – Ampere hour

B
BJT – Bipolar Junction Transistor
BMS – Battery Management System

C
C – Capacitor

D
DC - Direct Current
DOD - Depth of Discharge
3D – 3- dimentional

E
ESR – Equivalent Series Resistance
et al. – et alia (Latin), "and others" (English)
EVs - Electric Vehicles

F
F - Farad

G
GND – Ground

H
h – Hour

I
IC - Integrated Circuit

K
kV – Kilovolt

L
LED - Light Emitting Diode
LF – Low Frequency

M
MPPT- Maximum Power Point Tracking

MOSFET – Metal Oxide Silicon Field Effect Transistor
μ – Micro, 10^{-6}

N
η – Efficiency

O
OCV – Open Circuit Voltage
Ω – Ohm

P
PCB – Printed Circuit Board
PV – Photovoltaic
PWM – Pulse Width Modulation

R
R_{DS} – Drain-to-source resistance
R-C – Resistor-Capacitor

S
SC – Switched Capacitor
SLI – Starting Lighting and Ignition
SOC – State of Charge
SOH – State of Health

T
τ – Time constant

U
UPS – Uninterruptible Power Supply

V
V – Volt
V_{GS} – Gate-to-source Voltage
VRLA – Valve-Regulated Lead Acid

W
W – Watt

CHAPTER 1: INTRODUCTION

1.1 BACKGROUND

Batteries are electrochemical devices consisting of more than one electrically connected cell for storing electrical energy in chemical form and converting the stored chemical energy back to electricity when needed (Dell & Rand, 2001:10-14, Winter & Brodd, 2004:4245-4270).

In 1800, the first electric battery, the voltaic pile, was introduced by Alessandro Volta (Decker, 2005, Buchmann, 2013). This battery and others that followed, however, could not retain charges for a long period and could not be recharged after their inherent charges had been depleted. These challenges led to the introduction of rechargeable batteries, first invented in a lead-acid electrode-electrolyte combination by a French physicist, Gaston Planté, in 1859 (Buchmann, 2013, electrical4u, 2015). Meanwhile, in order to meet more specific demands of modern day applications, there have been more improvements to battery technology as the primitive lead-acid batteries are now being replaced with more efficient rechargeable batteries in different categories, such as silver-, nickel- and lithium batteries (Crompton, 2000, Gasper & Silver, 2015:924). Some common types in these categories include nickel-cadmium, nickel-zinc, silver-cadmium, silver-zinc, lithium-ion, etcetera, while some more are still in the experimental stage (Divya & Østergaard, 2009:511-520, Yuasa, 2010).

Due to the differences in their chemical constituents, the electrochemical characteristics of these batteries differ and so also their respective applications as shown in Table 1. Some of the earliest commercial applications of rechargeable batteries (the lead acid batteries) were found in frequency control, voltage regulation, etcetera (Rajasekharachari *et al.*, 2013), while today, portable workstations (laptop computer, barcode scanner, portable data assistant/ PDA scanner), cell phones, video camera, uninterrupted power supply (UPS) systems, cars, electric vehicles (EVs), etcetera depend mostly on batteries of various types, sizes and chemistries for their respective applications and functionalities. Meanwhile, the importance of rechargeable batteries in stand-alone photovoltaic (PV) applications cannot be overemphasised. Recently, especially in South Africa, focus is being shifted towards a more compact, efficient and sustainable renewable form

of alternative energy especially through photovoltaic cells (solar energy) and wind (Krupa & Burch, 2011:6254-6261).

Table 1: Electrochemical characteristics of some common batteries

	LEAD ACID BATTERIES		NICKEL (ALKALINE) BATTERIES		SILVER BATTERIES		LITHIUM BATTERIES
	Flooded (wet)	Sealed (*VRLA)	Nickel cadmium	Nickel-zinc	Silver-zinc	Silver-cadmium	Lithium-ion
Cathode	Lead dioxide	Lead dioxide	Nickel hydroxide	Nickel oxy-hydroxide	Silver oxide	Silver oxide	Lithium cobalt oxide ($LiCoO_2$)
Anode	Lead-Antimony	Lead-Calcium	Cadmium	Zinc	Zinc	Cadmium	Lithium Carbonate (LiC_6)
Electrolyte	Sulphuric acid	Sulphuric acid	Potassium hydroxide	Potassium hydroxide	Potassium hydroxide	Potassium hydroxide	Ethylene + propylene carbonate
***OCV/ Cell (V)**	2.10	2.12	1.35	1.71	1.86	1.4	4.1
Energy density (Wh/Kg)	15-26	22-23	26-37	33-37	55-220	24-120	125
References	(Anglin & Sadoway, 2014, Crompton, 2000)		(Crompton, 2000, Energizer, 2001)	(Crompton, 2000, Electropaedia, 2005)	(Anglin & Sadoway, 2014, Electropaedia, 2005)	(Crompton, 2000, Morehouse *et al.*, 1958:1462-1483)	(Nagaura & Tozawa, 1990:209, Ozawa, 1994:212-221, Mikolajczak *et al.*, 2012)

Solar and wind energy can be as unpredictable as the weather they depend upon; hence, a shift to these renewable forms of energy as a way of escape from fossil fuel and the grid system must be accompanied by a good intermediate energy storage system such as a battery bank setup to store their excess energy and provide a regulated and steady power supply for use when the sun has set and the winds have become still (Nathan, 2012).

A battery bank as a unit consists of more than one cell or battery connected together in a series-parallel configuration in order to generate a higher DC voltage and capacity for applications where maximum energy storage and/or supply are needed, ranging from household inverters to megawatt systems connected to stabilise an electrical distribution network (Daly, 1995:233-237, Taylor, 1996:249-252, Divya & Østergaard, 2009:511-520, Rajasekharachari *et al.*, 2013). This is necessary because the DC voltage requirements of most battery applications are higher than can be derived from a single electrochemical cell.

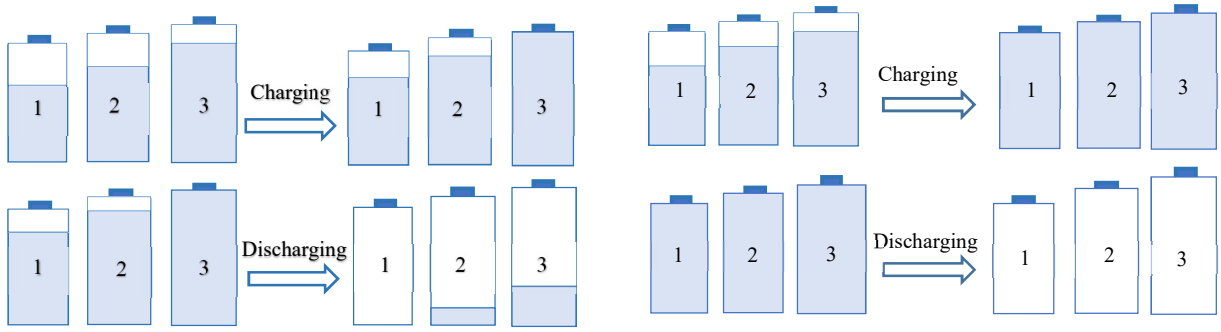
Whenever battery banks are discharged or recharged together as a unit, they are often faced with the challenge of charge imbalance among the individual batteries that constitute the bank. This charge imbalance happens due to the disparities that occur in the operating characteristics of batteries that constitute a bank. This is caused by either or both of two major categories, namely internal source and external source (Park *et al.*, 2009:3216-3223, Gallardo-Lozano *et al.*, 2014:934-949). The internal sources are the differences in the electrochemical characteristics of the batteries, which consist of manufacturing variance in physical volume, variation in internal impedance, different states of health (SOH) and different self-discharge rates; while the external sources are the differences in thermal variation across the battery pack, which results in different self-discharge rates of the batteries. Some protection ICs also affect battery packs externally by draining charges unequally from the different series ranks in the pack (Kim *et al.*, 2012:411-424, Han *et al.*, 2014:158-163, Cao *et al.*, 2008:1-6).

Battery charge imbalance is the most prominent challenge facing battery banks. It creates a gap difference between the residual capacities of batteries before charging and the restored capacities during charging, even though the same current is flowing through each battery (Moo *et al.*, 2003:704-710, Hsieh *et al.*, 2008:1083-1087). During charging, weak batteries, such as those with initial lower charge tend to be unsaturated at full charge termination, while others with an initial higher charge tend to be excessively overcharged when the charging process is terminated.

Conversely, during discharge, the weak batteries tend to have lower voltage than the other batteries in the bank; thereby, becoming excessively drained (see Figure 1a) and resulting in reduced capacity of the bank. These extreme conditions of charging and discharging have been attributed to major causes of battery failure such as sulfation, acid stratification, positive grid corrosion, gassing, explosion, etcetera (Catherino *et al.*, 2004:113-120, Duffy & Wright, 2016:374-375). Meanwhile, when the battery bank is charged and discharged repeatedly under these conditions without proper charge equalisation, this imbalance becomes magnified and extends to other batteries in the bank, reducing the battery life and bringing all the batteries to early degradation and loss of efficiency.

In order to maximise the capacity of these batteries and to prevent overcharging and undercharging, a battery management system (BMS) is required to actively ensure that battery

banks are kept at the same voltage or state of charge (SOC) through charge equalisation as indicated in Figure 1b.



a. Battery series pack without charge equalization

b. Battery series pack with active charge equalization

Keys: 1= low charge. 2= medium charge. 3= high charge or full

Figure 1: Charge and discharge of series battery packs (Zhong *et al.*, 2014:558-564)

A BMS is any electronic system that manages and protects a battery bank from operating outside of its safe operating area by monitoring its SOC/ SOH and providing charge equalisation on the batteries that constitute the bank (Barsukov & Qian, 2013).

Various charge equalisation techniques for proper BMS have been proposed by several authors (West & Krein, 2000:439-446, Moo *et al.*, 2003:704-710, Krein & Balog, 2002:516-523, Hung *et al.*, 1993:96-104) and these can be grouped into three: battery selection, passive methods, and active methods (Gallardo-Lozano *et al.*, 2014:934-949). Battery selection involves grouping of batteries with similar electrochemical properties for charging, but it is not efficient because the self-discharge of the batteries in the string can vary differently along their lifetime (Uno & Tanaka, 2012:4704-4712) and variations in an individual cell impedance, capacity and self-discharge rate can still lead to a divergence in its voltage over time.

On the other hand, the passive method balances through forced overcharge and/or dissipation of excess energy through a bypass resistor across each battery (Cadar *et al.*, 2010:1221-6542, Gallardo-Lozano *et al.*, 2014:934-949); this method, however, wastes much energy in the form of heat and thus reduces the system efficiency (Baronti *et al.*, 2014:1811-1816).

The active method balances using external circuits, which actively transport energy among the cells or batteries that constitute a string. This method is preferred to other methods by many

researchers due to its higher efficiency and its applicability to chemistries of different battery types (Fukui & Koizumi, 2013:6715-6720, Cadar *et al.*, 2010:1221-6542, Gallardo-Lozano *et al.*, 2014:934-949). The active method comes in different topologies such as cell bypass, cell to cell, pack to cell and cell(s) to pack to cell(s) (Gallardo-Lozano *et al.*, 2014:934-949).

1.2 PROBLEM STATEMENT

When a battery string is charged or discharged as a single unit, a slight mismatch in the dynamic characteristics of the batteries constituting the string can cause charge imbalance amongst them. When batteries are repeatedly exposed to charge imbalance, the imbalance becomes magnified and extends to other batteries in the bank, thus bringing all the batteries to early degradation, loss of efficiency and reduction of service life.

1.3 RESEARCH OBJECTIVES

The objective of this research is to design an active charge equaliser circuit which can be optimised and integrated into a universal BMS for common battery types used in stand-alone photovoltaic application.

1.4 RESEARCH METHODOLOGY

The systematic methods and analysis undertaken in order to execute the design and implementation of a battery charge equaliser for a universal BMS in a photovoltaic application is carried out in the following approach:

1.4.1 Literature study

A review of different categories of rechargeable batteries, charging characteristics and charge equalisation techniques will be done in order to determine the appropriate battery types for use in a photovoltaic application and to adopt a suitable equalisation technique for the battery banks to be considered.

1.4.2 Experimental design

After a review of different battery charge equalisation techniques already in existence, a battery charge equaliser will be designed, based on the best configuration, which can enable charge

equalisation on the selected battery types. The designed equaliser is expected to be applied to and tested with battery strings of different types for charge equalisation, mostly during their float charging state - that is after the charging process is completed. This is because batteries in a string mostly display a charge imbalance at their float charging stage due to the differences in their SOH levels. For effectiveness, the designed charge equaliser is expected to be applicable to battery pairs of similar voltage rating and type per time. The application of the designed charge equaliser with different battery types and strings used in photovoltaic application would thus enable an integration into a universal BMS.

1.4.3 Experimental set up and procedure

The arrangement of this design will include an array of solar PV panels set up to convert the irradiance energy from the sun to a direct current (DC) voltage for charging battery banks. Then a maximum power point tracker (MPPT) solar charge controller is utilised to supply a regulated DC voltage from the PV panels to the selected battery bank. After this, a designed battery charge equaliser would be connected across each battery bank that will be adopted for this research. A voltage data logger will be configured and implemented for recording the voltage variations of the battery bank during charging, discharging and the equalisation processes. These will be monitored through a computer interface in real time for further analysis. The current flow through the shuttling capacitor during these processes will also be considered and determined analytically and in simulations as this will help in verification and validation of the parameters of the proposed circuit design.

1.4.4 Experimental data analysis

A regression analysis will be undertaken to evaluate the empirical data obtained from the data logger, such as the SOC, voltages and balancing time. The equalisation process will also be tested with different rechargeable battery types. The data obtained from each battery string/bank will be monitored and recorded in two stages for analysis, namely first, the battery string without the equaliser and then the battery string after the charge equaliser is applied.

It is expected that the voltage of each battery pair converges after a certain period of time during the equalisation process. In order to estimate the efficiency of the designed system, some of the

parameters such as the operational charging and equalisation time, energy supply and usage and battery SOC will be considered.

1.5 DELIMITATIONS

Modelling of a new battery will not be included in this research work. Also, the proposed BMS design will be applicable to strings of 12 V rated rechargeable batteries on float charging state.

1.6 SIGNIFICANCE OF THE RESEARCH

The proposed design in this research will have the benefit of multiple usage with pairs of different battery types used in a stand-alone photovoltaic application, thus saving the costs of purchasing different chargers and balancers for different battery types. In addition, this research work is expected to improve the reliability and efficiency of the battery banks, while reducing the degradation of battery life through charge equalisation and operation of all the batteries within their voltage limits. Lastly, the DC supply to the designed BMS will be supplied from solar energy through PV panels. This makes the system applicable in (rural) areas where there is little or no dependence on electricity supply through the grid system.

1.7 OVERVIEW OF REPORT

This dissertation consists of five chapters, which relate to the design and optimisation of the BMS in (stand-alone) photovoltaic applications.

Chapter 1- This chapter consists of the introduction, the background study of batteries, BMS, photovoltaic applications, battery charge imbalance and charge equalisation techniques. This chapter also outlines the methodology of this research, while the delimitations and significance were considered.

Chapter 2- The chapter gives the review of the theoretical background and the literature that relates to the design and optimisation of a universal BMS in a photovoltaic application. In the review, basic information on batteries, BMSs, photovoltaic applications and methods of charge equalisation with special focus on the switched capacitor (SC) technique are considered while the components that make up the charge equaliser circuit design for this research are also discussed with their topologies.

Chapter 3- The chapter focuses on the practical design of the universal BMS in a (stand-alone) photovoltaic application using the selected charge equalisation technique. The design is presented and explained in a systematic approach in the order of charge flow from the solar panel to the charge controller, then to the designed charge equalisation system. The implementation of data logging software and hardware on a computer interface for the integration of the charge equaliser into a BMS is given. Lastly, the software simulation of the equaliser circuit and its printed circuit board layout are presented.

Chapter 4- The chapter gives the details of the results obtained from the experimental analyses of the designed battery charge equaliser circuit when applied to different battery pairs in a string having various charge difference ranges. The method of analyses of the charge equaliser includes the testing and comparison of the charge equaliser circuit with different rechargeable battery types of the same nominal charge rating and evaluation of the effect of the design on the reduction in charge imbalance ratio among the battery pairs both before and after the equalisation has been completed.

Chapter 5- In this chapter, the conclusions and recommendation drawn from the design and implementation of the designed equalisation circuit as well as the complete BMS are presented.

1.8 SUMMARY

This chapter presents the introduction to the research, which includes the background study of batteries, BMSs and battery charge imbalance and charge equalisation techniques. The factors that necessitated this research was presented in the form of a problem statement, while the methodology, significance and delimitation of the work are included. The chapter also gives a brief overview of the dissertation.

In the next chapter, the literature review and the theoretical study of batteries, BMSs, photovoltaic applications and battery charge imbalance and charge equalisation techniques are discussed. The review also incorporated the overview of the electronic components and devices, which are used for the design of the battery charge equaliser as implemented in this work.

CHAPTER 2: THEORETICAL CONSIDERATIONS

In the previous chapter, the background, purpose of study, problem statement and objectives of the research were covered. The methodology showing the systematic method of approach to the research study and the delimitations were also given alongside the overall significance of the research.

This chapter gives the review of the theoretical background and the literature that relates to the design and optimisation of a universal BMS in a photovoltaic application. The review gave the basic information on batteries, BMS, photovoltaic applications and methods of charge equalisation with special focus on the SC technique. Lastly, the components that make up the charge equaliser circuit design for this research were also discussed with their topologies.

2.1 INTRODUCTION

The need for renewable energy storage is important due to the continual climate change and the fickle nature of the weather upon which renewable energy sources depend. The photovoltaic system is one of the most commonly used renewable energy systems, which converts solar energy directly into electricity using the photovoltaic panels. The generation of electricity using this system does not require any moving part and poses no harmful threat to the environment, thus making it one of the most commonly utilised renewable energy systems.

Photovoltaic systems are used in a variety of different applications and these can be categorised into utility interactive systems and stand-alone systems (Center, 2002:1-4, Pearsall & Hill, 2001:1-42). The utility interactive, otherwise known as grid-connected system enables the backup of excess photovoltaic (PV) energy generated during the day on the utility grid through a feedback-into-the-grid process, while a standalone system is an isolated system, which generates electricity from a PV system and directly uses the electricity to power different applications without feeding back the excess into the utility grid system (Center, 2002:1-4, Pearsall & Hill, 2001:1-42). The excess energy generated in stand-alone systems by the PV systems can be stored in an intermediate energy storage device, usually a battery bank set up between the PV system and the end-application.

In comparison with other energy storage system technology in the recent times such as the pumped hydroelectric storage (PHS), compressed air energy storage (CAES), flywheels, and hydrogen energy storage, the conventional rechargeable battery energy storage systems (BESS) offer a more simple and efficient way of electricity storage, which can be integrated into renewable energy applications (Ogunniyi & Pienaar, 2017:233-239).

Although there are different categories of battery technologies that can be integrated into renewable energy sources such as the photovoltaic system, as further reviewed in this chapter, battery charge imbalance is one of the main challenges of BESS, which usually occurs when batteries are connected in series strings or series-parallel banks. This charge imbalance, when not controlled through an effective BMS, can result in quick degradation and damage the entire battery bank.

2.2 MAJOR CLASSES OF BATTERIES

Batteries can generally be classified into two groups: non-rechargeable batteries and rechargeable batteries. The non-rechargeable batteries, otherwise known as the primary batteries, cannot be recharged after their inherent charges are depleted, thus they are discarded when they can no longer supply enough electrical energy. Some examples of primary batteries include carbon zinc (Leclanché), alkaline manganese, mercury-zinc, silver-zinc, zinc/air, etcetera (Morehouse *et al.*, 1958:1462-1483, Crompton, 2000:2/3-2/9, Beaty & Fink, 2013, Anglin & Sadoway, 2014, Thomas, 2011). Rechargeable batteries, also known as the storage batteries can be re-energised after their inherent charges are depleted, through a reversible electrochemical process. Thus, by passing the current in the reverse direction to the battery during discharge, the lost chemical energy can be restored to the original state. Today the design of rechargeable batteries is in different chemical compositions, varieties of sizes, energy densities and capacity ratings to provide more advantages such as extended shelf life, load current adjustment with minimum current variations and operation under extreme temperature conditions to different modern applications.

2.3 CATEGORIES OF BATTERIES

There are four major categories of rechargeable batteries, which are being used in the recent times namely lead acid batteries, alkaline (nickel) batteries, silver batteries and lithium batteries.

2.3.1 Lead acid batteries

The lead-acid battery, discovered by Planté in 1860 (Buchmann, 2013) is still one of the most widely used rechargeable batteries. Lead acid batteries (LABs) consist of a lead (Pb) anode and a lead dioxide (PbO_2) cathode, dipped in a dilute sulfuric acid (H_2SO_4) electrolyte, separated by an inert porous material and are manufactured both in "flooded" type and "sealed" type (Scherz & Monk, 2013, PC-Control, 2008). The two common types of sealed lead acid (SLA) batteries are the absorbent glass mat (AGM)-valve regulated lead acid (VRLA) and the gel-VRLA batteries. Other types include silver calcium and lead crystal batteries, which can be classified as the hybrids of SLA batteries. Today, beside the photovoltaic applications, lead acid batteries are also widely used in automotive applications, emergency power supply systems, uninterruptible power supplies (UPS) systems and traction for industrial truck. The automotive applications use starting-lighting and ignition (SLI) batteries while other applications such as the photovoltaic, emergency power supply and uninterruptible power supply system utilise deep-cycled and stationary batteries (Orsino & Dunn, 1961, Morehouse *et al.*, 1958:1462-1483).

The SLI LABs are designed for delivering short, quick-burst, high currents over a wide range of temperature (Willihnganz, 1952:234C-236C). They are mainly used in automotive applications for cranking of the car engine, lighting and sometimes applied in electric vehicles (Morehouse *et al.*, 1958:1462-1483, PC-Control, 2008). The deep cycled LABs are designed to withstand frequent deep discharges in contrast to partial discharges in the case of SLI batteries. They are specifically designed for prolonged use (can deliver power for up to 10 hours). They, however, require longer charging times than is appropriate for regular batteries (PC-Control, 2008, Scherz & Monk, 2013). The stationary batteries are designed for long-life applications, which do not require the mechanical ruggedness or high current output. Low self-discharge, stability and high efficiency are important features. Most of the stationary batteries use pasted positive plate construction similar to the motive battery. They have a lower self-discharge rate due to the usage of pure lead or a lead-calcium alloy in their electrodes as against lead-antimony alloy used in other battery types that often results in a high self-discharge rate.

The advantages of lead acid batteries include low cost, high voltage per cell, good capacity life and good performance at room temperatures. However, they are relatively bulky with poor low temperature characteristics and cannot be left in the discharged state for too long without damage.

2.3.2 Alkaline secondary batteries

Alkaline secondary batteries are a group of rechargeable batteries, which depend on an aqueous solution of alkaline based electrolytes, such as potassium hydroxide (KOH) or sodium hydroxide (NaOH), to function as contrary to acid electrolyte in lead acid batteries. In addition, the active charge transport element within the batteries during their electrochemical processes is oxygen or hydroxyl ions and owing to this, they retain their electrolytes' concentration during charge-discharge mechanisms, thereby prolonging their service life (Reddy, 2002). Although, they are higher in cost when compared to LABs, they have special dominating characteristics of high continuous power provision capacity, fast recharge and long service life, especially in energy turnover (Köhler *et al.*, 2004:45-52). The alkaline batteries are also known as nickel batteries (Crompton, 2000) and some of the common examples of this technology include nickel-cadmium (NiCd), nickel-metal hydride (NiMH), nickel-iron (NiFe) and nickel-zinc (NiZn) batteries (Köhler *et al.*, 2004:45-52). Others include manganese-zinc (the only alkaline battery that does not use nickel electrodes), sodium-nickel chloride, nickel-hydrogen (NiH) and silver-hydrogen batteries (Crompton, 2000).

***2.3.2.1 Nickel-cadmium (NiCd) batteries*:** The NiCd batteries are the dominating alkaline secondary batteries ranging from the small sealed button and cylindrical cells to larger vented cells with capacities over 1000 Ah, which can be used for standby and emergency power systems such as in photovoltaic applications (Anglin & Sadoway, 2014, Berndt, 1997). The benefits of nickel cadmium batteries lie in their mechanical ruggedness, long service life and excellent low temperature characteristics (-54°C to 82°C). They can be trickle-charged and when standing idle, evolve practically no gas and thus can be hermetically sealed. In addition, they are chemically stable because their electrode materials are less reactive with alkaline electrolytes (Reddy, 2002, Crompton, 2000, Morehouse *et al.*, 1958:1462-1483). However, they are more expensive than lead acid batteries and are often faced with the memory effect − a situation in which a nickel battery (NiCd or NiMH) 'remembers' its previous low charge capacity level and apparently tends to

conform to such duty cycle that does not involve full discharging, consequently losing its maximum energy capacity (Reddy & Linden, 2011, Sato *et al.*, 2001:20-24, Sato *et al.*, 1996:L225-L228).

***2.3.2.2 Nickel-Metal Hydride (NiMH) batteries*:** The introduction of NiMH batteries has taken a significant preference over NiCd batteries due to their better technical properties, which lack poisonous heavy metals such as cadmium. NiMH technology is based on the reaction between nickel and metallic alloys in a potassium hydroxide (alkaline) solution. The metallic alloy, which would have the ability to absorb smaller hydrogen atoms in the interstices between the larger metal atoms are used to provide the active materials for the negative electrode in the cell (Crompton, 2000, Buchmann, 2013). NiMH batteries exhibit more superior practical energy densities (25-30% more) and higher capacity per unit mass compared to corresponding nickel cadmium (NiCd) batteries. Their intrinsic voltage (1.2 to 1.35v/cell) is similar to NiCd, which makes them compatible in applications where NiCd batteries are used. The challenge with NiMH is the instability of the metal hydride. More so, they are considerably expensive, though still competitive for consumer and industrial products (Beaty & Fink, 2013, Crompton, 2000).

***2.3.2.3 Nickel iron (Ni-Fe) batteries*:** A Ni-Fe battery is often called the Edison battery as it was discovered by Edison in 1900 (Tuck, 1991). It consists of pockets of iron (Fe) active material at the anode, while the cathode is an assembly of perforated nickel (Ni) tubes filled with nickel hydroxide and nickel (Morehouse *et al.*, 1958:1462-1483, Reddy, 2002). Ni-Fe batteries are widely used in heavy duty industrial and railway applications, underground vehicles, rapid-transit cars and can also be used in stationary applications such as in photovoltaic applications due to their extreme ruggedness, long life and durability. However, they are limited in usage due to their low specific energy, poor charge retention, poor low-temperature performance and high manufacturing cost, compared to the lead-acid battery. Furthermore, because of the instability of the Fe anode, they are vented, and this may require regular maintenance (Crompton, 2000, Reddy, 2002, Köhler *et al.*, 2004:45-52).

***2.3.2.4 Nickel-hydrogen (NiH) batteries*:** In order to retain all the benefits of NiMH, while eliminating the problem of metal hydride instability associated with them, the nickel hydrogen (NiH) battery was developed. NiH uses a steel canister to store hydrogen at a pressure of 1,200psi

(8,270kPa). The cell includes solid nickel electrodes, hydrogen electrodes, gas screens and electrolytes that are encapsulated in the pressurised vessel (Crompton, 2000, Buchmann, 2013). The benefits of NiH batteries over the NiMH and other nickel batteries include long service life, full discharge cycles, low corrosion, minimal self-discharge and a remarkable temperature performance of -28°C to 54°C (-20°F to 130°F). However, due to their relatively low specific energy (40-75Wh/kg) and very high cost, they are limited in application to satellite applications, so they are hardly used in photovoltaic applications.

2.3.3 Silver batteries

The most common types of silver batteries are silver zinc and silver cadmium batteries, while the other types such as silver-hydrogen and silver-metal hydride have been the subject of development activity but have not reached commercial viability.

***2.3.3.1 Silver-zinc (zinc-silver oxide)*:** Silver-zinc batteries exist both in rechargeable and non-rechargeable forms. The rechargeable silver-zinc batteries are otherwise known as zinc-silver oxide batteries because they are made of a metallic zinc anode and a silver oxide cathode immersed in an aqueous solution of potassium hydroxide electrolyte (Anglin & Sadoway, 2014). The batteries are light-weight and can provide high specific energy and power up to five times greater than the lead-acid, nickel-iron, or nickel-cadmium storage batteries. Also, they are mechanically rugged and offer good shelf life. A button cell silver zinc is suited for hearing aids, instruments, photographic applications, electronic watches and low power devices, while the larger size silver zinc batteries are used in submarines, missiles, underwater and aerospace applications (Electropaedia, 2005). However, they are not in wide commercial use since the silver utilised greatly increases production costs. More so, they have a shorter life cycle than the conventional storage batteries and are sensitive to overcharging (Crompton, 2000, Morehouse *et al.*, 1958:1462-1483).

***2.3.3.2 Silver-cadmium (cadmium silver oxide)*:** Silver-cadmium batteries are similar in construction to silver-zinc batteries except for the replacement of the zinc sponge anode with a cadmium sponge. The silver-cadmium battery combines the high capacity features of the silver oxide cathode with the favourable cycling and low-discharge rate characteristics of the cadmium anode. Currently, they have the ability to supply high energy density, which is about 2.5 times

higher than NiCd batteries. They are resistant to overcharging with a significantly longer cycle life. Compared to silver zinc, they have better low-temperature performance (Morehouse *et al.*, 1958:1462-1483). However, they are very expensive considering the fact that two of the more costly electrode materials (silver and cadmium oxide) are used in their construction. Owing to this, they are limited in commercial production; hence, they are used in special applications, such as nonmagnetic batteries and space applications. Compared to silver-zinc batteries, they give about 40 per cent less capacity and are not suitable for high rate discharge. They are recommended for low rate and long cycle life applications (Morehouse *et al.*, 1958:1462-1483).

2.3.4 Lithium batteries

It has become clear over the past few years that a higher energy density system from hermetically sealed cells at a reasonable cost could not all be supplied by mercury, silver, or alkaline manganese dioxide systems; hence, the need for the introduction of the lithium battery system. Lithium batteries contain organic electrolyte lithium and can offer gravimetric energy density of up to 330 Wh/kg, nearly three times that of mercury and silver batteries and four times that of alkaline manganese batteries, among other advantages (Crompton, 2000, Cairns & Albertus, 2010:299-320). The most common type of lithium batteries is lithium ion (Li-ion) batteries while with the recent advancements, there has been an introduction of lithium polymer batteries. Research is still ongoing with respect to the other lithium technologies such as lithium-molybdenum disulphide and lithium (aluminium) iron monosulphide batteries (Crompton, 2000).

***2.3.4.1 Lithium ion*:** The lithium-ion (Li-ion) battery technology was introduced commercially in 1991 by Sony. They are made of a lithium carbonate (LiC_6) anode and a lithium cobalt oxide ($LiCoO_2$) cathode, separated with microporous polypropylene in a non-aqueous and aprotic electrolyte. The anode allows the conduction and intercalation of lithium at potentials near that of pure lithium, while the cathode enables the transition of lithium ion between the electrodes. The electrolyte contains organic solvent (equal ratio of ethylene carbonate and propylene carbonate) and its conductivity is increased with the introduction of lithium salt (such as lithium hexafluorophosphate, $LiPF_6$). They have a nominal voltage of 3.6 V per cell and a specific energy of about 125 Wh/kg in commercially available lithium ion batteries. However, their theoretically

specific energy with the $LiCoO_2$ cathode could be up to 770 Wh/kg (Anglin & Sadoway, 2014, Cairns & Albertus, 2010:299-320)**.**

Due to their high specific energy and long cycle life (more than 1000 deep cycles), lithium-ion batteries currently have top usage in applications requiring portable power such as laptop computers, cell phones, camcorders, cameras and power tools (Nagaura & Tozawa, 1990:209, Ozawa, 1994:212-221, Mikolajczak *et al.*, 2012). Meanwhile, there has been a recent development of a lithium ion battery designed for photovoltaic applications due to their combination of advantages of high energy density and high specific energy. Their cycle life, moreover, is typically greater than 1000 cycles at 80% depth of discharge. As such, Li-ion batteries are displacing NiCd and NiMH from some of their traditional uses. However, they are very expensive (about $20,000/ kWh initial cost); hence, could be used only in applications that would tolerate this cost. More so, their performances are damaged from overcharging and undercharging so they require an external circuitry of a BMS to protect their cells from extreme charging conditions and this leads to an increased operational cost (Köhler *et al.*, 2004:45-52, Anglin & Sadoway, 2014, Cairns & Albertus, 2010:299-320).

2.3.4.2 Lithium (ion) polymer**:** These are lithium rechargeable batteries based on solid polymer electrolyte technologies. Lithium polymer batteries consist of complex solid polymer electrolytes (SPEs) formed by poly-ethylene oxide and a lithium salt, such as $LiCF_3SO_3$ (Scrosati *et al.*, 2001:93-100). The polymer electrolyte allows flexible, different shape, thin configurations in the production of rechargeable lithium polymer batteries; this property being a highly desirable feature in advanced battery technology (Scrosati *et al.*, 2001:93-100). The lithium polymer batteries, furthermore, are highly reliable and safe batteries, having high energy density, high specific energy and a long cycle life. Thus they are being used for extremely demanding applications, such as electric vehicles (EV), starting-lighting and ignition (SLI) and portable electronic and personal communication (Fauteux *et al.*, 1995:2185-2190). More recently, lithium polymer batteries are being used in photovoltaic applications, for example the "Solar-impulse 2" (Pleasance & O'Callaghan, 2015), a solar-driven airplane mainly powered by lithium polymer batteries and recharged by solar energy.

2.4 BATTERY MANAGEMENT SYSTEM (BMS)

A BMS is an electronic system for monitoring and controlling battery bank from extreme operating conditions in order to enable an extended service life for the batteries (Karden *et al.*, 1996:91-98, Jossen *et al.*, 1999:283-286). A BMS is often necessary in applications where batteries are primarily used for electric energy storage and supply. Such applications could include photovoltaic applications, uninterruptible power supply (UPS) systems, battery electric vehicles and electric load levelling systems. A schematic structure of a typical BMS is shown in the Figure 2.

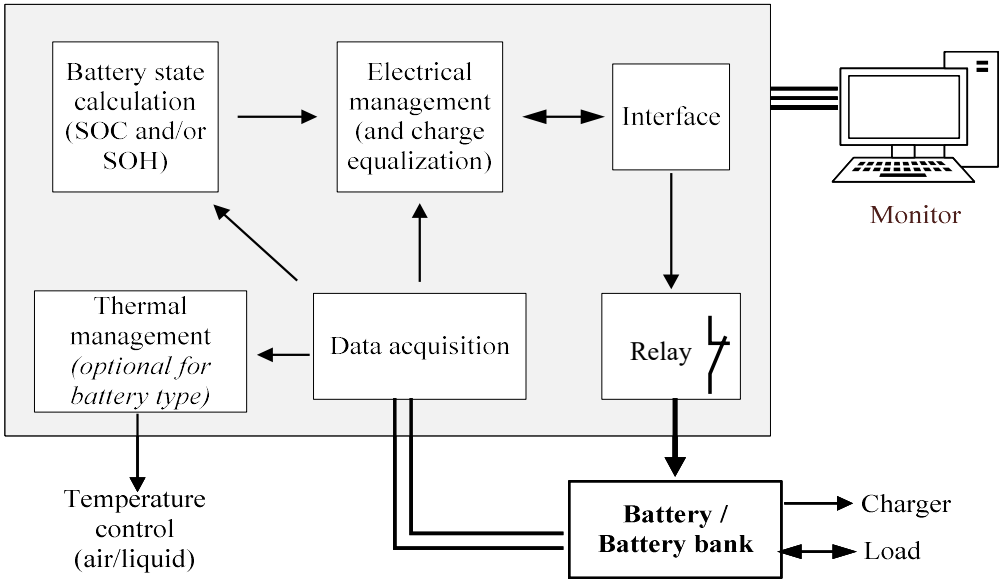


Figure 2: Schematic structure of a battery management system (BMS) (Jossen *et al.*, 1999:283-286)

2.4.1 Design consideration of a battery management system (BMS)

According to the experimental and existing BMS studies, the design consideration of a BMS should importantly provide a full battery equalisation capability among other features (Karden *et al.*, 1996:91-98, Jossen *et al.*, 1999:283-286). In most cases, the features to be considered for a typical BMS design depend on the battery type and the applications where the system is to be used. Meanwhile the basic features in the design of BMS for most conventional batteries include the following (Jossen *et al.*, 1999:283-286, Chatzakis *et al.*, 2003:990-999):

- Data acquisition

- Battery SOC determination
- Safety management (charge equalisation, overcharge- and under voltage protection)
- Communication.

2.4.2 Battery management systems (BMSs) in photovoltaic applications

In photovoltaic applications, a complete BMS for batteries would include the following:

- An array of PV panels, which supplies an unregulated DC voltage and current for charging a battery string/bank.
- A charge controller, which regulates the PV supply voltage and current using the maximum power point tracking (MPPT) or pulse width modulation (PWM) technique.
- A battery string or battery bank, which stores the supplied photovoltaic energy.
- A battery charge equaliser, which is applied across the battery strings or banks based on the suitable equalisation technique.
- A data logger, which measures and records the battery string charging states and parameters in the real time.
- A battery monitor, usually a computer interface where the SOC and equalisation of the batteries in the strings/bank can be observed in real time.

A typical block diagram of BMS in a photovoltaic (stand-alone) application as proposed in this research is shown in Figure 3.

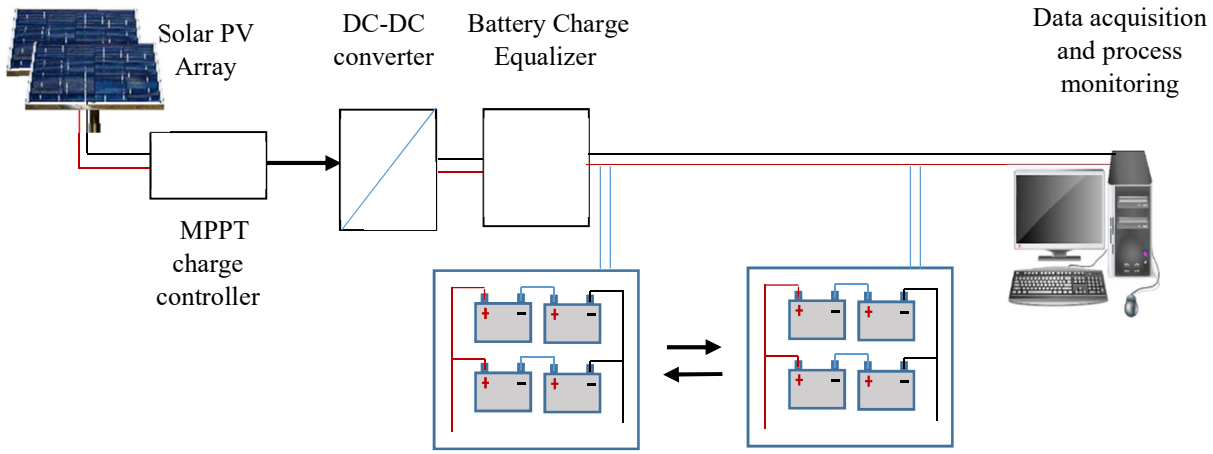


Figure 3: Block diagram of the typical BMS in photovoltaic application (Chatzakis *et al.*, 2003:990-999, Duryea *et al.*, 1999:2649-2654)

2.5 PHOTOVOLTAIC APPLICATIONS

The photovoltaic systems are used in variety of applications. These applications can be categorised into utility interactive (or grid-connected), stand-alone and hybrid systems (Center, 2002:1-4, Pearsall & Hill, 2001:1-42). The hybrid system consists of either a grid-connected or stand-alone system that is integrated with one or more alternative power supplies, for example diesel generator or wind turbine in order to meet more load requirements (Pearsall & Hill, 2001:1-42).

2.5.1 Utility interactive (or grid-connected) system

The utility interactive or grid-connected system enables the backup of excess photovoltaic (PV) energy generated during the day on the utility grid through a feedback-into-the-grid process. This process is done by connecting the PV system into a high quality inverter, which converts the direct current output of the PV system into an alternating current electricity that is in phase with the grid electricity supplied by the power company (Pearsall & Hill, 2001:1-42). Meanwhile, when a PV system generates less energy than is required, with utility interactive systems, the supplementary energy required is supplied by the local power company. The process of the utility interactive photovoltaic system is depicted in Figure 4.

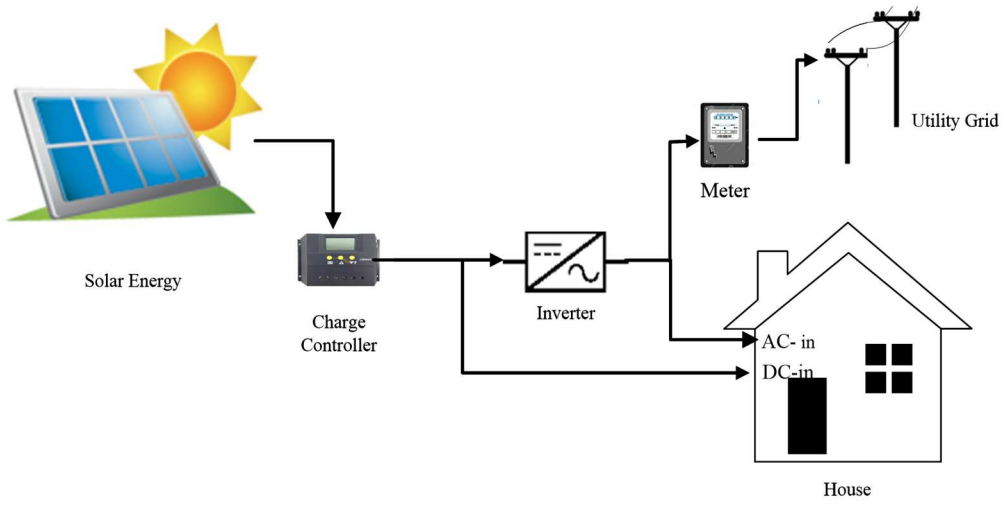


Figure 4: Utility interactive photovoltaic system (Pearsall & Hill, 2001:20, Center, 2002:1)

These interactive systems allow an offset of electricity costs for homes and commercial buildings. However, due to some control strategies, safety government policy etcetera (Obi and Bass,

2016:1082-1094), the implementation of this system in some part of the world is currently restricted.

2.5.2 Stand-alone systems

A more common photovoltaic application is found in stand-alone systems. A stand-alone system is an isolated system which generates electricity from a PV system and directly uses the electricity to power different applications without feeding back the excess into the utility grid system (Center, 2002:1-4, Pearsall & Hill, 2001:1-42). In stand-alone systems, the excess energy generated by the PV systems is stored in an intermediate energy storage device, usually a battery bank set up between the PV system and the end-application. The battery direct current (DC) charge could be used to directly power some applications that require a DC to function or rather be converted to an alternating current (AC) electricity using an inverter in order to power devices that operate on AC. PV stand-alone systems are commonly applied in the applications such as industrial and small scale household lighting, communications, remote site electrification, traffic and street lighting, remote monitoring, electric vehicles, etcetera. The process of a stand-alone photovoltaic system is depicted in Figure 5.

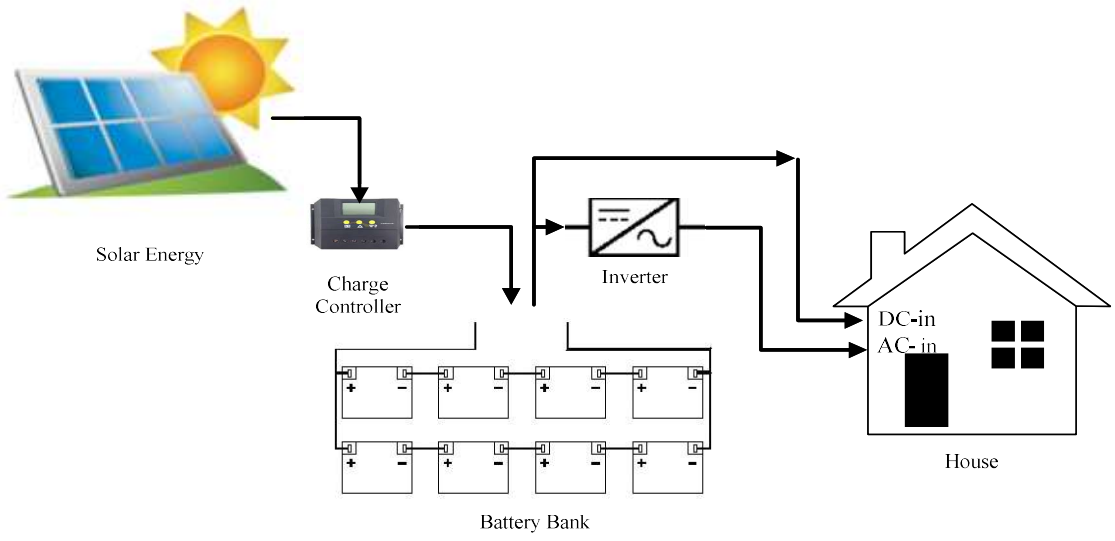


Figure 5: Stand-alone photovoltaic system (Pearsall & Hill, 2001:20)

Meanwhile, beside the battery electric vehicle, there are more recent developments in the transportation industry that depend on a stand-alone photovoltaic system to function. Some of

these include the solar-driven airplane, such as the solar-impulse 2 (Si2) currently under world test flight (Pleasance & O'Callaghan, 2015) and the solar-powered bus train recently exhibited in China (Thompson, 2016).

2.6 BATTERY CHARGING AND CHARGE IMBALANCE

For a proper recharging of a rechargeable battery, the battery must be charged in stages. Meanwhile, when batteries in a series string are charged or discharged together, they are often faced with the challenge of charge imbalance, which could damage the entire battery string in a short while. In order to reduce or eliminate this charge imbalance, the charge on a battery string must be equalised.

2.6.1 Solar charge controller

A solar charge controller is an essential part of the photovoltaic system. It is an electronic device, which regulates the voltage and current supplies from solar panels to the batteries and protects them from extreme charging conditions as the atmospheric weather condition changes. (Koutroulis & Kalaitzakis, 2004:191-197). Solar energy supply depends on the sun's availability; meanwhile its supply to a charge controller in photovoltaic applications can be affected by the average atmospheric weather condition such as the cloud's movement.

Charge controller can either be programmable or non-programmable. In most programmable types, such as shown in Figure 6a, charge equaliser circuits are mostly incorporated but this incurs more cost of implementation to a BMS. However, in typical non-programmable types such as shown in Figure 6b, the cost of implementation is relatively low while charge equaliser circuit may be locally designed and incorporated into the BMS design.

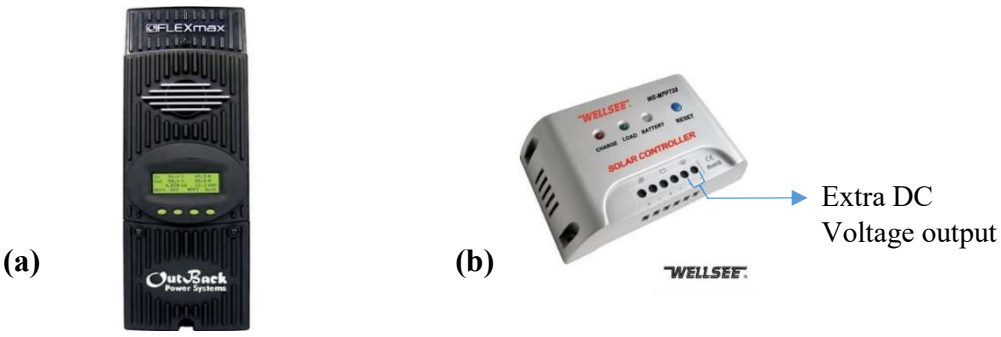


Figure 6: Typical solar charge controllers a) "FLEXmax" programmable charge controller b) "WELLSEE" non-programmable charge controller

The latter is cost effective for household and small scale stand-alone photovoltaic application. Meanwhile both types consist of input terminals for solar energy supply, output ports for battery terminals connection and extra DC voltage output terminal, which can power any other device that operates within such DC voltage range.

2.6.2 Three-stage charging method of battery

The common three-stage method, either by a smart charger or solar charge controller, which ensures that a battery attains 100% SOC, is bulk, absorption and float charging (Armstrong *et al.*, 2008:1469-1475, Mayfield, 2010:141-143). Figure 7 shows a typical graphical curve of voltage and current of a battery during this three-stage charging process.

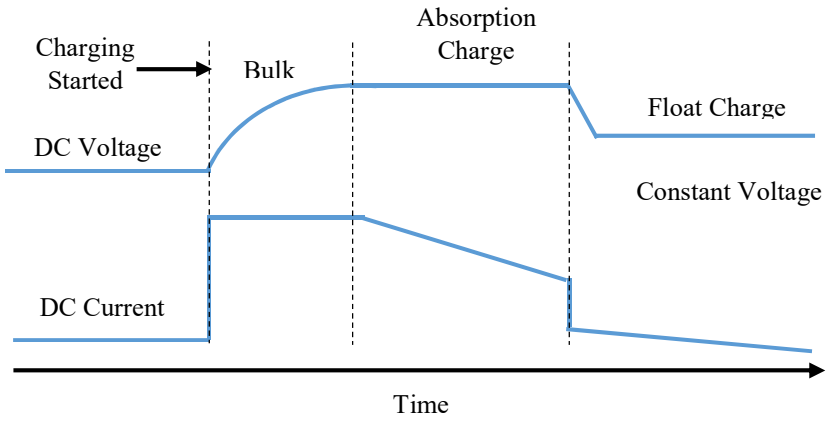


Figure 7: Three-stage charging curve of rechargeable batteries (Mayfield, 2010:141-143)

- **Bulk charging:** During the bulk stage, a relatively high charging current is held constant by the charge controller against the rising internal resistance of the battery and, hence, the voltage rapidly rises to about 80-90% SOC, (attaining between 14.4-14.6 volts for lead acid batteries) (Armstrong *et al.*, 2008:1469-1475, Mayfield, 2010:141-143).

- **Absorption charging:** During the absorption stage, battery charge voltage is held constant at the bulk voltage level for a period of time (usually about one hour) by the charge controller, while the current gradually tapers off due to an increased internal resistance of the battery as it charges up. This allows the battery to be charged up to 98% SOC (Armstrong *et al.*, 2008:1469-1475, Mayfield, 2010:141-143).

• **Float charging:** During the float charging stage, the charging voltage is dropped to a level, which is below the absorption charge voltage, (this is usually between 13.4 to 13.7 volts for lead acid batteries) and the batteries draw a very minimal maintenance current continuously. This stage finally brings the battery to a 100% SOC and maintains this charge level continuously to compensate for the battery self-discharge (Armstrong *et al.*, 2008:1469-1475, Mayfield, 2010:141-143).

2.6.3 Battery charge imbalance

Battery charge imbalance is the difference in SOC levels of batteries when connected in a series string or a bank. The charge imbalance occurs due to the variations in the operating conditions of the batteries such as external load mismatch or through the inherent differences in the chemical properties of the batteries. Mostly, charge imbalance among batteries can be caused by two categories of factors: the internal sources and the external sources (Park *et al.*, 2009:3216-3223, Cao *et al.*, 2008:1-6).

The charge imbalance from the internal source factors is due to the differences in the electrochemical characteristics of the batteries, which consist of manufacturing variance in physical volume, variation in internal impedance, different SOH and different self-discharge rate (Park *et al.*, 2009:3216-3223, Gallardo-Lozano *et al.*, 2014:934-949). The charge imbalance caused by the external source factors is due to an unequal draining of charge externally from some individual batteries that constitute the bank through a load, protection ICs, or different thermal variation across the pack (Kim *et al.*, 2012:411-424, Han *et al.*, 2014:158-163, Cao *et al.*, 2008:1-6). These factors result in different self-discharge rates of the batteries across the battery bank.

2.7 BATTERY CHARGE EQUALISATION AND METHODS

Battery charge equalisation is a process of eliminating the charge imbalance among battery strings/ banks through a SOC balancing of the batteries using a certain charging device and control rules. Battery charge equalisation enables batteries to be charged up to their maximum capacity while not being subjected to an overcharge state (Krein & Balog, 2002:516-523, Peiying Li, 2011:141-144). More so, this prevents the batteries from quick degradation and accelerated ageing. Of more noticeable importance of charge equalisation to a battery string or bank is an extended service life,

which is a function of a good SOH of the batteries. Various charge equalisation techniques for the proper BMS have been proposed by several authors (West & Krein, 2000:439-446, Moo *et al.*, 2003:704-710, Krein & Balog, 2002:516-523, Hung *et al.*, 1993:96-104) and these can be grouped into three types: battery selection, passive methods and active methods (Gallardo-Lozano *et al.*, 2014:934-949).

A summarised classification of these charge equalisation techniques is shown in Figure 8; the highlighted technique trend was adopted in this research. The reasons for which are further explained in the subsequent chapters of this work.

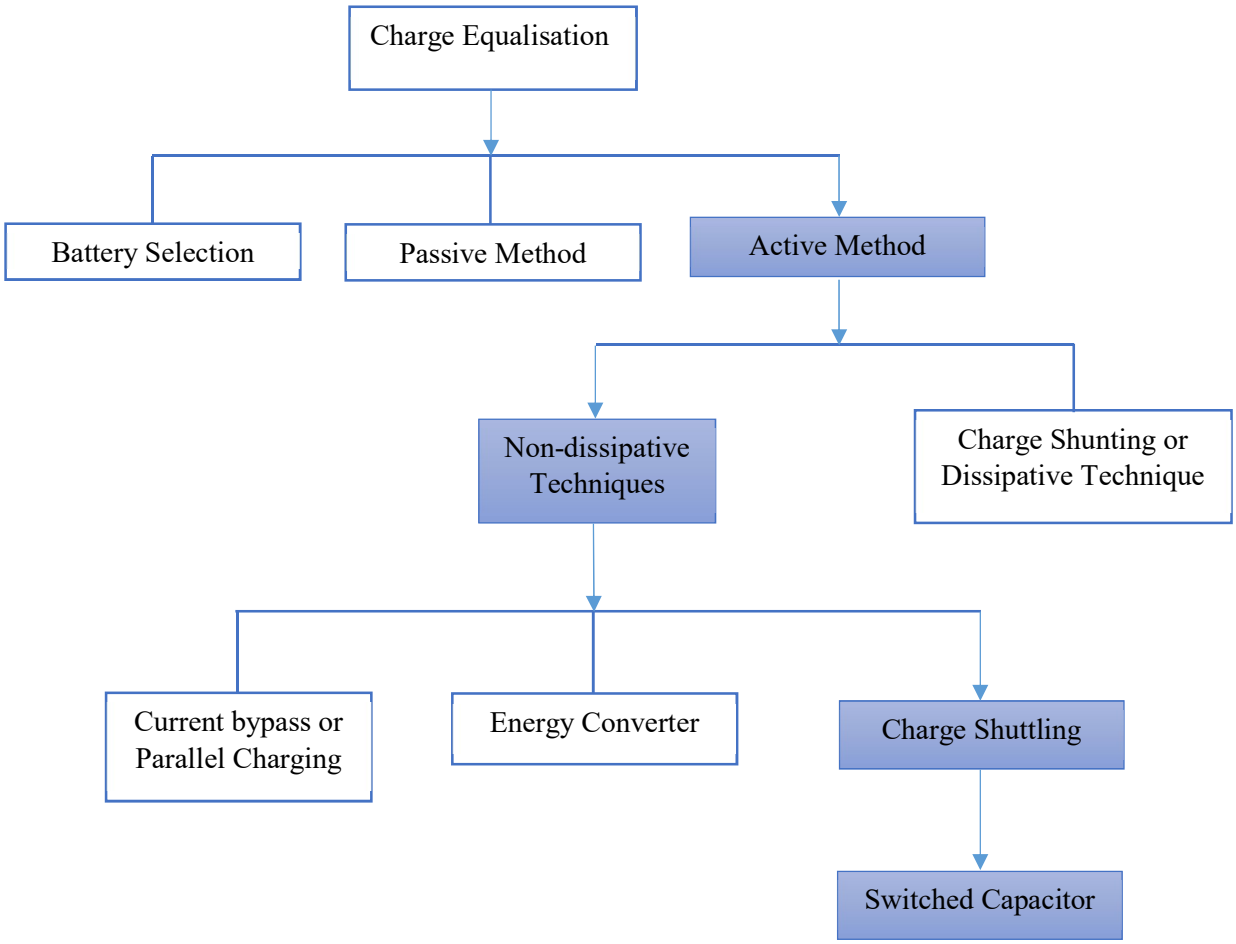


Figure 8: Classification of equalisation technique

2.7.1 Battery selection method

This method involves the grouping of batteries, which have similar electrochemical properties together during charging. This is because such batteries are expected to have similar SOC or SOH

levels, the same measured capacity, the same age and the same chemical compositions. However, this method is not very efficient due to the individual self-discharge rates of batteries, which vary from one battery to another. This results in charge imbalance among battery strings over a period of operation. Also, the cell impedance and capacity of the batteries may vary along the battery service life and this can also lead to a divergence in SOC levels among batteries in a string (Uno & Tanaka, 2012:4704-4712).

2.7.2 Passive method

The passive method of charge equalisation among batteries balances through a forced overcharge and/ or dissipation of excess energy through a bypass shunting resistor across each battery as shown in Figure 9 (Cadar *et al.*, 2010:1221-6542, Gallardo-Lozano *et al.*, 2014:934-949). A forced overcharged method is often used with valve-regulated lead-acid (VRLA) batteries (West & Krein, 2000:439-446) because these batteries are constructed with several design features such as recombinant catalyst technology that recovers water as gas is produced during overcharging to mitigate imbalance problems (Misra *et al.*, 1999:8 pp.).

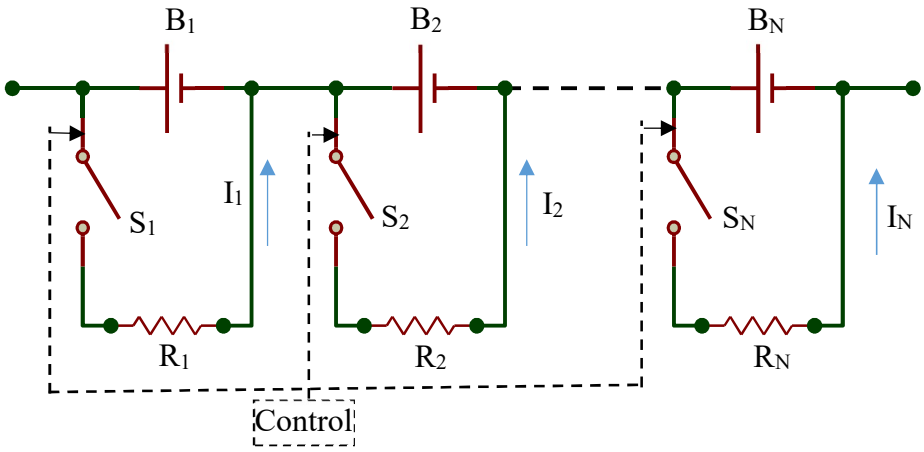


Figure 9: Equalisation with shunting resistor (Cadar *et al.*, 2010:1221-6542)

However, a forced overcharge has a negative effect on the battery service life and it creates large inefficiency during the charging process (West & Krein, 2000:439-446). In a dissipative method, a dissipative element such as a resistor (or a transistor operated in its linear regime) is switched on across individual cells as they reach the maximum allowable voltage. The drawbacks to this approach are that it dissipates substantial energy in the form of heat during the equalisation and this thus reduces the overall system efficiency (Baronti *et al.*, 2014:1811-1816).

2.7.3 Active methods

The active charge equalisation methods balance battery SOC use external circuits, which actively transport energy among the batteries in a string. The active methods are preferred to the battery selection or passive method due to their higher efficiency and applications to different battery chemistries and types (Fukui & Koizumi, 2013:6715-6720, Cadar *et al.*, 2010:1221-6542, Gallardo-Lozano *et al.*, 2014:934-949). Based on energy transfer among the batteries, active charge equalisation methods can be categorised into four designed topologies, which are charge shunting, current by-pass, energy converter and charge shuttling.

***2.7.3.1 Charge shunting*:** The charge shunting method is otherwise known as end-of-charge cell balancing (Moore & Schneider, 2001). It diverts the excess energy in each battery through a resistor or other load round the battery when the voltage exceeds a predetermined level or selectively shunts the charging current around each cell as they become fully charged. The method of predetermining the limit of battery charge voltage is mostly done either by using a zener diode (Z) or a voltage comparator circuit as shown in figures 10a and 10b respectively.

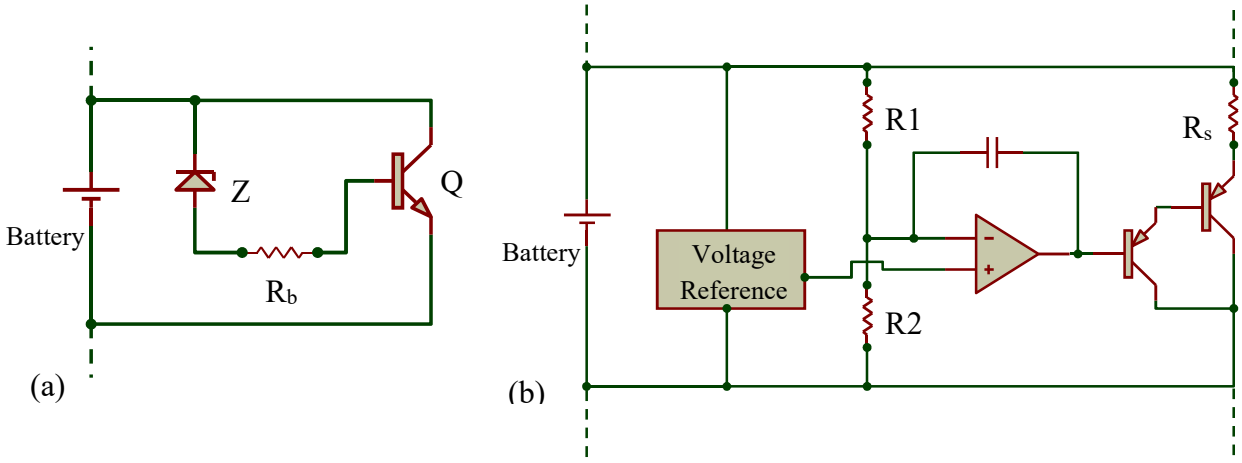


Figure 10: Analog shunt equaliser (a) with a zener diode reference circuit (b) with voltage comparator circuit (Yarlagadda, 2011:1-124)

When battery voltage exceeds the limit indicated by Z in Figure 10a, excess charge is selectively shunted around the battery through the transistor Q. Similarly, in Figure 10b, the comparator circuit selectively shunts the excess charge round the circuit through the shunt resistor R_s when the battery voltage exceeds the limit indicated by the comparator. The shunt resistor is sized to shunt exactly the charging current when the fully charged cell voltage is reached. To avoid extremely large

power dissipations due to the resistor, this method is best used with stepped-current chargers with a small end-of-charge current. Disadvantages of this method include the dissipation of too much energy in the form of heat and through the large power dissipating resistors, thus reducing the efficiency of the charging system.

***2.7.3.2 Current by-pass (or parallel charging)*:** Series-connected batteries are charged in parallel at a constant current until all cells reach the maximum voltage, then current is allowed to taper. Charging is terminated when charging current to all cells reaches 10% of the initial constant current. In this arrangement (Teofilo *et al.*, 1997:30-36), switches or relays reconfigure the battery pack. During discharge, a series connection is used while during charging, the pack is reorganised to place the smallest allowable units in parallel to assure equal voltage charging. A key drawback of this approach is that it is difficult to scale to large series strings (West & Krein, 2000:439-446). Also, the need to reconfigure requires a distinction between charge and discharge sequences that is inconvenient in many applications.

***2.7.3.3 Energy converters*:** The battery charge equalisation technique that utilises an energy conversion method employs inductors or transformers to move energy from a cell or group of cells to another cell or group of cells. The methods adopted in this technique include the use of multiple transformer, single/ multi-windings transformer, single/ multi switched inductor, buck-boost DC converter, flyback energy converter, etcetera (Daowd *et al.*, 2011:2974-2989). Figures 11-16 show the schematic diagrams of these basic design topologies respectively.

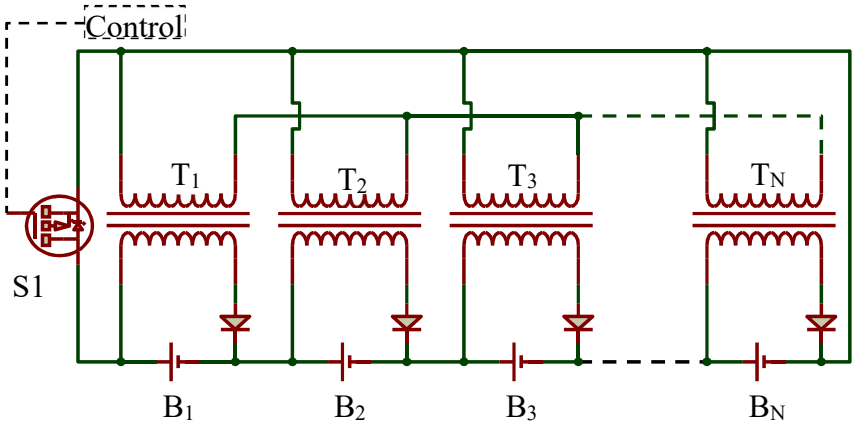


Figure 11: Multiple transformer balancing topology (Daowd *et al.*, 2011:2974-2989)

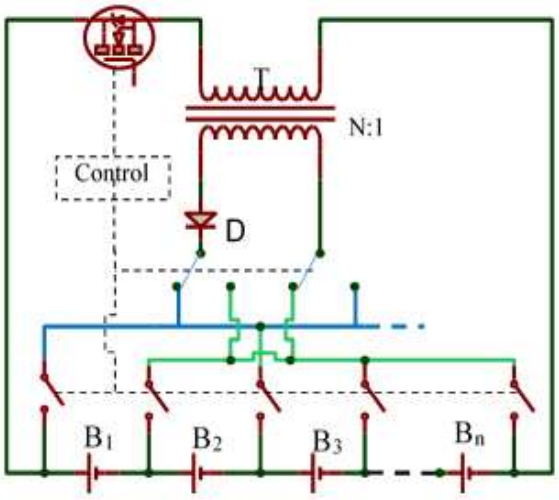


Figure 12: Single windings transformer balancing topology (Daowd *et al.*, 2011:2974-2989)

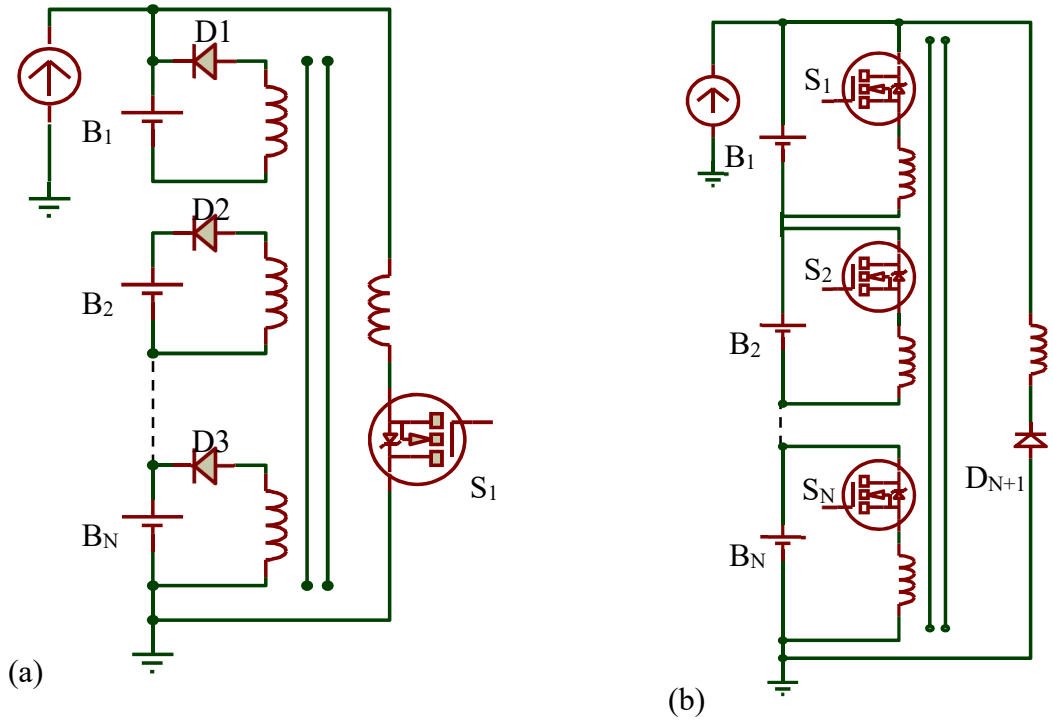


Figure 13: Multi-windings transformer balancing topology a) flyback structure b) forward structure (Daowd *et al.*, 2011:2974-2989)

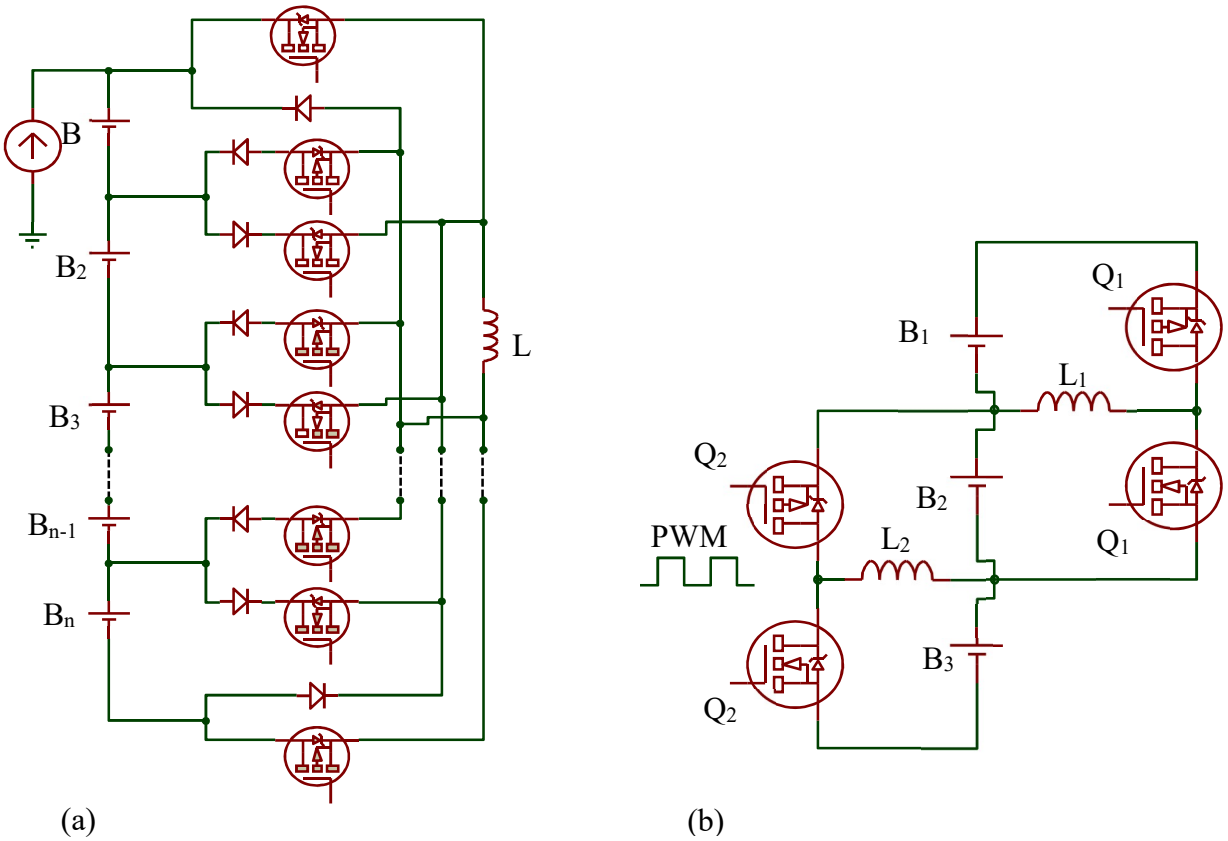


Figure 14: Single/multi inductor balancing topologies a) single-inductor and b) multi-inductor (Daowd *et al.*, 2011:2974-2989)

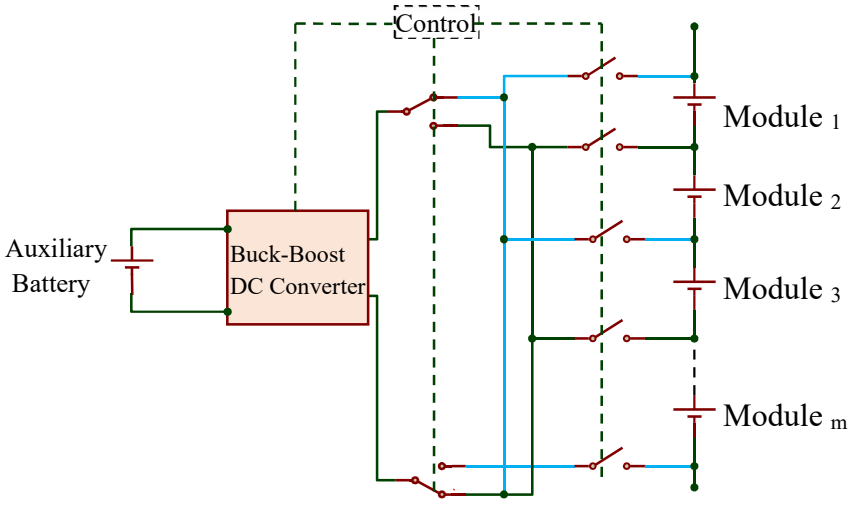


Figure 15: Buck-boost DC converters (BBC) cell balancing topology (Daowd *et al.*, 2011:2974-2989)

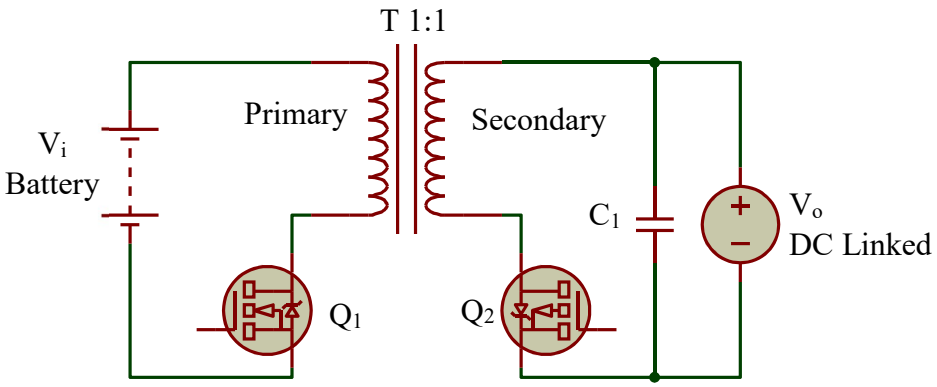


Figure 16: Flyback energy converter balancing topology (Daowd *et al.*, 2011:2974-2989)

The main disadvantages of these methods are their relatively high cost and magnetic losses for the transformers. In addition, filter capacitors must be connected across each battery to filter the high switching frequency, thus this increases the cost in the implementation of the technique. Also, this technique takes a relatively long equalisation time, especially when implemented for a long string of battery pack (Daowd *et al.*, 2011:2974-2989).

***2.7.3.4 Charge shuttling*:** The charge shuttling equalisation technique consists of an active energy storage device, such as a capacitor, which stores the charge from a selected cell or battery and transfers it to or shuttles it with another cell or battery using a set of switches, which may be logically controlled. The capacitor can be referred to either as a shuttling capacitor or a flying capacitor. In a more specific term, shuttling capacitor is mostly adopted in the design of a DC-DC converter while a flying capacitor is usually used in the design of a charge pump although the capacitors perform similar functions of charging and discharging for a particular purpose in a circuit. In battery charge equalisation design, this capacitor is referred to as a shuttling capacitor. Charge shuttling capacitor method for battery equalisation can be categorised into four, which are switched capacitor, double-tiered switched capacitor, single switched capacitor and modularised switched capacitor (Daowd *et al.*, 2012:0385, Moore & Schneider, 2001).

2.8 CAPACITOR CHARGE SHUTTLING ANALYSIS DURING BATTERY CHARGE EQUALISATION

This process of capacitor shuttling for charge equalisation has a simple control strategy and high efficiency, however, with a relatively long equalisation time and relatively high cost (Daowd *et*

al., 2013:2149-2174). Meanwhile, since this technique uses a capacitor as the main charge shuttling device, there is a benefit of using the technique to equalise different battery types. This is because the charging process of capacitors depends only on a DC voltage source, thus when a capacitor is charged by a battery, it assumes the battery as a DC voltage source and hence does not depend on the electrochemical properties of the batteries involved. This then can make this technique suitable for the design of a battery charge equaliser, which can be used in different applications. In the configuration detail above and the ones in the following sections, every two-MOSFET connected as a switch was replaced with a single-pole, double-throw (SPDT) switch for simplicity of the design.

2.8.1 Switched capacitor technique

A basic SC technique used in battery charge equalisation is a voltage-based equalisation technique, which involves a direct transfer of charge from a higher charged battery to the lower ones using capacitors. The process of a SC equalisation technique requires *n-1* capacitors to balance *n* batteries as shown in Figure 17.

Each capacitor, *C* is alternately switched across adjacent batteries at a frequency *f* with the aid of *2n* bi-directional switches.

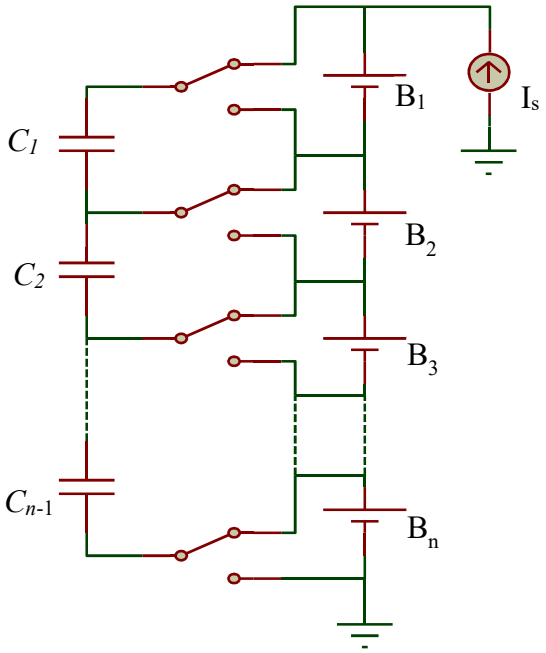


Figure 17: Switched capacitor technique topology (Gallardo-Lozano *et al.*, 2014:934-949)

When the capacitors are switched backed and forth repeatedly across a battery string, their charges are equalised with time thus converging to a relatively equal value (Pascual & Krein, 1997:848-854, Kobzev, 2000:57-59, West & Krein, 2000:439-446, Cao *et al.*, 2008:1-6, Daowd *et al.*, 2012:0385, Daowd *et al.*, 2013:2149-2174, Gallardo-Lozano *et al.*, 2014:934-949).

The main advantages of this SC battery equalisation technique are that, it does not require bulky magnetic components (such as in the energy converter equalisation method) and there is a simplicity of design which allows all the switches which are mostly MOSFETs to be controlled with just a pair of complementary pulse signals. However, the SC topology has a relatively long equalisation time and a quite high cost of implementation (Daowd *et al.*, 2012:0385, Daowd *et al.*, 2013:2149-2174).

2.8.2 Double-tiered switched capacitor technique

The double-tiered switched capacitor (DTSC) is a derivative of the SC method, which uses two capacitor tiers for energy shuttling among the battery pairs (Daowd *et al.*, 2012:0385, Baughman & Ferdowsi, 2005:109-113, Baughman & Ferdowsi, 2008:2277-2285, Daowd *et al.*, 2013:2149-2174). As shown in Figure 18, a DTSC requires n capacitors and $2n$ bi-directional switches for balancing n batteries.

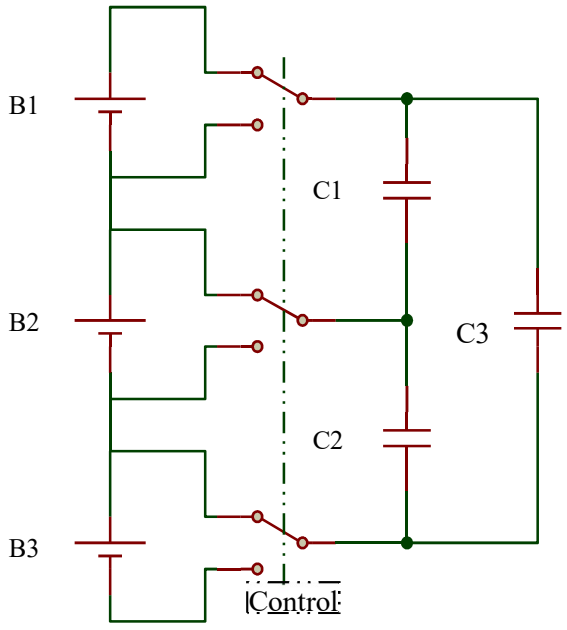


Figure 18: Double-tiered switched capacitor battery balancing topology

Due to more capacitor tiers in this technique, there are more paths between the batteries, thus there is less impedance during charge transport across the battery pack (Baughman & Ferdowsi, 2008:2277-2285). In addition, the second capacitor tier in this topology results in the reduction of the balancing time to more than half of the basic SC topology. However, this topology costs more to implement and requires a more structured control logic switching system than the SC technique.

2.8.3 Modularised switched capacitor technique

The modularised switched capacitor (MSC) method of battery charge equalisation is another topology which utilises the shuttling capacitor method. Adoption of this technique involves the division of the battery pack into groups of twos or modules. In this technique, only two batteries are paired together with one capacitor per time. A typical battery pack modularisation according to Daowd *et al*. is shown in Figure 19 (Daowd *et al.*, 2012:0385).

The system can then be extended to more than two batteries by connecting each battery pair together with another pair through another equalising capacitor. The capacitors are switched at a high enough frequency to move the charge between adjacent batteries.

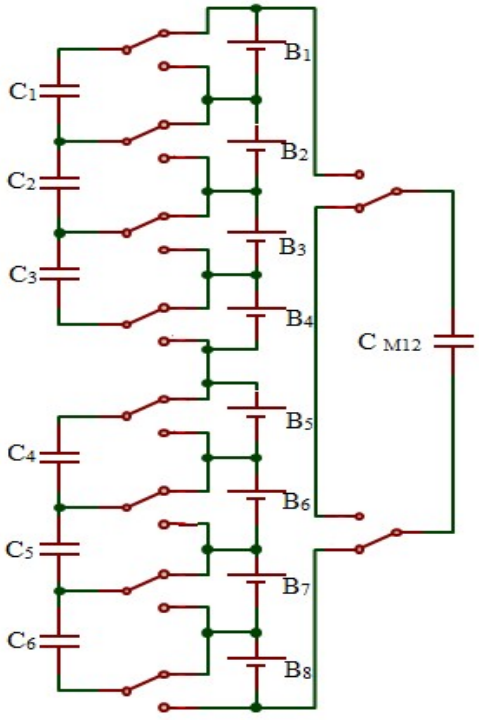


Figure 19: Modularised switched capacitor cell balancing (Daowd *et al.*, 2012:0385)

The difference between an MSC and basic SC technique is that after the SCs C_1, C_2…C_6 have been applied across each module to perform a separate equalisation with individual battery pair, another equalisation system operates on all the modules using a modularised switched capacitor C_{M12}. This technique has the benefit of fast equalisation time. However, due to the increasing number of switches and capacitors, there are more losses and the balancing system costs significantly more.

2.8.4 Single switched capacitor technique

The single switched capacitor (SSC) topology is a derivative of a SC, which makes use of a single capacitor and $n + 5$ bi-directional switches to balance n batteries, thus making it more cost-efficient than SC and DTSC. A basic schematic of SSC equalisation topology as explained in Daowd *et al.*, (2012:0385) and Daowd *et al.*, (2013:2149-2174) is shown in Figure 20.

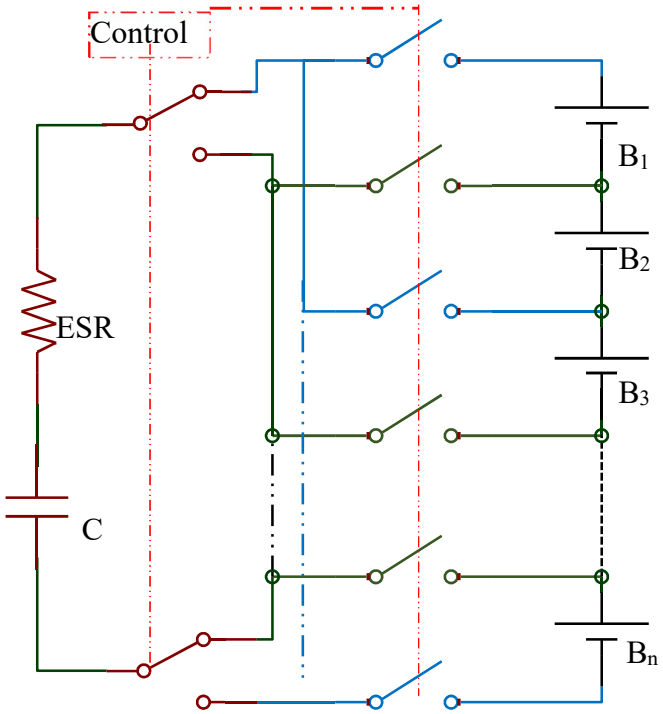


Figure 20: Single switched capacitor battery balancing topology (Daowd *et al.*, 2013:2149-2174)

With the controller, a capacitor is shuttled between high and low energy batteries. The capacitor could be used to balance more than four batteries. The equalisation time for this topology, however, takes longer than the modular or DTSC method.

2.9 SWITCHED CAPACITOR EQUALISATION PROCESS AND EQUIVALENT RESISTANCE MODELLING

When a capacitor is switched across two batteries during a charge equalisation process, the capacitor acts like a parallel resistor across each battery during each charging and discharging process. The knowledge of the equivalent resistance of the capacitor and the switches in parallel across the batteries during switching enables a proper selection of right device components for the design of the SC circuit. This can also give an idea of the equalisation time by taking into consideration the voltage difference between the batteries and the switching frequency.

2.9.1 Analysis of capacitor shuttling process in a circuit

A typical method of capacitor shuttling between two voltage sources in a circuit, which is usually applied in power applications according to Kimball and Krein, (2005), is shown in Figure 21.

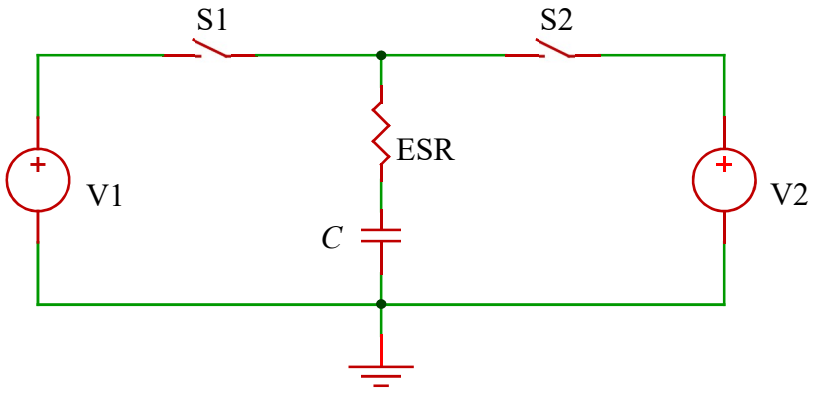


Figure 21: Capacitor shuttling between two voltage sources in a circuit (Kimball & Krein, 2005)

The setup consists of two switches S1, S2 and one capacitor *C* that is shuttled between two voltage sources V1 and V2. ESR is the equivalent series resistance of the capacitor, which is useful for modelling. When S1 is closed and S2 opened, the capacitor becomes connected to the voltage source V1, thus levelling up or down to the charge level of V1. Meanwhile, when the switching is swapped by closing S2 and opening S1, the capacitor is connected to V2 and the attained charged level of the capacitor becomes equalised with V2 (Kimball & Krein, 2005).

To control this circuit with logical controls, the switches can be replaced with MOSFETs Q1 and Q2 which are controlled by two non-overlapping pulse signals φ and $\overline{\varphi}$ as shown in Figure 23.

When a high pulse signal φ is fed into Q1 and low pulse $\overline{\varphi}$ is fed into Q2, Q1 conducts and acts like a closed switch connecting C with V1. When the pulse signals are alternated by feeding φ into Q2 and $\overline{\varphi}$ into Q1, then Q2 only conducts thus connecting C to V2 only. By switching a capacitor among two voltage sources at a defined frequency, the charges of V1 and V2 becomes leveraged with time.

2.9.2 Analysis of capacitor shuttling process in battery strings

When a shuttling capacitor method is implemented for battery charge equalisation, a modification to the circuit in Figure 22 is done by replacing the voltage sources V1 and V2 with batteries BAT1 and BAT2 arranged in series. The two (2) MOSFETs are also replaced with four (4) MOSFETs for proper connections between the battery terminals as shown in Figure 23.

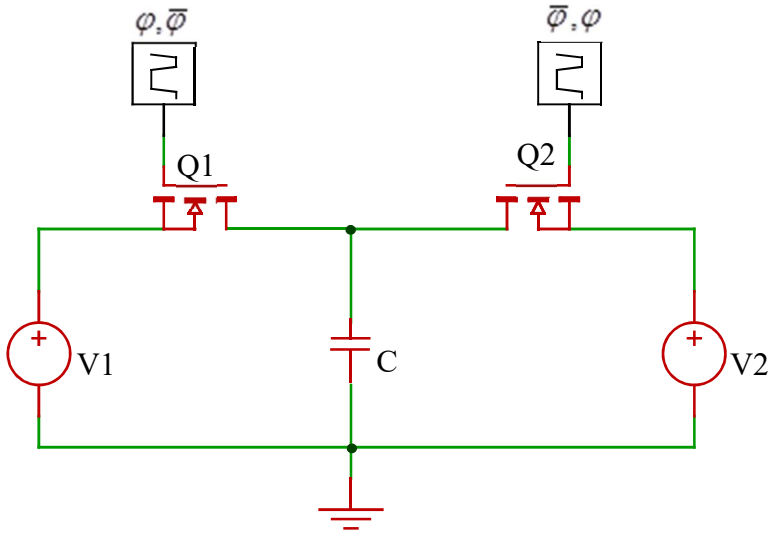


Figure 22: Capacitor shuttling controlled by MOSFETs and non-overlapping pulse signals

In this configuration, the shuttling process of a capacitor for charge equalisation among battery pairs in a series string involves a switching of the capacitor in parallel connection across each battery during the period of the equalisation. The switching is usually done using N-channel MOSFETs, which are logically controlled using high and low pulse signals. A high input pulse signal would enable the MOSFETs to conduct and act like a switch to connect the battery with the capacitor, while a low input pulse signal makes the MOSFETs disconnect the capacitor from the battery.

In Figure 23, when a high pulse signal φ is fed into the Drive1 and low pulse $\overline{\varphi}$ is fed into the Drive2, the transistors Q1 and Q3 conduct thus acting like a SPDT switch to connect the capacitor *C* with the first battery BAT1 and the capacitor charges or discharges to the voltage of BAT1.

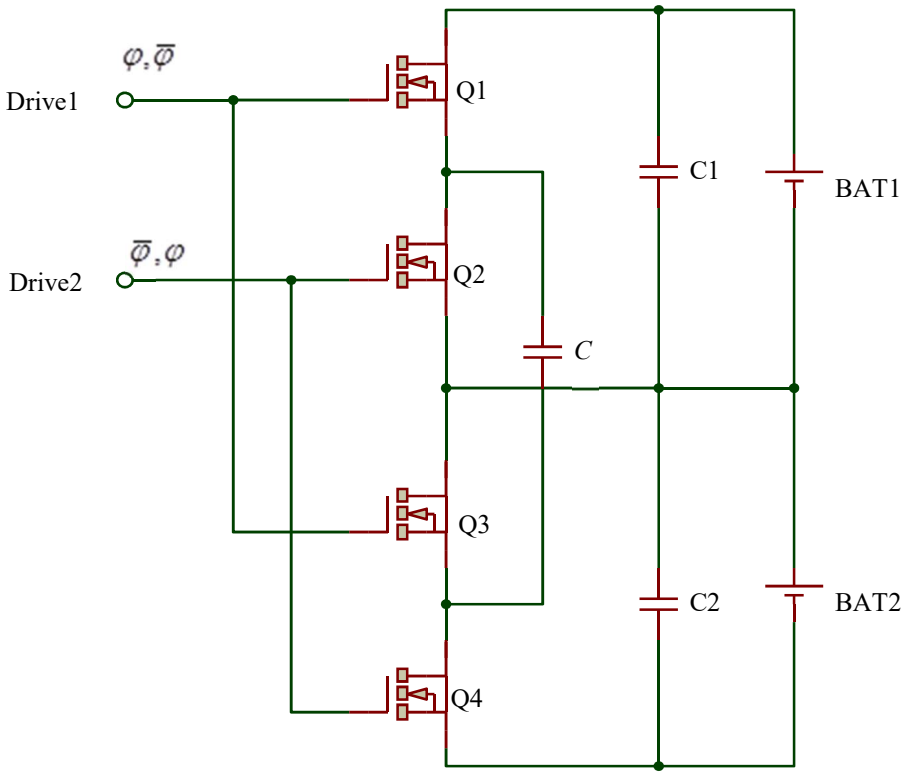


Figure 23: A basic topology of a switched capacitor (SC) battery voltage equaliser (Krein *et al.*, 2001:125-130)

When the pulse signals are alternated by feeding φ into the Drive2 and $\overline{\varphi}$ into the Drive1, the transistors Q2 and Q4 become active thus connecting the capacitor *C* with the battery BAT2. These processes are shown in figures 24a and 24b.

Through this process, the equalisation capacitor is shuttled between the two batteries continuously until BAT1 and BAT2 equalise. The capacitors C1 and C2 are filtering capacitors connected to decouple the inductance across BAT1 and BAT2 respectively for a faster equalisation time.

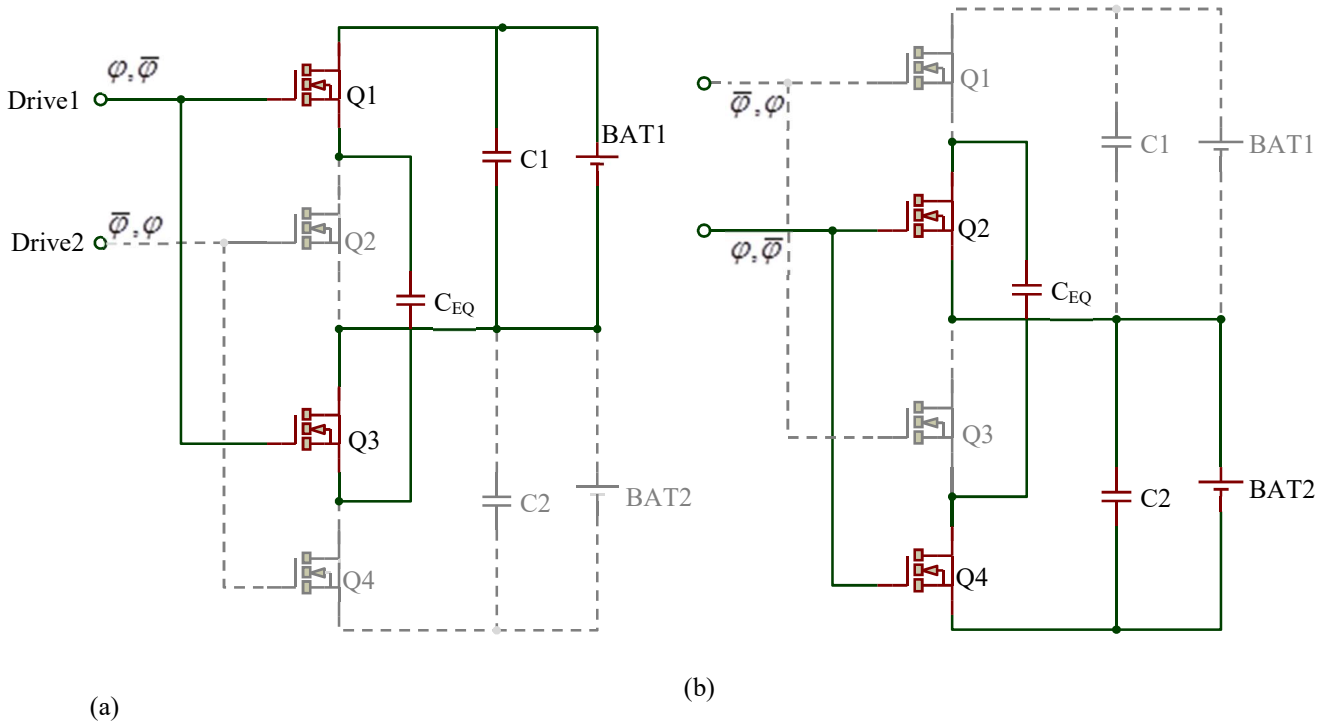


Figure 24: Pulse signal controlled MOSFETs acting as switches for capacitor shuttling in a battery string. a) High pulse signal connecting C_{EQ} with BAT1 b) High pulse signal connecting C_{EQ} with BAT2

2.10 MODELLING OF SHUTTLING CAPACITOR EQUIVALENT RESISTANCE DURING CHARGE EQUALISATION

When an equalisation capacitor (C_{EQ}) is switched across a battery, it acts as a resistor in parallel across the battery during its charging and discharging. In the design of a SC charge equaliser, the determination of the equivalent resistance of a shuttling capacitor across each battery must be determined with respect to the nominal voltage of the batteries to be equalised in order to appropriate the best oscillation period for the capacitor's shuttling across the batteries. Also, this can help in the choice of the proper C_{EQ} value to be used in the design.

2.10.1 Capacitor charging

The time required for a capacitor to get charged is dependent on the capacitance of the capacitor and the equivalent series resistance between the capacitor and the voltage source V_S. The product of the series resistance R and the capacitance C of the capacitor is called the time constant τ, a

value that characterises the rate of capacitor charging and discharging in a resistor-capacitor circuit. The relationship between the τ (s), R (Ω) and C (F) is shown in the Equation 1.

$$\tau = RC \tag{1}$$

The time needed for a capacitor to be fully charged approximately to its source voltage V_S is five time constants (5τ). Due to the exponential nature of capacitor charging, 5τ can be considered close enough to fully charged that the difference becomes negligible. A typical capacitor charging curve is shown in Figure 25.

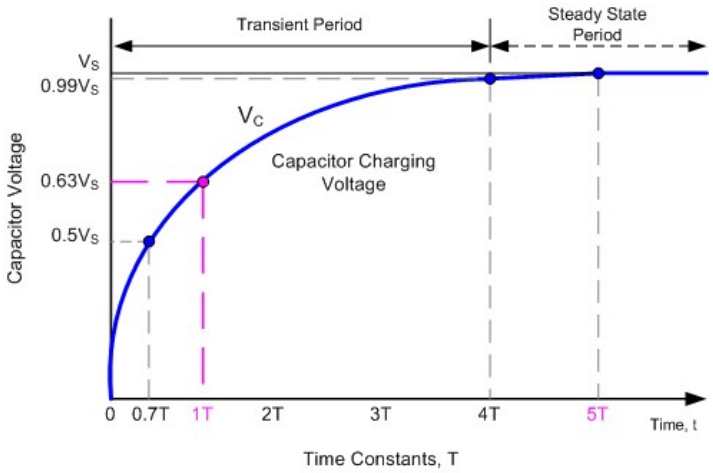


Figure 25: A typical capacitor charging curve

From Figure 26, the capacitor voltage V_C increases with respect to its source voltage V_S exponentially and this can be related using the Equation 2.

$$V_C = V_S\left(1 - e^{\frac{-t}{RC}}\right) \tag{2}$$

When a capacitor is fully charged, that is at t = 5RC, the exponential term of the Equation 2 becomes very small in value close to zero (0.0067). The capacitor's voltage, therefore, becomes approximately equal to the source voltage. Otherwise, the capacitor would be charged to a fraction of the voltage source when it is rapidly switched across the voltage source at the time constant less than 5RC.

2.10.2 Capacitor discharging

In a*n* RC circuit, a capacitor discharges exponentially through a load resistance (R) connected across it as shown in Figure 26. If the initial voltage of the capacitor before discharge is V_S, the available capacitor's voltage, V_C, at any time t in the discharge period are related using the Equation 3.

$$V_C = V_S\left(e^{\frac{-t}{RC}}\right) \tag{3}$$

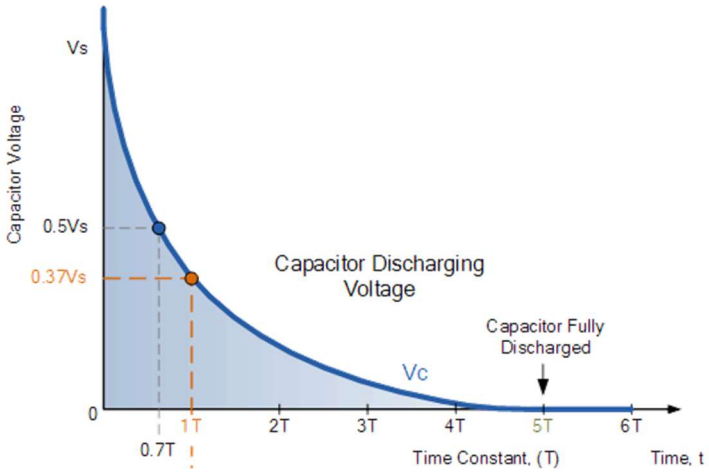


Figure 26: A typical capacitor discharging curve

Likewise, in capacitor charging, it takes 5τ for a capacitor to get approximately fully discharged to a steady state period during capacitor discharging. When t = 5τ =5RC in Equation 3, then $V_C \cong 0$.

2.10.3 Equivalent resistance modelling and analysis

The charge transfer between the equalisation capacitor and the two batteries during a charge equalisation process can be modelled by considering the charge-discharge characteristics of this capacitor during each cycle of the shuttling process. An idealised equalisation capacitor is charged during one half-cycle and discharged during the other half-cycle following exponential charge-discharge curves as described in Figure 26 and Figure 27. In a periodic steady state, the capacitor's charge, V_C alternates between two states of V_{C1} and V_{C2}, where V_{C1} and V_{C2} are capacitor's charge at the end of charge and discharge period respectively.

For a shuttling capacitor equalisation circuit, the charge-discharge process of the shuttling capacitor is usually symmetric, operating at about 50% duty cycle. Meanwhile due to the rapid shuttling period, which is mostly less than 5τ of the shuttling capacitor, the capacitor is not always fully charged or discharged during the shuttling process. Thus, the pattern of the capacitor's voltage V_C during the periodic SOC and discharge as shown in the Figure 27, would have a ripple voltage (or voltage difference) Δv which is symmetric about the mean of the two batteries voltages V_1 and V_2 (Krein *et al.*, 2001:125-130, Seeman, 2009:10-36).

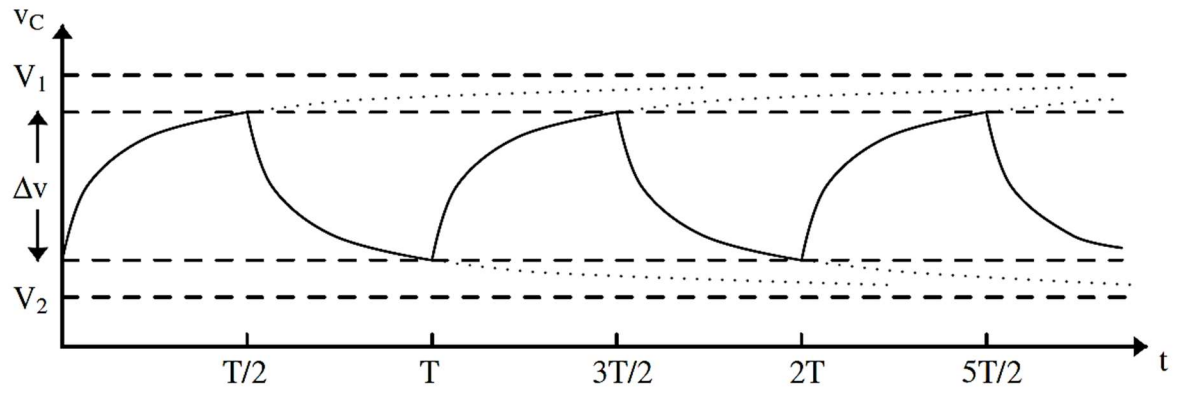


Figure 27: Capacitor voltage waveform during periodic states of charge and discharge (Seeman, 2009:10-36)

The voltage difference Δv can then be expressed as a decaying exponential equation as shown in the Equation 4 (Seeman, 2009:10-36).

$$\Delta v = \left(\Delta v + \frac{V_1 - V_2 - \Delta v}{2} \right) \left(1 - e^{-T/2RC} \right) \tag{4}$$

By simplification,

$$\Delta v \left(2 - \left(1 - e^{-T/2RC} \right) \right) = \left(V_1 - V_2 \right) \left(1 - e^{-T/2RC} \right)$$

$$\Delta v = \left(V_1 - V_2 \right) \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \tag{5}$$

T is the capacitor's switching period, which is also an inverse of the switching frequency $\left(1 / f_{sw} \right)$ Thus, Equation 5 can be represented as Equation 6 below.

$$\Delta v = (V_1 - V_2)\frac{1 - e^{-1/2RCf_{sw}}}{1 + e^{-1/2RCf_{sw}}} \tag{6}$$

a) Current flow through SC circuit during charge shuttling

The quantity of charge q stored in a capacitor is the product of capacitance C and voltage V of the capacitor. Thus, the charge gained or transferred by a shuttling capacitor during charge equalisation process between two batteries can be given as $q = C\Delta v$, where Δv is represented by Equation 6. Since the current flow through a circuit is the rate of flow of charge round the circuit q/t, the time-averaged current i flow through the SC equalisation circuit can then be given as Equation 7, where the switching frequency f_{sw} is an inverse of the shuttling period T.

$$i = \frac{q}{T} = \Delta v C f_{sw} \tag{7}$$

Alternatively, by substituting Equation 6 into Equation 7, the current can also be given as:

$$i = \frac{Cf_{sw}\left(1 - e^{-1/2RCf_{sw}}\right)}{1 + e^{-1/2RCf_{sw}}}(V_1 - V_2) \tag{8}$$

b) Equivalent series resistance of SC circuit

From Ohm's law where voltage is the product of resistance and current, the equivalent series resistance R_{eq} of a SC and other connection resistance during the charge shuttling process across two batteries of voltage difference ($V_1 - V_2$) can be represented as Equation 9, where i_c is the current flow through the capacitor. The batteries voltage difference can be represented as ($V_2 - V_1$) depending on the direction of current flow through the shuttling capacitor.

$$R_{eq} = \frac{V_1 - V_2}{i_c} \tag{9}$$

By substituting Equation 7 into 9, the expression for calculating the equivalent resistance of the switched capacitor during battery charge equalisation can then be given as Equation 10.

$$R_{eq} = \frac{V_1 - V_2}{\Delta v C f_{sw}} \tag{10}$$

Alternatively, if Equation 6 is substituted into Equation 10, the equivalent resistance can be given in Equation 11.

$$R_{eq} = \frac{1 + e^{-1/2RCf_{sw}}}{Cf_{sw}\left(1 - e^{-1/2RCf_{sw}}\right)} \tag{11}$$

c) Analysis of the equivalent resistance

The equivalent resistance in Equation 11 can be analysed in three ways for circuit parameters estimation.

- Case 1: Equivalent resistance when the switching frequency limit tends towards zero.

When the switching frequency is very low, tending towards zero, the equivalent resistance at this limit $R_{eq(\lim)}$ can be given in Equation 12 below.

$$R_{eq(\lim)} = \lim_{f_{sw} \to 0} R_{eq} = \lim_{f_{sw} \to 0} \frac{1 + e^{-1/2RCf_{sw}}}{Cf_{sw}\left(1 - e^{-1/2RCf_{sw}}\right)} = \frac{1}{Cf_{sw}} \tag{12}$$

This equation, also referred to as the slow-switching limit (SSL) output impedance (Seeman, 2009:10-36), applies when the switches and all other conductive interconnects of the circuit are assumed to be ideal, such that the currents flowing through the capacitor are impulsive and the finite resistances of the switches are neglected. In addition, it gives an idea of the inverse proportion between the switching frequency and the capacitance with respect to the output impedance. However, it cannot be used to precisely estimate the components' values in SC battery charge equaliser design operating at a higher frequency since the switching frequency may not be zero during the equalisation process.

- Case 2: Equivalent resistance at low switching frequency, such that the capacitor is completely charged, then completely discharged

A capacitor is said to be approximately *completely* charged or discharged in five time constants. Thus, when the switching period T is substituted into Equation 11, we have

$$R_{eq(T)} = \frac{1+e^{-T/2RC}}{Cf_{sw}\left(1-e^{-T/2RC}\right)} \tag{13}$$

When $T = 5\tau = 5RC$,

$$R_{eq(1)} = \frac{1+e^{-2.5}}{Cf_{sw}\left(1-e^{-2.5}\right)} \cong \frac{1.1789}{Cf_{sw}} \tag{14}$$

Equation 14 can be used to estimate the equivalent series resistance during one shuttling period at a low switching frequency that enables the capacitor to be approximately completely charged and discharged.

- Case 3: Equivalent resistance at low switching frequency such that the capacitor is not completely charged or completely discharged during the shuttling process

During rapid shuttling process, a capacitor may not be completely charged or completely discharged to the battery's voltage. Thus, the capacitor's switching period is likely to be less than five time constants, that is $T < 5\tau$. For analysis, if we assume $T = 1\tau = 1RC$, Equation 13 can thus be given as:

$$R_{eq(T)} = \frac{1+e^{-1/2}}{Cf_{sw}\left(1-e^{-1/2}\right)} \cong \frac{4}{Cf_{sw}} \tag{15}$$

Although the switching period may be less than one time constant during the rapid equalisation process, the equation gives a better estimation when a capacitor is not completely charged or completely discharged during the rapid switching process. As earlier depicted in Figure 27, the capacitor's ripple voltage Δv should be less than the charge imbalance $V_1 - V_2$ during rapid shuttling process. This makes the ratio $\left(V_1 - V_2\right)/\Delta V$ greater than one in Equation 10, supporting Equation 15.

2.11 EFFECT OF CURRENT RIPPLES ON BATTERY PERFORMANCE

During SC charge equalisation process, batteries are exposed to charge-discharge pulse current from the SC and this creates current ripples on them. Current ripples on batteries over a long term impact can affect their performance and degrade their capacity (Sritharan, 2012, Uddin *et al.*, 2016:142-154). The degradation, which includes capacity fade and progressive impedance rise is accelerated when the superimposed pulse current occurs at a high frequency such as in kHz range (Uddin *et al.*, 2016:142-154). Although the underlying causality for this degradation has not yet been fully harnessed in research, it has, however, been reported to have important implications on BMS performance if not properly managed (Uddin *et al.*, 2016:142-154, Huhman *et al.*, 2017:A6401-A6411). Due to this undertone, the proposed SC battery charge equaliser design in this work is designed to provide low frequency charge shuttling equalisation to the batteries. This will protect the batteries from charge imbalance, while preventing them from future accelerated capacity degradation that may occur due to high frequency SC current ripples on them.

2.12 OVERVIEW OF MOSFET SWITCHING CHARACTERISTICS

A MOSFET can be configured to act as a switch in an electronic circuit by supplying an appropriate gate-to-source voltage (V_{GS}) to it as referenced in Table 2. When a V_{GS} suitable enough to drive a MOSFET into saturation mode is supplied, the drain-to-source terminals of the MOSFET conduct thus acting like a closed switch by allowing a flow of current through them. Otherwise, when the V_{GS} is not enough to drive the MOSFET into saturation mode, the drain-to-source terminals become disconnected thus acting as an open switch. Also in this mode, it functions in its linear region as a voltage-controlled amplifier. For circuit design purpose, an appropriate V_{GS} range required for gate drive of any MOSFET type could be found in their manufacturer datasheet.

Table 2: MOSFETs characteristics with respect to V_{GS} input

MOSFET Type	*V_{GS} (0V)*	*V_{GS} (+ve)*	*V_{GS} (-ve)*
N-channel enhancement	OFF	ON	OFF
N-channel depletion	ON	ON	OFF
P-channel enhancement	OFF	OFF	ON
P-channel depletion	ON	OFF	ON

Meanwhile, a power MOSFET has some advantages over bipolar junction transistors (BJTs) — another category of transistors that can also be used for switching applications (Rashid, 2010:50-52). First, unlike the BJTs, which require base current control for current to flow in the emitter, the power MOSFET devices are voltage-controlled devices and this makes them demand only a small amount of input current, thus requiring less drive power than BJTs.

In addition, MOSFET devices, unlike BJTs, can allow current to be shared with other MOSFETs in parallel due to its negative feedback thermal characteristics. That is, a MOSFETs $R_{DS(on)}$ increases with temperature. If a MOSFET in parallel with another has a lower intrinsic resistance, more current flows through it, heating it up more. Due to the negative feedback thermal characteristics, the MOSFETs $R_{DS(on)}$ will increase at the higher temperature, reducing the current flowing through it and cooling it down. Furthermore, MOSFETs implementation as a switch is essential when a more efficient and rapid switching frequency is required. The schematic diagrams of an implementation of a typical MOSFET device as a switch in a circuit are shown in the Figure 28a and 28b.

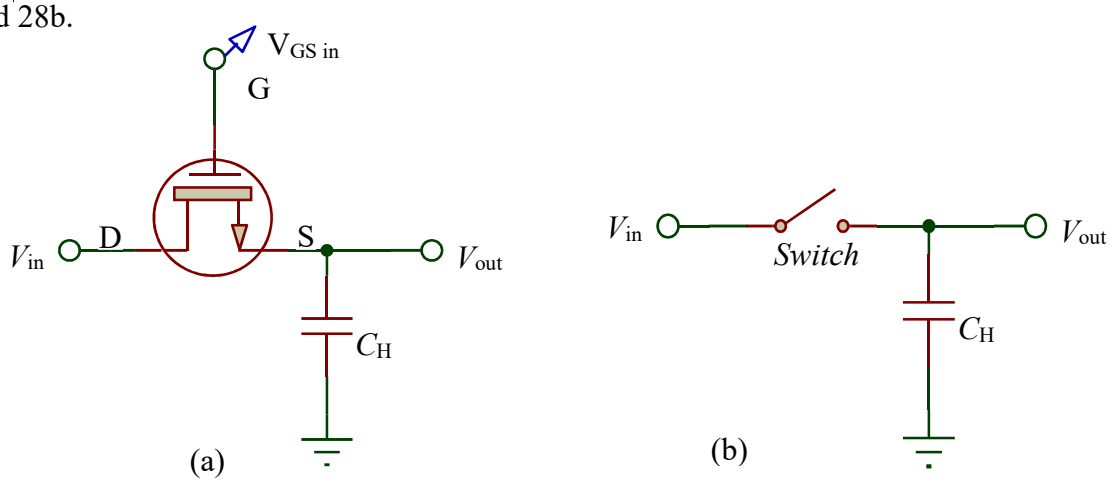


Figure 28: Typical MOSFETs implementation as a switch a) schematic circuit b) equivalent circuit with a switch (Agrawal, 2014:1531)

In Figure 28, V_{in} and V_{out} represent the input and output voltage respectively and C_H is the load referenced to the ground. When a MOSFET is in the on-state, that is the triode region when the drain-to-source terminals conduct, the drain-to-source terminals have some finite resistance known as the $R_{DS(on)}$ of the transistor (Agrawal, 2014:1531, Rashid, 2010:50-52). The $R_{DS(on)}$ values of MOSFETs are usually indicated in their manufacturer datasheet. The current flowing through

the gate of a MOSFET during this on-state can thus be calculated using the relation in Equation 16 (Rashid, 2010:50-52):

$$R_{DS(on)} = \frac{\partial v_{DS}}{\partial i_D}\bigg|_{V_{GS}=Constant} \tag{16}$$

2.12.1 MOSFET high side gate drive configuration

To drive a MOSFET into conduction, the gate terminal must be made positive with respect to its source terminal. The gate drive voltage of a MOSFET, however, differs with respect to its configurations. A MOSFET configured on the high-side has a load connection between its source terminal and the grounds. This means the current travels from the supply through the MOSFET to the load and then to ground. The MOSFET connected in this configuration is otherwise referred to as a floating MOSFET, which requires a floating charge supply to drive it into conduction. The low side configured MOSFET, meanwhile, does not consist of any load between its source terminal and the ground. This MOSFET configuration does not require a floating supply to drive it into conduction, as the specified gate-drive voltage of the MOSFET is enough to drive it into conduction.

For a high side configured MOSFET having its source terminal floating in a circuit, there are three common methods of generating the floating DC supply to drive it; these are isolated supply, charge-pump supply and bootstrap supply (Rashid, 2010:551-558). The isolated supply generates a floating supply of a continuous large amount of current with the use of a high frequency isolated DC/DC converter, which is fed from an existing DC supply. This converter has an inherent isolation transformer which usually makes them very bulky (Rashid, 2010:551-558). The charge-pump supply is a method that superimposes the voltage of one supply onto another, normally used for boost voltage generation over the main high voltage supply. This method, however, has a high cost of implementation and complexity in design (Rashid, 2010:551-558).

The bootstrap supply is the most common technique for generating floating supply voltage. This method is simple to implement with the use of only one diode and a supply storage capacitor. The typical applications of this method include variable motor drives and often in high side MOSFET driver configurations (Rashid, 2010:551-558).

A typical schematic bootstrap supply circuit for floating supply is shown in Figure 29.

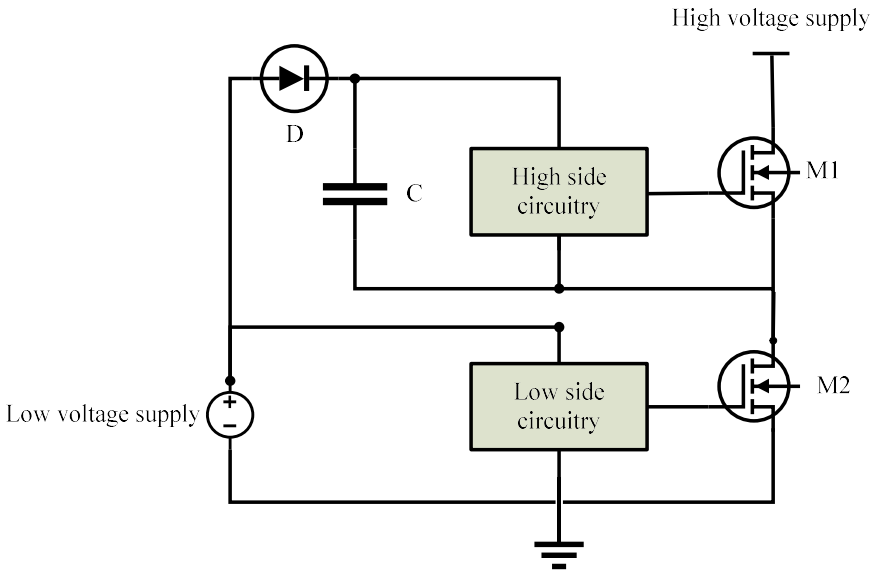


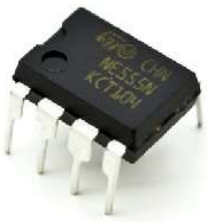
Figure 29: Bootstrap technique for high side MOSFET floating supply (Rashid, 2010:551-558)

When the low side MOSFET M2 is on, the bootstrap diode D conducts and charges the storage capacitor C to the approximate voltage on the low voltage supply. Thus when M2 is off, D is reverse-biased and the high side circuitry is powered from the charge on C (Rashid, 2010:551-558). This makes the gate-source potential of the high side MOSFET M1 to be high enough to overcome the potential difference relative to the ground.

2.13 PULSE SIGNAL FROM 555 TIMER ASTABLE MULTIVIBRATOR

Astable multivibrator is a circuit which uses 555 timer IC to generate a continuous pulse signal that oscillates continuously between two unstable states without the aid of external triggering, forming a square wave at a specific mark-to-space ratio. A typical 555 timer IC, NE555 is shown in Figure 30 alongside its pins layout.

(a)



(b)

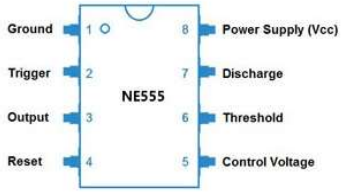


Figure 30: NE555 timer IC (a) magnified image view (b) pin configurations

2.13.1 50% duty cycle astable multivibrator and limitation

The normal astable configuration of NE555 timer IC can only strictly produce a duty cycle greater than 50%. Meanwhile in a special configuration mode as shown in one of the application circuits of NE555 datasheet provided in Annexure A of this report, the astable can be designed to produce 50% duty cycle output when some circuit conditions are taken into consideration.

In the utilisation of a stable multivibrator for SC charge equaliser design as implemented in this work, the choice of 50% duty cycle astable would have been a better option as this would enable the equalisation capacitor to be switched between the two batteries at an equal ratio. However, when the purpose of the output pulse of the astable is to drive some device such as a motor, the 50% duty cycle design of the astable will introduce some limitations, which can hinder this purpose.

First, the design assumes that the output of the astable changes between 0V and Vcc, but in practice the actual output voltage of this astable configuration depends to some extent on the load placed on the output. It is common, for example, that in an astable with a 12.0 V supply the output may change between 0 V and just a little over 11.0 V, but when different load resistances are introduced, the difference between Vcc and output voltage may vary. Also, under load, the circuit surprisingly may not always produce exactly 50% duty cycle (Coates, 2018). This is because the trigger points at which the NE555 IC switches its output are a fixed proportion of Vcc because they are supplied from the three internal resistors between +Vcc and 0V, but the rate at which the timing capacitor in this design charges now depends, not on Vcc as in the basic design, but on the output voltage. Therefore, differences in timing can occur because the voltages at the output pin 3 and at Vcc are not the same, this can affect both the frequency and mark to space ratio (Coates, 2018).

2.13.2 Basic configuration design of NE555 timer astable multivibrator

According to the datasheet information of this IC as provided in Annexure A, the basic configuration of NE555 IC is shown in Figure 31. From this configuration, the oscillation frequency and the duty cycle of the generated pulse signal output are both accurately controlled with two external resistors R1, R2 and one capacitor C1 while the periodic oscillation between high and low pulse states of the IC during operation can be calculated using the Equation 17 and 18.

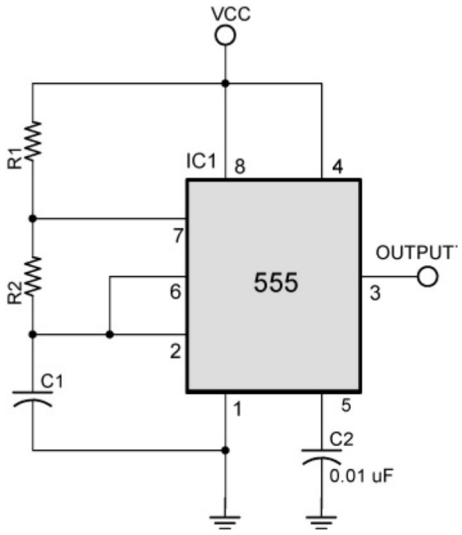


Figure 31: NE555 timer IC basic circuit configuration

$$t1 = 0.693(R1 + R2) * C1 \tag{17}$$

$$t2 = 0.693(R2) * C1 \tag{18}$$

Where $t1$ is the high state period while $t2$ is the low state period. Both $t1$ and $t2$ are measured in seconds. The period T taken for one complete oscillation is the sum of $t1$ and $t2$.

- **Frequency calculation:** Since a frequency of oscillation is a reciprocal of the period T as given in Equation 19a, the output frequency f of oscillation of NE555 astable multivibrator circuit can then be calculated using the Equation 19b.

$$f = \frac{1}{T} \tag{19a}$$

$$f = \frac{1}{t1 + t2} \tag{19b}$$

By substituting the equations 17 and 18 into Equation 19b, the frequency f of the oscillation can be given as shown in the Equation 20 below.

$$f = \frac{1.44}{(R1 + 2R2)C1} \tag{20}$$

Where:

$R1$ ≡ resistance of R1 *(*measured in *Ohms)*

$R2$ ≡ resistance of R2 *(*measured in *Ohms)*

$C1$ ≡ capacitance of C1 (measured in *Farads*)

And other terms retain their usual meaning as earlier described.

- **Duty cycle calculation:** The duty cycle is the percentage ratio of each pulse width ($t1$ or $t2$) to the period T. The duty cycle of a pulse width $t1$ is given as Equation 21.

$$\left(\frac{t1}{T}\right)100\%$$

or,

$$\left(\frac{R1 + R2}{R1 + 2R2}\right)100\% \tag{21}$$

While the duty cycle of the alternated pulse with $t2$ is given as Equation 22.

$$\left(\frac{t2}{T}\right)100\ \%$$

or,

$$\left(\frac{R2}{R1 + 2R2}\right)100\% \tag{22}$$

2.14 THE OPTO-COUPLER

The opto-coupler, otherwise known as the opto-isolator, is a device used to provide level shifting for MOSFET gate drivers and/or galvanic isolation for circuit parts that require an isolated ground from the main power supply in the complete circuit (Waaben, 1975:30-31). An opto-coupler is an integrated circuit device that contains a light-emitting diode (LED) and a photo-sensor such as a photo-resistor, a photo-diode or a photo-transistor. A schematic diagram of an opto-coupler is shown in Figure 32 (Mohan & Undeland, 2007).

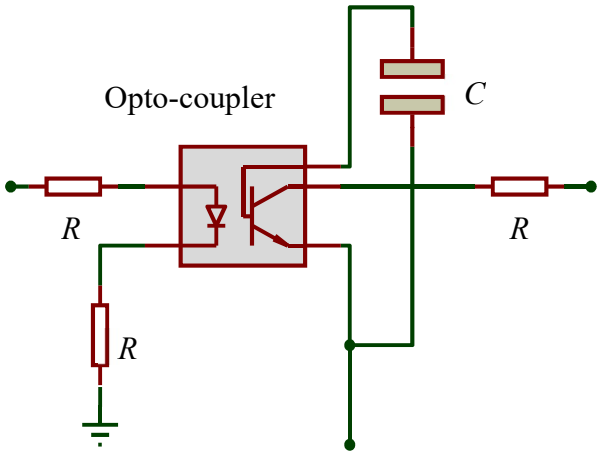


Figure 32: A schematic diagram of an opto-coupler (Mohan & Undeland, 2007)

The purpose of an opto-coupler is to transfer signals from one circuit to another, yet keeping the circuits galvanically isolated. However, one of the limitations of an opto-coupler is that it requires a separate floating supply at the receiving end of the gate driver interface (Mohan & Undeland, 2007). Also it is susceptible to noise and fast voltage transitions, which are common in MOSFET gate drive circuits (Bhattacharya & Pang, 1994). In some applications, the collector terminal of an opto-coupler is usually connected to the ground via a very high resistance in order to reduce the noise. The opto-coupler provides a wide range of optical isolation voltages up to 5 kV, this makes it more useful as most semiconductors' breakdown voltage is usually lower than this value (Khan, 2007).

2.15 VOLTAGE REGULATOR

A voltage regulator is designed to automatically maintain a constant voltage level from an input range of voltage supply, using a voltage regulator IC. The LM78XX series of three-terminal fixed

positive regulator ICs are the common type of ICs usually implemented for the regulation of DC voltage output from a range of DC voltage supply.

The LM78XX series consists of LM7805, LM7806, LM7808, LM7809, LM7810, LM7812, LM7815 and LM7824 which can be configured to supply the DC voltage of 5 V, 6 V, 8 V, 9 V, 10 V 12 V, 15 V, 18 V and 24 V respectively in the format of Figure 33.

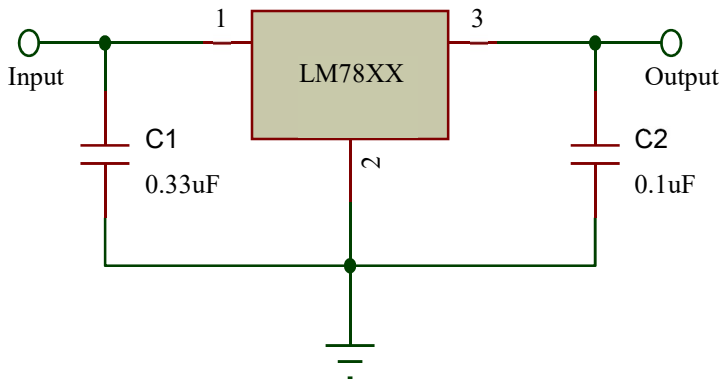


Figure 33: Schematic diagram of voltage regulator circuit using LM78XX IC

More information about their configuration setup for a regulated DC voltage output can be found from their datasheet as included in Annexure B.

2.16 RELATED RESEARCH WORKS

Different strategies to the design of battery charge equalisers or management systems in recent times as proposed by different authors, are mostly related to cell-to-cell balancing of battery technologies such as lithium ion or nickel cadmium whose cells can be physically connected in series to the desired output voltage. Such design structures pose restraints when they are to be implemented on other battery types whose cells are not exposed. In related research work, Ouyang *et al.* (2018) proposed a cell-to-cell balancing of lithium ion battery pack by utilising a bidirectional modified Ćuk converter as the cell equalising circuits (Ouyang *et al.*, 2018:350-360). However, this system, although efficient for cell-to-cell charge equalisation, requires *n-1* equalisers for *n* number of cells, which can incur more cost. This proposed design and other related design strategies may not be applicable to sealed battery types such as valve regulated lead acid batteries which are still commonly used in stand-alone photovoltaic applications and UPS (Baronti *et al.*, 2013:1139-1147, Zahran, 2007, Wang *et al.*, 2015:36-42).

For sealed battery types such as lead acid, the design strategies have been both of a novel approach (Moo *et al.*, 2003:704-710, Krein *et al.*, 2001:125-130, West & Krein, 2000:439-446, Peiying Li, 2011:141-144) and few implementations. In a related practical design, Yarlagadda presented in his work on "battery management system using an active charge equalisation technique based on DC-DC converter topology", a design topology, which introduced *n* bulky circuit to equalise *n* number of lead acid batteries (Yarlagadda, 2011:1-124). The topology could amount to an increased cost of implementation due to multiple circuits required for the equalisation. More so, the design was tested and applicable to 6 V rated lead acid batteries only, which may restrict the implementation of the design on batteries with higher DC voltage, such as batteries used in stand-alone photovoltaic applications.

However, a BMS design which can be applicable to different batteries used in stand-alone photovoltaic applications as proposed in this work, has not been fully presented or addressed in most related works. The proposed BMS introduces a design of low frequency-controlled SC active charge equaliser, which can be applicable to common battery types used in stand-alone photovoltaic application, such as lithium ion or lead acid.

2.17 SUMMARY

This chapter gives a broad overview and review of the literature that explains the theoretical basis and systematic practical approach of the design structure, components and requirements necessary for the implementation of the design of a BMS in a photovoltaic application. In the review, information on batteries, BMS, photovoltaic applications and methods of charge equalisation with a special focus on the SC technique were considered, while the components that make up the charge equaliser circuit design for this research were also discussed with their topologies.

The next chapter will focus on the practical design of the BMS using a selected topology of the SC active charge equalisation technique.

CHAPTER 3: DESIGN OF UNIVERSAL BATTERY MANAGEMENT SYSTEM (BMS)

In the previous chapter, an overview of the literature that explains the theoretical basis and systematic practical approach of the design structure, components and requirements necessary for the implementation of a universal battery management system (BMS) design in a photovoltaic application was considered. In this chapter, a practical BMS design using a selected topology of SC active charge equalisation technique is presented. Based on the design parameters, the choice of the SC value was estimated and optimised for implementation. The photovoltaic (PV) supply, as regulated by solar charge controller, was utilised to power this design and a necessary simulation on the design is done and reported to ascertain its practicality.

3.1 INTRODUCTION

In a typical BMS design, the charge equalisation circuit and technique imbibed are crucial among other implementation parameters (Glavin & Hurley, 2006:79-83, Chatzakis *et al.*, 2003:990-999). In this work, an active charge equaliser circuit was designed based on SC topology. The design equalises the charge imbalance among batteries in a series string in a modular approach. The choice of SC technique is due to its capability of being integrated into a modular design, also it is the most effective method that can be applied to batteries, both during charging and discharging (Cao *et al.*, 2008:1-6). Based on the parameters estimation, the SC circuit was designed using a high capacitance and relatively low switching frequency supplied from an astable multivibrator. The block diagram of the design process is shown in Figure 34.

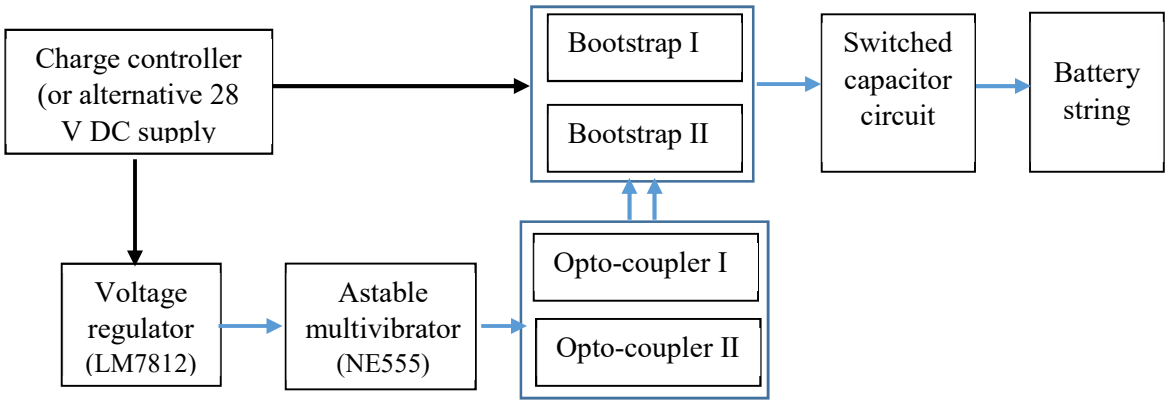


Figure 34: Block diagram of the SC equaliser design process

The complete charge equalisation design for the proposed universal BMS is further discussed in this chapter vis-a-vis detailed circuitry analyses.

3.2 HARDWARE DESIGN OF THE SWITCHED CAPACITOR (SC) BATTERY CHARGE EQUALISER

In the design, an input 28 V DC was supplied from PV panels through a solar charge controller to enable the incorporation of the design into BMS in stand-alone photovoltaic applications, meanwhile alternative equivalent DC voltage may be supplied from other sources. The input supply was used as a floating supply to the bootstrap circuits, while also concurrently regulated to power the astable multivibrator circuit. MOSFETs string were configured to act a double pole-double throw (DPDT) switch to switch the equalisation capacitor C_{EQ} among two modular batteries B_1 and B_2 in a series string. The schematic of the SC battery charge equaliser circuit is shown in Figure 35.

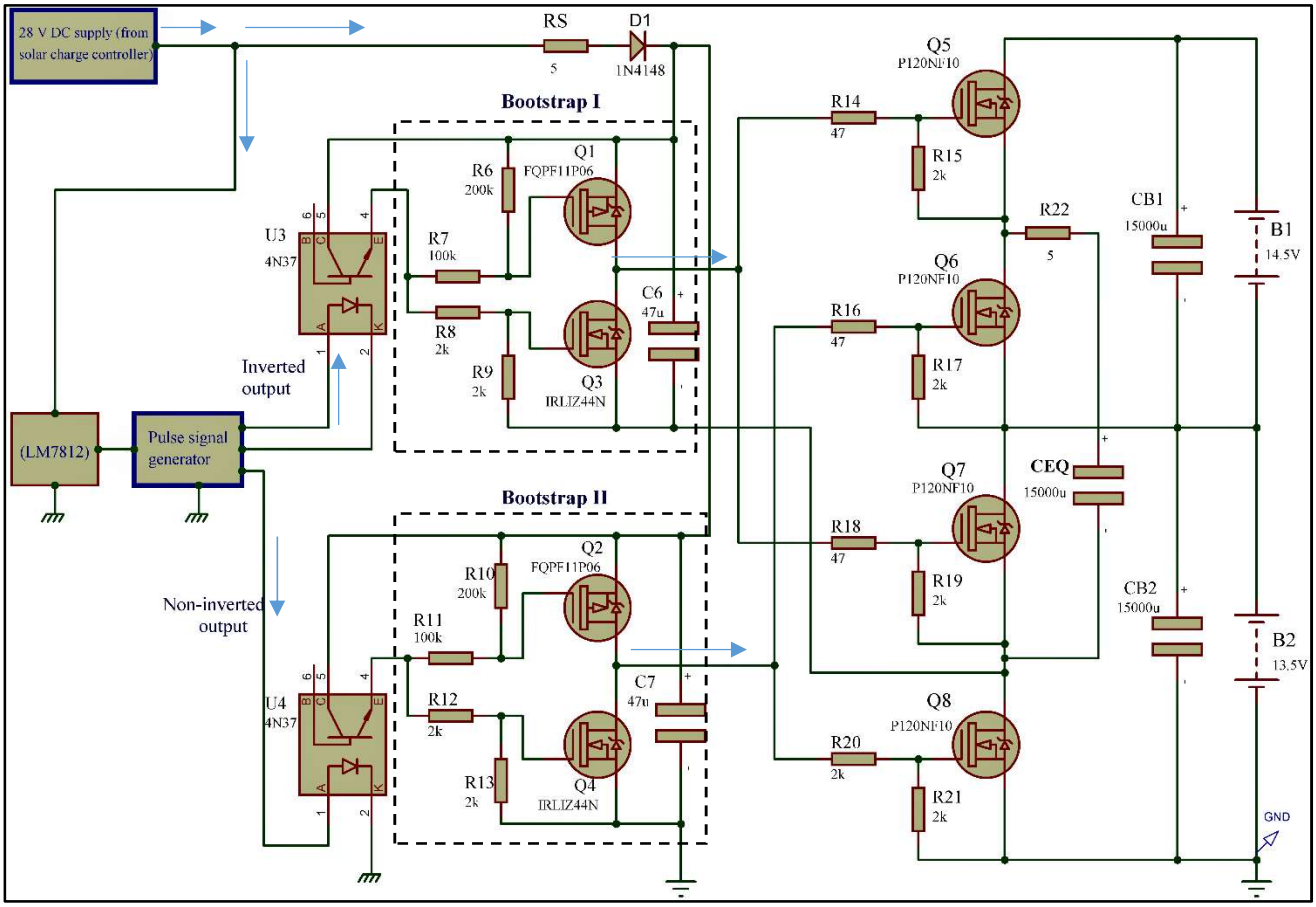


Figure 35: Schematic diagram of the designed switched capacitor equaliser circuit

3.2.1 Voltage regulator circuit

As introduced in Section 2.15, a voltage regulator supplies a regulated fixed voltage output from a wide range input voltage. In this design, LM7812 voltage regulator IC was configured to supply a regulated 12 V DC to the astable multivibrator circuit as shown in Figure 36.

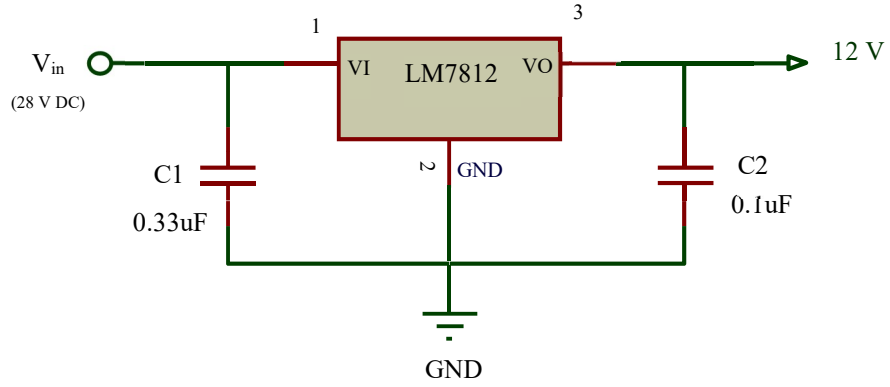


Figure 36: LM7812 voltage regulator circuit schematic diagram

The input voltage (V_{in}) was supplied from the solar charge controller DC voltage output, while the capacitors C1 and C2 respectively ensure the stability of the input and output voltage.

3.2.2 NE555 Astable multivibrator choice of design

As introduced in Section 2.13.1, an astable multivibrator circuit that produces 50% duty cycle could introduce some limitations when the purpose its output pulse voltage is to drive a motor or optocouplers as implemented in this work. Thus for the SC equaliser circuit design, the basic astable multivibrator design was implemented, giving preference to the pulse voltage output stability rather than describing the mark to space ratio of astable. Although the basic design may not give exactly 50% duty cycle, it enables more stable output pulse voltage required to sufficiently activate the opto-couplers and power the bootstrap circuits needed to oscillate the SC circuit without the pulse voltage drop. To regulate the duty cycle and have control over the output frequency, a variable resistor (VR) is introduced into the astable design accordingly. The schematic diagram of the astable multivibrator as implemented in this design is shown in Figure 37.

The input supply V_{CC} to NE555 timer IC in this design is 12 V as supplied from the regulated voltage output of the LM7812 circuit. The choice of 12 V supply to this circuit is based on the V_{CC}

voltage range of the NE555 IC which is between 9 V and 15V as indicated in its data sheet in Annexure A.

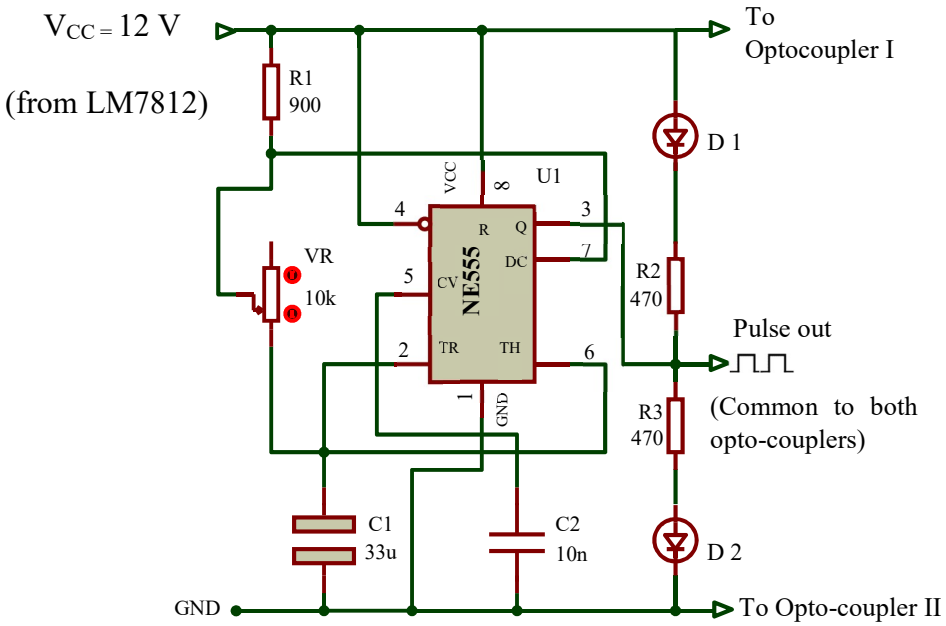


Figure 37: Schematic of the designed astable multivibrator circuit

The VR was introduced so to control or vary the output pulse signal frequency. The values for the selected resistors and capacitors were chosen based on the estimation of the desired duty cycle and pulse frequency of the oscillation as described in Section 2.13.2.

Using the selected values of R1 and C1 in Figure 37, the output pulse frequency and duty cycle can be calculated as VR changes. For example, when VR is 1 kΩ, the frequency of oscillation f according to the Equation 19 be given as:

$$f = \frac{1.44}{(900 + 2000)\,0.0000033}$$

$$f \cong 15.05\,Hz$$

Also, from Equations 20 and 21, the high period $t1$ duty cycle and low time period $t2$ duty cycle when VR is 1 kΩ can be given as follows:

$$t1 \text{ duty cycle} = \left(\frac{900+1000}{900+2000}\right)100\% \cong 65.5\ \%$$

$$t2 \text{ duty cycle} = \left(\frac{1000}{900+2000}\right)100\% \cong 34.5\ \%$$

These calculated values can be varied as VR changes while keeping other components' values constant. The corresponding variation between the frequency and duty cycles as VR varies between 0 and 10 kΩ are shown in Table 3. The maximum frequency used for the experimental purpose in this work is 40 Hz; as shown in Table 3, t2 duty cycle would approach zero limit at a further frequency rise.

Table 3: Duty cycles and frequency estimation for the designed astable multivibrator circuit

Sample	C1 (*μF)*	R1 (Ω)	VR (kΩ)	*t*1 duty cycle (%)	*t*2 duty cycle (%)	Pulse Frequency *f* (Hz)	Period T (secs)
1	33	900	0	100	0	48.48485	0.020625
2	33	900	1	65.51724	34.48276	15.04702	0.066458
3	33	900	2	59.18367	40.81633	8.90538	0.112292
4	33	900	3	56.52174	43.47826	6.324111	0.158125
5	33	900	4	55.05618	44.94382	4.902962	0.203958
6	33	900	5	54.12844	45.87156	4.003336	0.249792
7	33	900	6	53.48837	46.51163	3.382664	0.295625
8	33	900	7	53.02013	46.97987	2.928615	0.341458
9	33	900	8	52.66272	47.33728	2.582033	0.387292
10	33	900	9	52.38095	47.61905	2.308802	0.433125
11	33	900	10	52.15311	47.84689	2.087864	0.478958

A chart of this phenomenon shown in Figure 38 shows the plot of the frequency and duty cycles variations as VR varies between 0 and 10 kΩ.

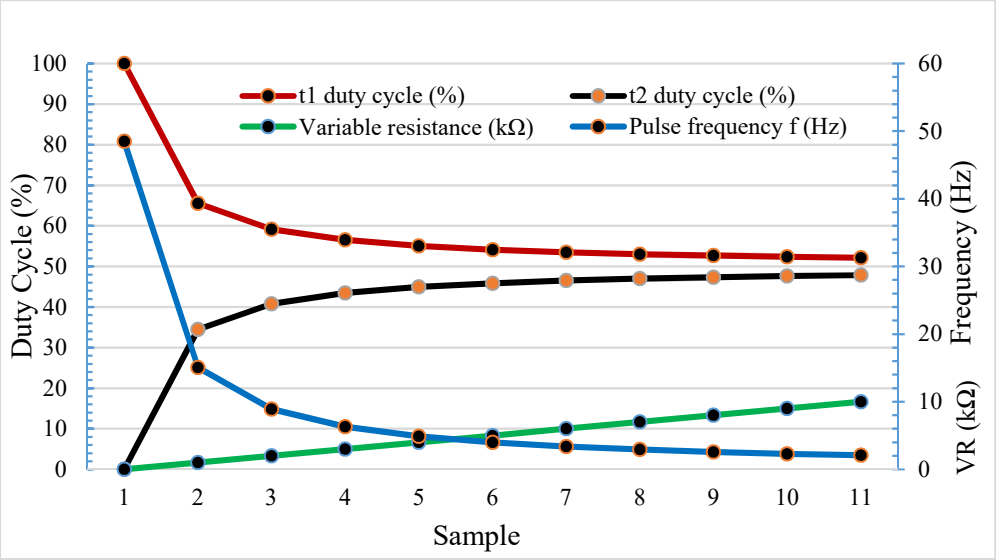


Figure 38: Relationship between duty cycles and frequency of oscillation of the designed NE555 timer circuit

In this case, the variable resistor enables a manual manipulation of the output expectations from this astable multivibrator circuit to the best of the expectations, which should be close to 50% duty cycles. From the astable multivibrator circuit in Figure 37, the frequency of the oscillation can be perceived based on the alternation speed of the LEDs as they glow. When the output pulse is high, D1 is ON while the D2 is OFF and when the pulse signal is low, the D2 glows while the D1 is OFF. The voltage required to power LED1 and LED2 of the astable multivibrator from the pulse signal output is utilised to power the opto-couplers I and II respectively. This is possible because opto-couplers contain embedded LEDs which must be triggered on or off for them to function.

3.2.3 Opto-coupler circuit

Opto-couplers were introduced to this circuit in order to provide optical isolation to the MOSFET pairs, while alternating the shuttling capacitor among the batteries. The optical isolation enables the MOSFET pairs to share a common ground (GND) interchangeably to avoid bridging the batteries. The two opto-couplers introduced in this design (model 4N37) were interchangeably driven by the pulse signal outputs from the astable multivibrator circuit. The choice of 4N37 was due to some of its unique features such as the ability to interface with common logic families while providing voltage isolation up to 5000 V_{RMS}. It can be used in applications that require a logic ground isolation and switch mode power supply feedback Also, it allows easy configuration

method. The datasheet of this IC is included in Annexure C for other details. The schematic analysis of these opto-couplers together with the bootstraps charge supply and the SC implementations for this design are shown in Figure 39 and Figure 40.

3.2.4 MOSFETs' V_{GSS} requirements and bootstrap charge circuits' implementation

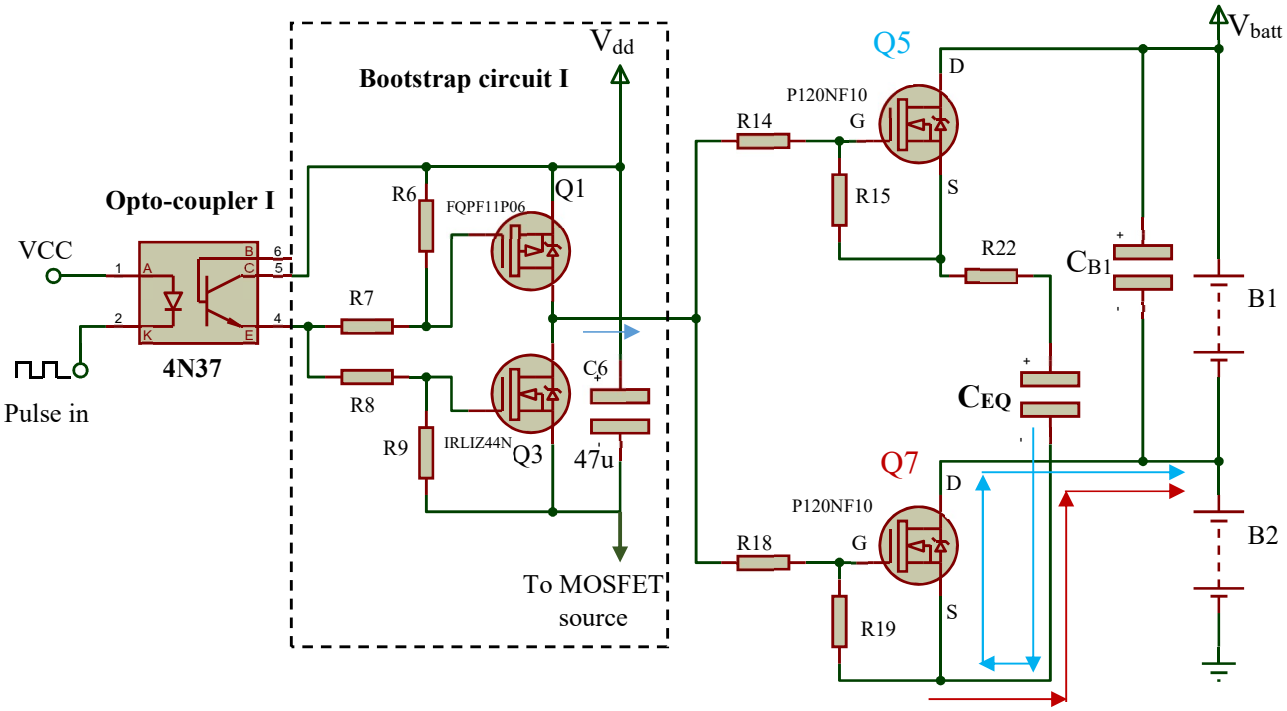


Figure 39: Schematic of opto-coupler I and bootstrap circuit I implementation for switching CEQ across B1 while Q5 and Q7 are on

In Figure 39, the equalisation capacitor C_{EQ} is connected across B1 when the two N- channel MOSFETs Q5 and Q7 are turned on. When Q5 and Q7 are on, there is a flow of current through their drain (D) to source (S) terminals thus creating a closed parallel loop between the C_{EQ} and B1.

However, since Q5 and Q7 are on high side configuration, their source terminals need to overcome a potential barrier in reference to ground, thus their gate to source voltage (V_{GS}) must be higher than the potential between their source terminals and the ground for them to be turned on. The minimum gate voltage required to turn on Q5 and Q7 relative to their source terminals (V_{GSS}) can respectively be given in equations 23 and 24.

$$V_{GSS}(Q5) = V_{GS} + V_{CEQ} + V_{SD}(Q7) \quad (23)$$

$$V_{GSS}(Q7) = V_{GS} \quad (24)$$

Where V_{GS} is the nominal gate-to-source voltage required to turn a MOSFET on when the source is connected directly to the ground, usually, 8 V $\leq V_{GS} \leq$ 20 V for power MOSFETs. V_{CEQ} is the instantaneous voltage across C_{EQ} when it is switched across B1 and V_{SD} (Q7) is the forward voltage of the inbuilt zener diode across the source and the drain terminals of Q7, often less than 1.5 V for a power MOSFET. Hence, since Q5 and Q7 are connected in parallel, (with gate to gate and the source to source via a C_{EQ} load), the highest voltage of equations 1 and 2 takes the dominant voltage to drive these two MOSFETs relative to the ground.

In Figure 40, the switching of the C_{EQ} across the battery B2 is shown. In this configuration, Q6 has a high side connection while Q8 is on a low side configuration with no load between its source terminal and the ground.

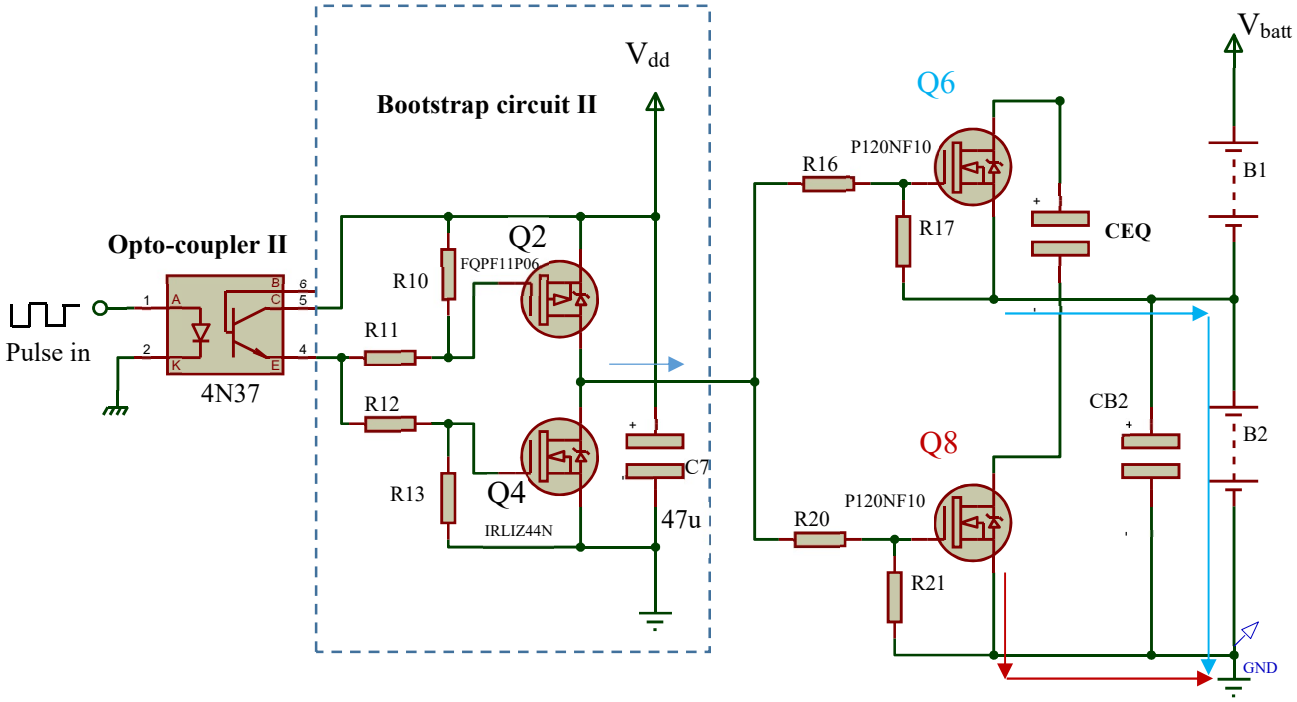


Figure 40: Schematic of opto-coupler II and bootstrap circuit II implementation for switching CEQ across B2 while Q6 and Q8 are on

In the same process as in Figure 39, the gate voltage required to drive Q6 and Q8 relative to their source terminals is expressed in the following equations 25 and 26.

$$V_{GSS}(Q6) = V_{GS} + V_{B2} \quad (25)$$

$$V_{GSS}\,(Q8) = V_{GS} \tag{26}$$

Where V_{B2} is B2 instantaneous voltage and V_{GS} follows the same meaning as in equations 23 and 24.

The resistors R14 - R21 provide voltage divider input to the gate and source terminals of the corresponding MOSFETs (Q5 – Q8) to allow the MOSFETs to operate within their V_{GS} specification limit. The voltage divider is required since the voltage output of the bootstraps exceeds the maximum V_{GS} requirement of the MOSFETs according to the datasheet. By relating the equations 23 to 26, only MOSFET Q8 would require the least V_{GS} since there is no potential barrier between its source terminal and the ground. Thus, R20 and R21 are chosen to be equal in order to provide half of the bootstrap output to drive Q8.

In figures 39 and 40, C_{B1} and C_{B2} enable the voltage stability and reduction of inductance across the batteries B1 and B2 respectively during each shuttling process. These capacitors contribute to the optimisation of the SC equaliser design as subsequently described in this chapter.

3.2.5 Bootstrap charge supply circuits for gate drive

As shown in equations 23-24, the average V_{GSS} for the MOSFETs is the sum of V_{GS} and V_{B2}, which by an average estimation is greater than or equal to 22 V. This is higher than what a MOSFET driver can supply if MOSFET drivers were to be used to drive the MOSFETs. In this case and as earlier explained in section 2.12.1 of this work, a floating supply is needed to provide the required V_{GS} supply to drive the MOSFETs.

In this design, two bootstrap circuits I and II as respectively indicated in figures 39 and 40, are designed to supply the floating voltages required to drive the MOSFET pairs. Unlike the common bootstrap supply circuits that normally consist of a series-connected NPN and PNP BJTs, a forward-biased diode from the *Vdd* reference and a capacitor, which is charged and discharged during high side gate drive of a MOSFET**,** the bootstraps in this design are modified bootstrap circuits, re-designed to suit the switching configuration process of this design. These bootstraps rather consist of P- channel MOSFET (PMOS) Q1, Q2 and N- channel MOSFET (NMOS) Q3, Q4 connected in series (Q1 source to Q3 drain and Q2 source to Q4 drain) having their floating voltage supplied from the alternative DC output of the solar charge controller used in the BMS.

The resistor RS is a current limiting resistor for the capacitors C6 and C7. The positive terminals of C6 and C7 are connected to the positive terminal of the 28 V floating supply via RS and their negative terminals are optically isolated and connected to the respective lower source terminals of the MOSFETs string that needs to be powered.

The capacitors C6 and C7 are charged when both NMOS and PMOS of their respective bootstrap are turned ON. Here, the charging time, which is five time constants, depends on the R_{DSon} of both NMOS and PMOS and the capacitance value. The stored charge in C6 or C7 is then transferred through the PMOS to the gate terminals of SC MOSFETs only when the NMOS of the bootstrap circuits is turned OFF. It is essential to note that the PMOS device in the bootstrap is an enhancement type, that is, it is always ON when its V_{GS} is 0 V or higher positive voltage. It is turned OFF when negative V_{GS} is detected. Thus, the switching of the bootstrap output mostly depends on the switching of the NMOS device used.

The opto-couplers in the bootstraps allow charge flow from their collector (C) to the emitter (E) when turned ON. The charge flow is disconnected when the opto-coupler is OFF. Thus, when the opto-coupler I is ON, Q3 conducts and the floating supply across the drain-to-source terminal of Q1 is referenced to ground, charging the capacitor C6. On the other hand, when the opto-coupler I is OFF, Q3 goes OFF as well and through the common node between Q1 source and Q3 drain, the stored charge in C6 is then supplied to drive the gate of the MOSFETs Q5 and Q7. In this way, Q5 and Q7 simultaneously alternate between the floating supply and 0 V continuously at the frequency of the pulse signal. This process is the same with the operation of opto-coupler II circuit for the switching of the MOSFETS Q6 and Q8.

The resistors R6 – R13 in the bootstrap circuits provide voltage divider to the gate-source terminals of the NMOS and PMOS devices. The selected limiting base resistances to the input of PMOS devices, (R7, R11), have higher values in order to compensate for the differences in the in-built input capacitances of the PMOS and NMOS devices so as to reduce the turn off delay time of the NMOS device. This is further buttressed in the choice of MOSFETs in the following section.

3.2.6 The choice of MOSFETs

Most P channel MOSFETs have a very low in-built input capacitance when compared to N channel types. In some cases, the input capacitance of some N channel MOSFETs can be more than 10 times that of a P channel MOSFET and this can determine the switch on or switch off delay of the MOSFETs among other factors. In bootstrap circuits, the delay can create longer time for the NMOS to switch off after the PMOS already conducts thus creating a low resistant path across the bootstrap capacitor and discharging them rapidly. When the switching frequency is very high, the bootstrap capacitor may not be charged enough to the floating supply or discharge properly to the intended load device. Thus, the choice of PMOS and NMOS device for the bootstrap circuits in this work is based on this consideration, while the MOSFETs with minimum R_{DSon}, which can also withstand high current, is considered for the SC circuit for a better performance. With this consideration, MOSFETs FQPF11P06 and IRLIZ44N, which are respectively PMOS and NMOS device, are used in the bootstrap design, while P120NF10 is selected for the SC circuit.

The FQPF11P06 MOSFET is a P-channel enhancement mode power MOSFET with low on-resistance of $175\ m\Omega$ designed for fast switching application. It has a typical input capacitance of 420 *pF* and turn-off delay of 45 ns. This MOSFET model has a capacity to withstand a high-energy pulse in different model and it is recommended for high efficiency switching for power management in portable and battery-operated products. More information about this MOSFET is included in its datasheet in Annexure D of this report.

The IRLIZ44N is an N-channel power MOSFET that allows logic-level gate drive with the benefit of fast switching speed. It is designed with extremely low on-resistance of $22m\Omega$ and can be used in wide variety of applications. It has a typical input capacitance of 1700 *pF* and turn-off delay of 26 ns. Other information about this MOSFET is attached in Annexure E.

The P120NF10 is an N-channel enhancement mode power MOSFET also designed with extremely low on-resistance of $9m\Omega$ which provides a least possible resistance to the flow of current through the shuttling capacitor during the equalisation process. Also, this model can allow up to 100 V drain-to source voltage and 110 A drain current. These enable a large clearance for the MOSFETs from breakdown during charge shuttling. P120NF10 has a high typical input capacitance of 5200 *pF*, and it is more suitable for switching applications and any applications with low gate drive

requirements. Further details about this MOSFET model are included in its datasheet as attached in Annexure F of this report.

3.2.7 Shoot-through mitigation in the design configuration

In a situation when all the MOSFETs Q5 – Q8 is ON for a brief period, there can be a shoot-through in the SC circuit, causing the short-circuiting of the batteries and the capacitors. This situation may be caused if the two bootstraps supply the same output at the same time or if there is no sufficient deadtime between the switching states of the shuttling capacitor among the batteries.

- **Bootstrap control:** Shoot-through may occur when any or all the MOSFETs in the bootstraps breakdown during operation, especially when operated outside their specification limits, thereby sending wrong signals to the SC circuit, which may inadvertently bridge it. A high shuttling frequency during operation could increase the reactance in capacitors C6 and C7 thereby allowing an increase of current flow through the bootstrap MOSFETs that may lead to their increased temperature beyond their design limits. To mitigate this, the bootstrap circuits and concurrently the entire SC equalisation circuit, are operated on low switching frequency sufficient for the charge equalisation while less than the range of AC frequency that can cause an increased reactance in the capacitors. In addition, voltage divider resistors were introduced to the bootstraps MOSFETs to allow them to operate within their V_{GS} specification limits. The resistors R6, R7, R10, R11 by calculation and in simulation, divide the floating supply voltage and supply its two-third value to Q1 and Q2, while the resistors R8, R9, R12, R13 divide the floating supply voltage and supply the exact half to Q3 and Q4.

- **Deadtime control:** During rapid shuttling process at high frequency, a SC experiences ripple voltage while equalising charges among batteries. The ripple voltage may allow current flow through the battery opposite terminals and cause a shoot-though which can bridge the system. To mitigate this, a deadtime between the switching states may be introduced (Baughman & Ferdowsi, 2008:2277-2285). A SCs deadtime implies that the capacitor's switching time length is shorter than the switching frequency. One method of introducing the deadtime is to avoid shuttling the SC directly across the batteries during each switching cycle. When other capacitor tiers are introduced, charge transport from battery to battery per switching cycle is done through the capacitor tiers

thereby introducing a slight and consistent deadtime between the SC and the batteries. In this design, capacitors CB_1 and CB_2, which help reduce the inductance across batteries B_1 and B_2 respectively also serve as different tiers through which charge is transported from the SC to the batteries. Their charging and discharging process during each shuttling cycle enable a slight deadtime between the SC and the batteries.

- **Battery terminal control:** The connections between the circuit and battery terminals are bypassed with switches, which trip off to protect them when a short circuit is detected in the system. Also due to MOSFETs turn on delays, which vary during operation, the equalisation circuit is first enabled for a few seconds to allow all the MOSFETs conduct before connecting the batteries via their respective switches in order to allow an easy flow of the switching process.

3.3 DESIGN PARAMETERS ESTIMATION

In the design of SC battery charge equaliser, the following design parameters are mostly considered, namely the equivalent resistance of the switches and other series resistance in the circuit, the switching frequency, the equalisation capacitor's value and the expected charge imbalance to be equalised. When a pulse current is applied to a battery at a high frequency, the battery respectively experiences a step response (Alexander & Sadiku, 2000:273-279) and increased cell impedance. This could affect the battery's SOH and may reduce the design efficiency of a SC equaliser due to increased resistance in the circuit. Thus, in this work, a low switching frequency was adopted in the design parameters to shuttle a high capacitance value capacitor across battery strings.

3.3.1 Resistance selection

A low resistance value of 5Ω is introduced in series with the equalisation capacitor through which its charging and discharging can be referenced, also this limits the current flow through the circuit. A lower or higher series resistance may be used with respect to the designer's choice of desired current flow through the circuit. Other source of series resistance to the circuit is from the MOSFETs R_{DSon}. Two N-channel MOSFETs having $R_{DS\,on}$ of $9m\Omega$ each act as a DPDT switch connecting the capacitor across each battery during each shuttling cycle. Thus, during each

shuttling process, the equivalent series resistance (R_{eq}) of approximately 5.018Ω is used for analysis, assuming the internal resistances of the batteries are not considered.

3.3.2 Frequency selection

A low switching frequency for the SC equaliser circuit is supplied by an astable multivibrator whose maximum output frequency is $50\ Hz$. The astable multivibrator is not operated at this limit due to the consideration of duty cycle balance during the switching process of the design. Thus, it is regulated to the desired frequency using the variable resistor in the astable design to give an output in the range of $35-40Hz$. For reference, a low switching frequency of $40Hz$ was used in this work for analysis and estimation of other design parameters.

3.3.3 Capacitor's selection

Due to rapid shuttling process the equalisation capacitor may not be completely charged or discharged during each shuttling cycle, thus, Equation 15 is used to determine the capacitor's estimated value.

$$5.018 \cong \frac{4}{40C}$$

This gives an approximated capacitor value of $0.02F$ which falls in supercapacitor range. However, a $20000\ \mu F$ high capacitance electrolytic capacitor may be used, or lower capacitance electrolytic capacitors connected in parallel to yield an equivalent value. In this design, an estimated $20000\ \mu F$ capacitance is suitable for the SC equaliser design, however, after the optimisation of the design, a choice of $15000\ \mu F$ was subsequently adopted based on the optimisation conditions as later discussed in Section 3.5.

3.3.4 Projected charge imbalance (V_1-V_2) to be equalised

The SC charge equaliser is designed to be applicable to two 12 V rated batteries per time, connected in series. A maximum voltage difference or charge imbalance of 1 V for each battery pair is projected for estimation of the design parameters. So, for the circuit's simulation or further

calculation of the design parameters, the voltages of battery 1 (V_1) and battery 2 (V_2) are selected to be 14.5 V and 13.5 V respectively.

3.4 NODAL CURRENT THROUGH THE SWITCHED CAPACITOR (SC) IN A TYPICAL RC CIRCUIT

A SC topology shown in Figure 41a can be represented as a resistor-capacitor (RC) circuit shown in Figure 41b. The $R_{DS\,on}$ is the MOSFETs on resistance when in the saturation region.

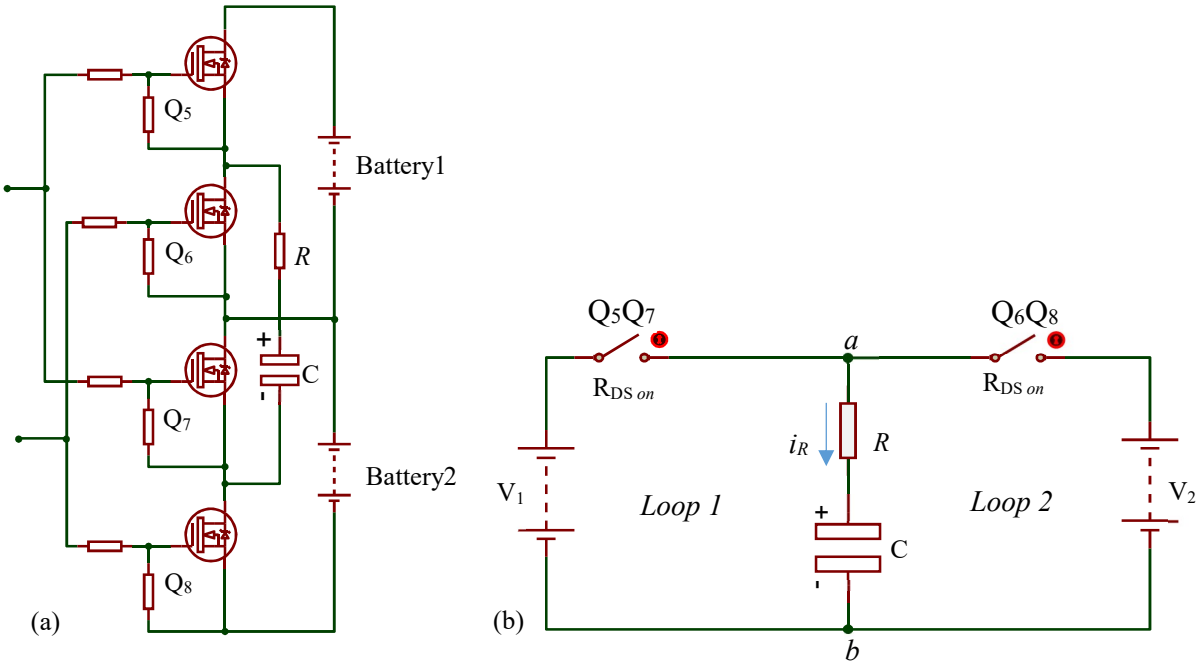


Figure 41: SC battery charge equaliser (a) Basic topology (b) Equivalent circuit for analysis

The two common techniques for circuit analysis are nodal analysis, which is based on a systematic application of Kirchhoff's current law (KCL) to determine node voltages and mesh analysis, which is based on a systematic application of Kirchhoff's voltage law (KVL) to determine node currents. With these techniques, any linear circuit can be analysed by obtaining a set of simultaneous Equations that are then solved to obtain the required value of current or voltage.

3.4.1 Basic estimation of maximum current in each battery loop without the capacitor

If the capacitor C is assumed not present in Figure 41b, the maximum current flow through the circuit can be estimated using Ohm's law. Given that R_{eq}, V_1, V_2 are respectively 5.018 Ω, 14.5 V,

13.5 V as earlier indicated in the previous session, the current flow through the loop1 i_{b1} , loop2 i_{b2} and the node ab i_R when the switches are closed can be estimated as:

$$i_{b1} = \frac{V_1}{R_{eq}} \cong \frac{14.5}{5.018} \cong 2.89\,\text{A}$$

$$i_{b2} = \frac{V_2}{R_{eq}} \cong \frac{13.5}{5.018} \cong 2.69\,\text{A}$$

Using Equation 9,

$$i_R = \frac{V_1 - V_2}{R_{eq}} \cong \frac{1}{5.018} \cong 0.20\,\text{A}$$

In this estimation, the resistance effects of the switches R_{DSon} were ignored since they do not contribute much to the estimation of i_R due to their very small value.

3.4.2 Circuit analysis of the capacitor's shuttling current during equalisation

The equalisation current, which is the current flow through a SC during rapid shuttling process, is analysed in this work by first considering the capacitor's complete step response, then using mesh analysis technique, the resultant equalisation current due to the two meshes in the circuit is calculated.

(a) The circuit's step response: The step response of a circuit is the behaviour of the circuit when a DC voltage or current source is suddenly applied to it. In a resistor-capacitor (*RC*) circuit, a sudden application of a DC voltage source can be done in two ways: First, by application of an independent DC source (Alexander & Sadiku, 2000:273-279) as illustrated in Section 2.10.1 (Equation 2). Second is by initial conditions of the capacitor where its stored energy excites the circuit and gradually get dissipated by the resistors (Alexander & Sadiku, 2000:273-279) as indicated in section 2.10.2 (Equation 3).

A SC charge equaliser is like an *RC* circuit with step response, which can be modelled as first-order differential Equations using Kirchhoff's laws. Through modelling, the complete response of a capacitor's voltage V_C at a time t > 0 is given as the sum of its natural response (stored energy)

$V_0 e^{-t/\tau}$ and forced response $V_s\left(1 - e^{-t/\tau}\right)$ from an independent source (Alexander & Sadiku, 2000:273-279). That is;

$$V_C = V_0 e^{-t/\tau} + V_s\left(1 - e^{-t/\tau}\right) \tag{27}$$

where V_0 is the initial voltage of the capacitor and V_s is DC voltage supply. If the capacitor is initially uncharged $V_0 = 0$, the complete step response is given as:

$$V_C(t) = V_s\left(1 - e^{-t/\tau}\right) \tag{28}$$

At any time, $t > 0$, the current through the capacitor is given as:

$$i(t) = C\frac{dv}{dt} = \frac{C}{\tau}V_s e^{-t/\tau} \tag{29}$$

or

$$i(t) = \frac{V_s e^{-t/\tau}}{R} \tag{30}$$

Where $R = \frac{\tau}{C}$ using the definition of time constant and *u(t)* indicates the dependence of the equation on time.

(b) Mesh analysis: The circuit in Figure 41b can be analysed as having two meshes with assigned mesh currents i_1 and i_2 in each mesh. Although these currents may be assigned to each mesh in an arbitrary direction, it is conventional to assume that they flow clockwise. In mesh 1 analysis, when Q_5 and Q_7 are in the saturation region during the SC equalisation process as shown in Figure 42, Q_6 and Q_8 are simultaneously cut off but their inherent zener diodes DQ_6 and DQ_8, having typical source-to-drain forward voltage (V_{SD}) of 1.3 V each, allow some current to flow the opposite direction through the zener diode, while closing the other mesh of the circuit. In Figure 42, the current *I* flowing through the capacitor can be given as the sum of the current in both meshes. Since i_2 flows in the opposite direction to i_1, then for $V_1 > V_2$,

$$I_C = i_1 - i_2 \tag{31}$$

For the estimation of possible maximum current flowing through the circuit or the shuttling capacitor, it will be assumed that the shuttling capacitor is initially uncharged. For the analysis,

Equation 31 is used to estimate I_C during a rapid shuttling process using the given parameter values earlier introduced: $t = 1\tau$, $R_{eq} = 5.018\ \Omega$, $V_1 = 14.5$ V and $V_2 = 13.5$ V.

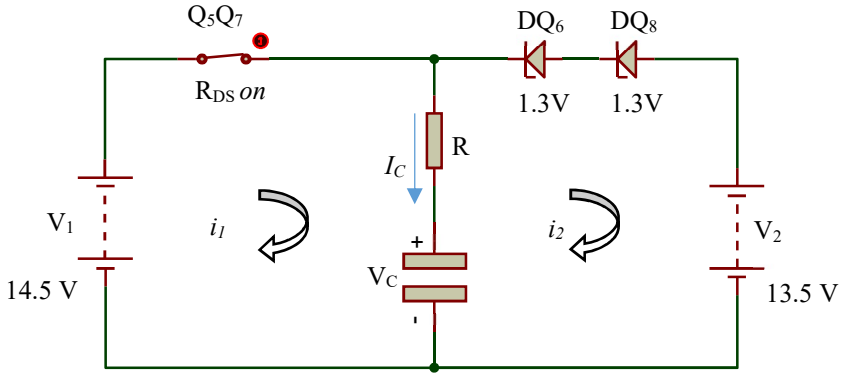


Figure 42: Mesh 1 analysis of a typical SC charge equaliser circuit

The capacitor's voltage V_C is varying and dependent on V_1 and V_2, thus Equation 30 was used for the estimation of current flow in each loop rather than using Kirchhoff's Voltage Law for each mesh.

$$i_1 = \frac{V_1 e^{-t/\tau}}{R_{eq}} = \frac{14.5 e^{-0.5}}{5.018} = 1.753\ \text{A}$$

$$i_2 = \frac{(V_2 - 1.4) e^{-t/\tau}}{R_{eq}} = \frac{12.1 e^{-0.5}}{5.018} = 1.463\ \text{A}$$

$$I_C = 1.753 - 1.463 = 0.29\ \text{A}$$

The estimated current flow through the capacitor I_C shows a positive value. This implies that the capacitor would charge up while connected to the higher voltage battery V_1.

In mesh 2 analysis, the capacitor is connected to V_2 when Q_6 and Q_8 are in the saturation region as shown in Figure 43. The MOSFETs Q_5 and Q_7 are simultaneously cut off but their inherent zener diodes DQ_5 and DQ_7, having typical source-to-drain forward voltage (V_{SD}) of 1.3 V each, allow some current to flow the opposite direction through the zener diode while closing the mesh 1 of the circuit.

Thus, during a rapid shuttling process and using the parameter values earlier introduced for mesh 1 analysis, the current flow through the capacitor I_C when connected to V_2 can be estimated as:

$$i_1 = \frac{(V_1 - 1.4)e^{-t/\tau}}{R_{eq}} = \frac{13.1e^{-0.5}}{5.018} = 1.583\,\text{A}$$

$$i_2 = \frac{V_2 e^{-t/\tau}}{R_{eq}} = \frac{13.5e^{-0.5}}{5.018} = 1.632\ \text{A}$$

$$I_C = 1.583 - 1.632 = -0.049\ \text{A}$$

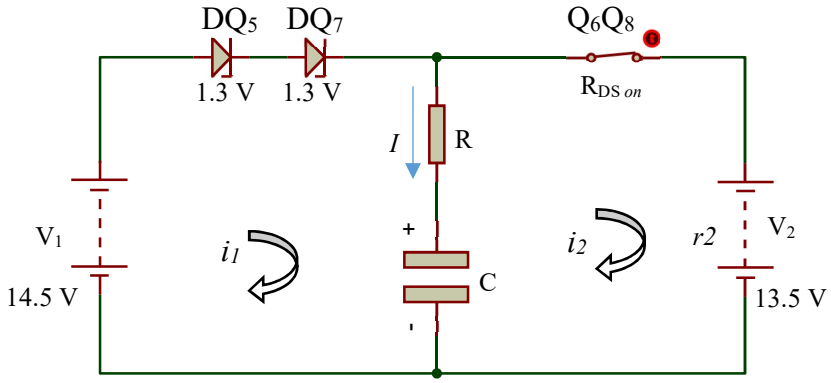


Figure 43: Mesh 2 analysis of a typical SC charge equaliser circuit

The current estimation shows negative current flowing through the capacitor at the second shuttling process, which implies that the capacitor would be subjected to discharge when connected to V_2 having a lower voltage value than V_1. This current estimation and analysis give an idea of the current flow in the SC circuit, necessary for the PCB design. However, when the difference between the two batteries is more than 2.6 V (2 x 1.3 V), huge currents will flow from the higher voltage battery to the other, thus connecting the batteries together.

3.5 OPTIMISATION OF THE DESIGN

One of the ways of optimising a design is through component sizing, that is, each component must be sized relative to each other to obtain the best performance for a given total device area or parasitic power loss. In SC equaliser, if the losses attributed to ideal capacitors and resistive switches are taken into consideration in the computation of the output resistance, the capacitor's

size or the switches resistance can be optimised to minimise this output impedance, as minimal output impedance corresponds to maximum efficiency for a given power delivered and alongside, corresponds to maximum power delivery for a given loss.

Due to the susceptibility of small capacitance value SC to ripple voltage, which may have a negative effect on the equaliser circuit such as bridging the batteries during charge transfer and affecting the overall performance efficiency of a BMS (Seeman, 2009:10-36), in this work, the SC was optimised to minimise ripple voltage during each shuttling cycle. When a linear capacitor is charged via voltage sources as in SC analysis, the capacitor loses a substantial fraction of the transfer energy in the charging process. The loss is due to the impulsive charging during the switching process and can be related to the square of the magnitude of each charge impulse (Seeman, 2009:10-36) as expressed in the Equation 32 .

$$E_{LOSS} = \frac{1}{2}\Delta q_C \Delta V_C = \frac{1}{2}C(\Delta V_C)^2 \tag{32}$$

The loss can be minimised if the impulses are of equal size in each phase, which is possible when the charge gained by the SC from a battery is equal to the charge transferred by the capacitor to the other battery in one shuttling period. When the charge shuttling is equal in each phase, then using Lagrange multiplier method for equality constraint optimisation problem, a SC size can be optimised, having minimum output impedance while the constraint on total energy is held constant (Seeman, 2009:10-36). The area (or volume) of capacitors is typically related to their maximum possible energy storage and the energy storage cost of a capacitor is related to its rated voltage $V_{C(rated)}$. Thus, the following optimisation will hold total capacitor energy storage E_{tot} constant using this constraint:

$$E_{tot} = \sum_{i \in caps} \frac{1}{2} C_i \left(V_{C,i(rated)}\right)^2 \tag{33}$$

Thus, if $C_{B1} = C_{B2} = C_{EQ}$, the total energy storage of the three capacitors in a SC equaliser can then be given as:

$$E_{tot} = \frac{3}{2} C_{EQ} \left(V_{C(rated)}\right)^2 \tag{34}$$

The optimised capacitor values and total output impedance (R_{out}) for a two-phase SC converter are given by the following expression (Seeman, 2009:10-36).

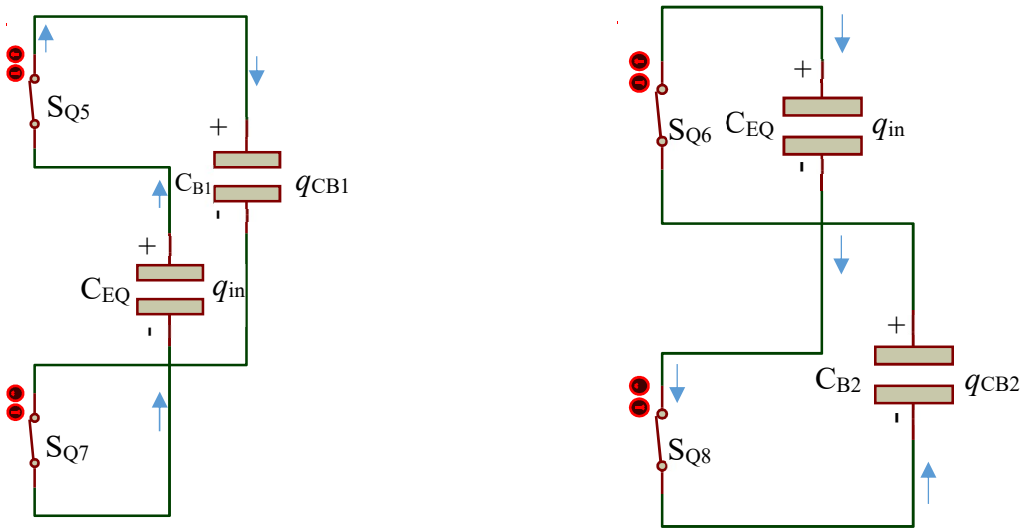
$$C_i = \left| \frac{a_{c,i}}{v_{c,i(rated)}} \right| \frac{2E_{tot}}{\sum_k \left| a_c . kv_{c,k(rated)} \right|} \tag{35}$$

$$R_{out} = \frac{1}{2E_{tot} f_{sw}} \left(\sum_{i \in caps} \left| a_c . iv_{c,k(rated)} \right| \right)^2 \tag{36}$$

Where a_c is a charge multiplier vector, which is equal in each phase for an optimised SC switching process. The charge multiplier vector corresponds to charge flows that occur immediately after the switches are closed to initiate each respective phase of the SC circuit and can be derived for any SC converter or equaliser.

3.5.1 Charge multiplier vector

A capacitor's charge multiplier vector a_c represents the charge flow into the capacitor, normalised with respect to the output total charge flow. For analysis, each phase of the SC charge equaliser as implemented in this work can be represented as Figure 44.



(a) Phase 1 **(b) Phase 2**

Figure 44: Switched capacitor charge flow

Let the charge flow into C_{EQ} be defined as q_{in} while q_{CB1} and q_{CB2} represent the output charge flow in phase 1 and phase 2 respectively. The sum of the output charges over both phases q_{out} equals to the sum of q_{CB1} and q_{CB2}. If $C_{B1} = C_{B2}$ for optimisation, then their maximum charge quantity will be the same. That is,

$$q_{CB1} = q_{CB2} = \frac{1}{2}(q_{out})$$

Assuming battery 1 voltage is higher than battery 2 voltage, by following the direction of charge flow, C_{EQ} is charged from C_{B1} in phase 1 and thus, q_{in} is positive while in phase 2, C_{EQ} is discharged into C_{B2} and q_{in} is negative with respect to total output charge. Applying Kirchhoff's current law (KCL), the charge flows are determined iteratively as follows:

Phase 1:
$$q_{in} = q_{CB1} = \frac{1}{2} q_{out}$$

Phase 2:
$$q_{in} = -q_{CB2} = -\frac{1}{2} q_{out}$$

The phase independent capacitor's charge multiplier vector a_c for all the capacitors with respect to total output charge is defined as:

$$a_c{}^1 = \left[q^1{}_{out} \quad q^1{}_{CB1} \quad q^1{}_{CB2} \quad q^1{}_{in} \right]^T / q_{out} \tag{37}$$

Each element is the ratio of charge transfer in each capacitor during phase 1 of the switching period to the charge delivered to the output during full period. We can re-write Equation 37 as:

$$a_c{}^1 = \left[a^1{}_{out} \quad a^1{}_{CB1} \quad a^1{}_{CB2} \quad a^1{}_{in} \right]^T = \left[\frac{1}{2} \quad \left(-\frac{1}{2}\right) \quad \frac{1}{2} \quad \frac{1}{2} \right]^T$$

Likewise in phase 2,

$$a_c{}^2 = \left[a^2{}_{out} \quad a^2{}_{CB1} \quad a^2{}_{CB2} \quad a^2{}_{in} \right]^T = \left[\frac{1}{2} \quad \frac{1}{2} \quad \left(-\frac{1}{2}\right) \quad \left(-\frac{1}{2}\right) \right]^T$$

3.5.2 Optimisation of the equalisation capacitor

By definition, the sum of the charge multiplier vector of the output charge flow a_{out} in both phases must be one. Using the above equations 35 and 36, the expression for optimising the equalisation

capacitor ($C_{EQoptimised}$) in a SC charge equaliser while switching across two battery outputs, B1 and B2 with capacitors *CB1* and *CB2* respectively connected across each battery can be given as:

$$C_{EQoptimized} = \left| \frac{a_{in}}{v_{c(rated)}} \right| \frac{2E_{tot}}{\sum_k \left| a_{out} k v_{c,k(rated)} \right|} \tag{38}$$

Substituting Equation 34,

$$C_{EQoptimized} = \left| \frac{a_{in}}{v_{c(rated)}} \right| \frac{3C_{eq}\left(v_{c(rated)}\right)^2}{\sum_k \left| a_{out} k v_{c,k(rated)} \right|} \tag{39}$$

Where a_{in} represents the charge multiplier vector into C_{EQ} in either phase, while the term $\sum_k \left| a_c k v_{c,k(rated)} \right|$ represents the absolute summation of the product of output capacitors rated voltages and their respective charge multiplier vectors in the output. The term $v_{c(rated)}$ is capacitor's rated voltage. For a choice of $25\ V_{(rated)}$ C_{EQ} and by substituting in the values of the charge multiplier vectors in to Equation 39, the optimised equalisation capacitor $C_{EQoptimised}$ can then be given as:

$$C_{EQoptimized} = \left| \frac{1/2}{25} \right| \frac{3\ x\ (25)^2 C_{EQ}}{|1\ x\ (50)|} = 0.75\ C_{EQ}$$

This optimisation value depends majorly on the charge multiplier vectors at the chosen optimisation conditions. The value remains the same as long as the capacitors $C_{B1} = C_{B2} = C_{EQ}$ and they are of the same rated voltage. Also using Equation 36, the total output impedance/resistance of the optimised SC at a selected switching frequency of 40 Hz can be given as:

$$R_{out} = \frac{1}{2E_{tot} f_{sw}} \left(\sum_{i \in caps} \left| a_c . i v_{c,k(rated)} \right| \right)^2 = \frac{1}{3C_{EQoptimized}\left(v_{c(rated)}\right)^2 x\ 40} (1x50)^2 = 0.222\ \Omega$$

This gives a minimum output impedance of the equalisation capacitor during charge shuttling process. However, if Equation 15 is used to determine the output impedance of the un-optimised equalisation capacitor 20000 μF at the same switching frequency of 40 Hz, a higher output impedance value will be derived.

3.6 COMPLETE CIRCUIT SIMULATION TEST

The designed SC equalisation circuit, as shown in Figure 35 schematic, was simulated using the Proteus 8.0 circuit design software before the practical implementation. The complete circuit simulation test is necessary in order to ascertain the switching feasibility of the designed SC circuit across any two batteries. This software also enables a digital oscilloscope interface through which the signal processes can be viewed. Some of the screenshots of the software interface during the simulations are shown in figures 45 to 48.

3.6.1 Schematic circuit simulation on Proteus 8.0 software

Figures 45 and 46 show the cropped view of the schematic circuit diagram during the simulation test.

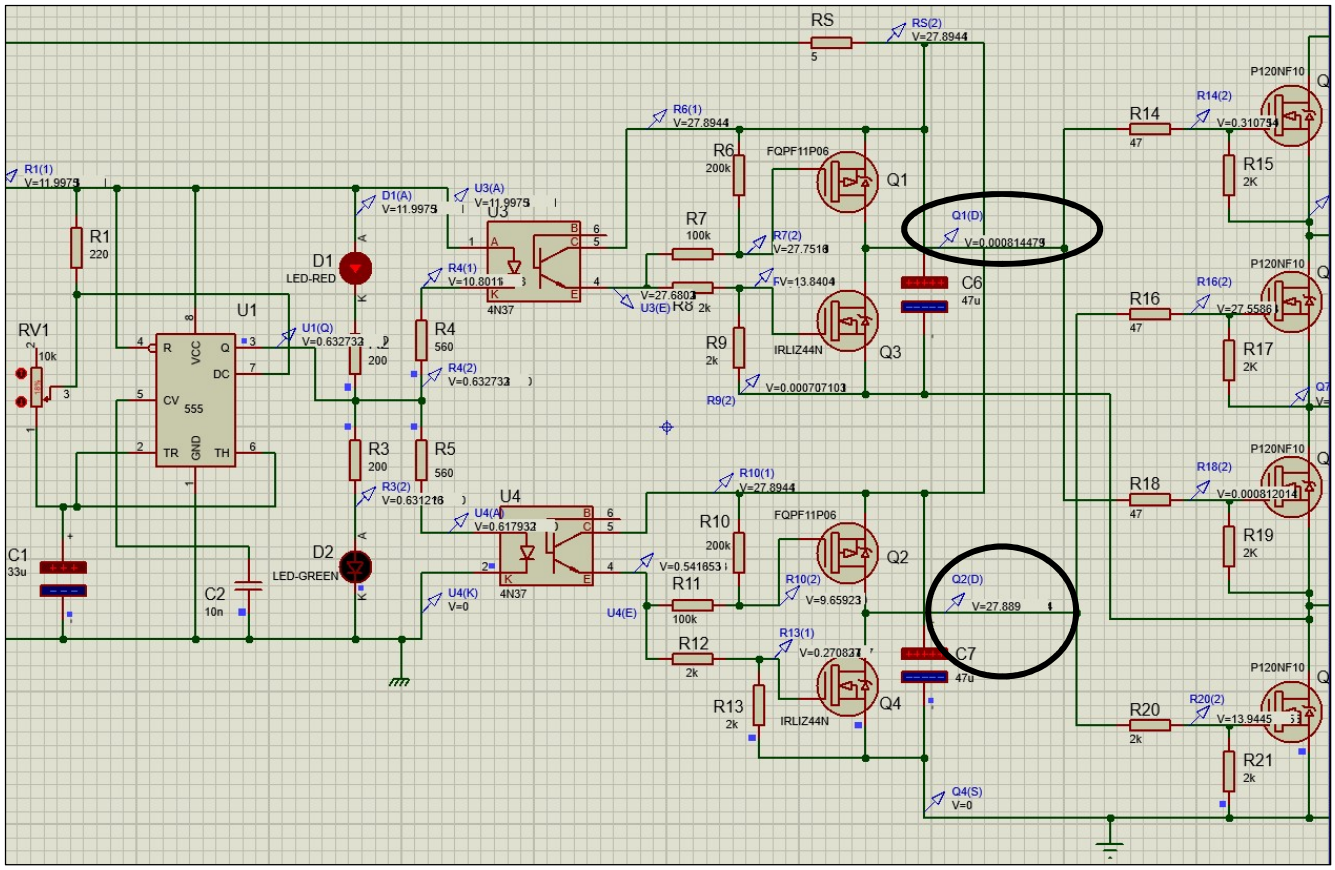


Figure 45: The bootstrap circuits I and II output voltage generation when triggered by alternated pulse signals (circuit I = 0V low output, circuit II = 27.89 V high output)

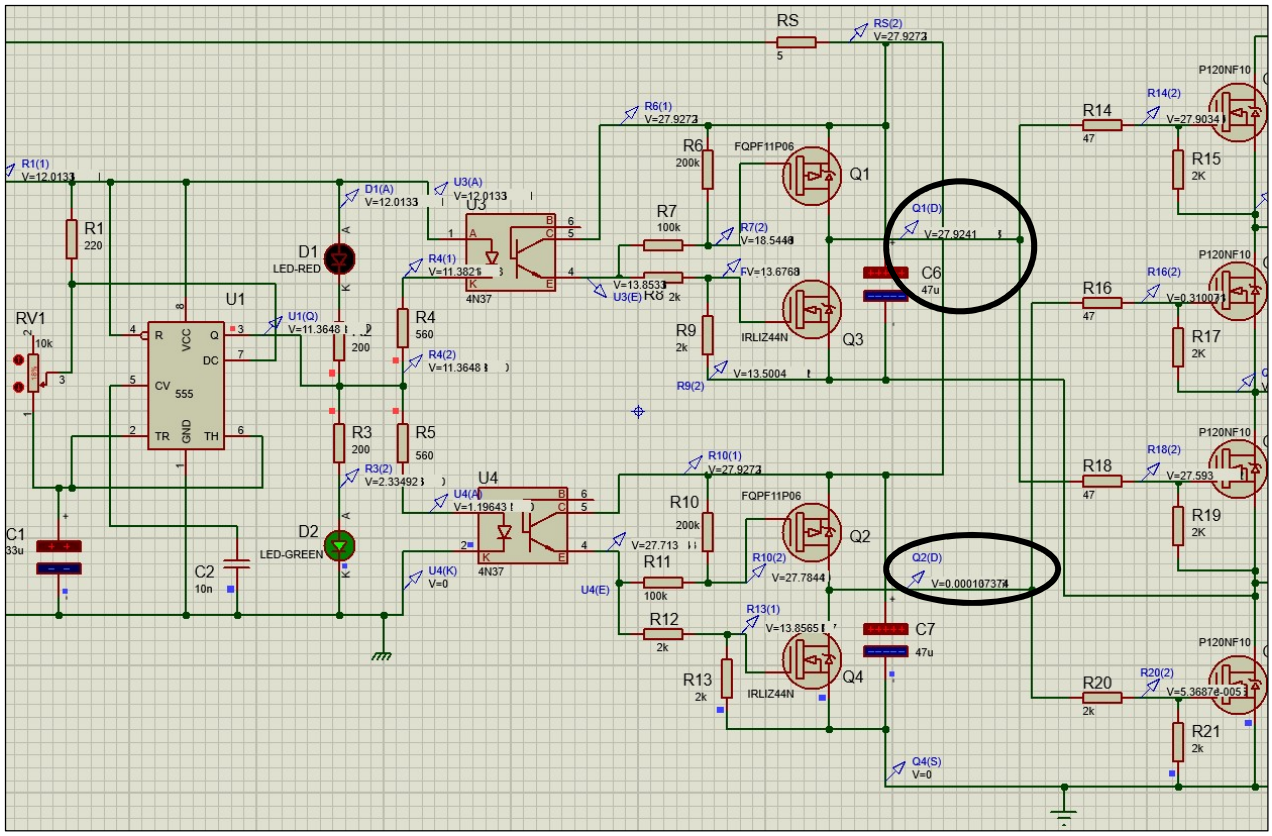


Figure 46: The bootstrap circuits I and II output voltage generation when triggered by alternated pulse signals (circuit I = 27.92 V high output, circuit II = 0 V low output)

These figures emphasise how the alternating pulse signal outputs from the astable multivibrator controlled the respective opto-couplers, which in turn control the bootstrap circuits I and II to generate an alternated isolated output DC voltage sufficient enough to drive the high-side MOSFETs in the circuit into conduction.

3.6.2 Digital oscilloscope interface

In figures 47 and 48 the digital oscilloscope view of four signal inputs: the astable multivibrator pulse signals, Bootstrap I&II output voltage supply signals and the SC charge-discharge voltage signal are shown. The digital oscilloscope views show the correlations between these signals and how the bootstrap outputs voltage could drive each MOSFET pair into conduction for switching the SC across the batteries.

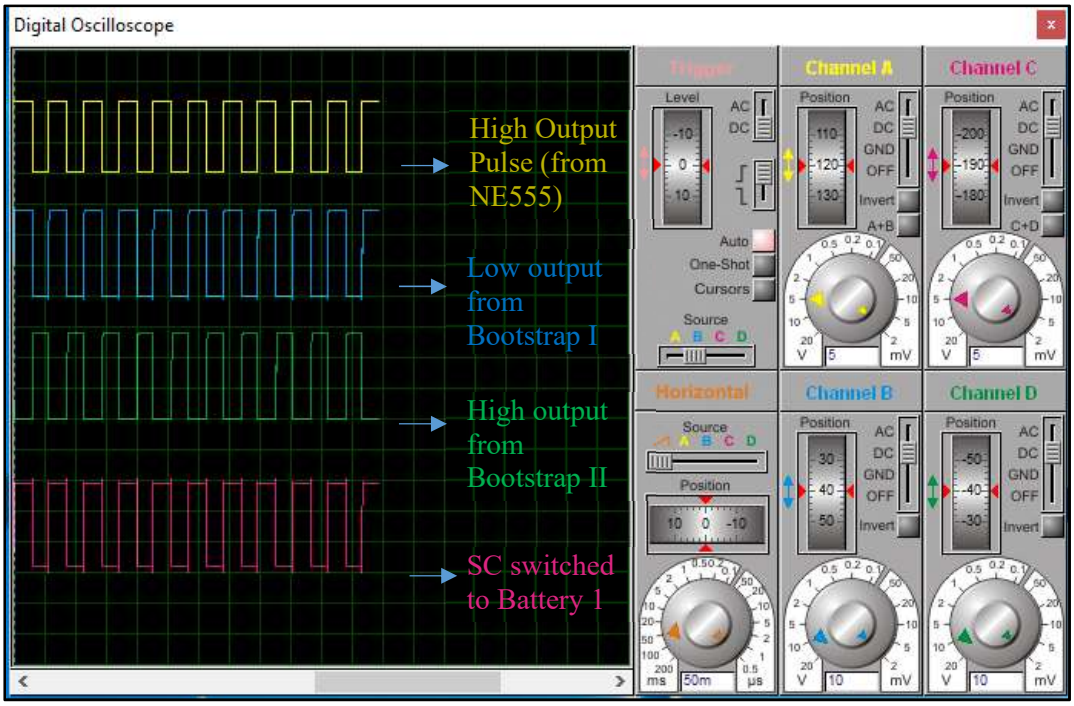


Figure 47: Digital oscilloscope interface indicating the switching of the SC across Battery 1 when Bootstrap II supplies a high gate drive voltage

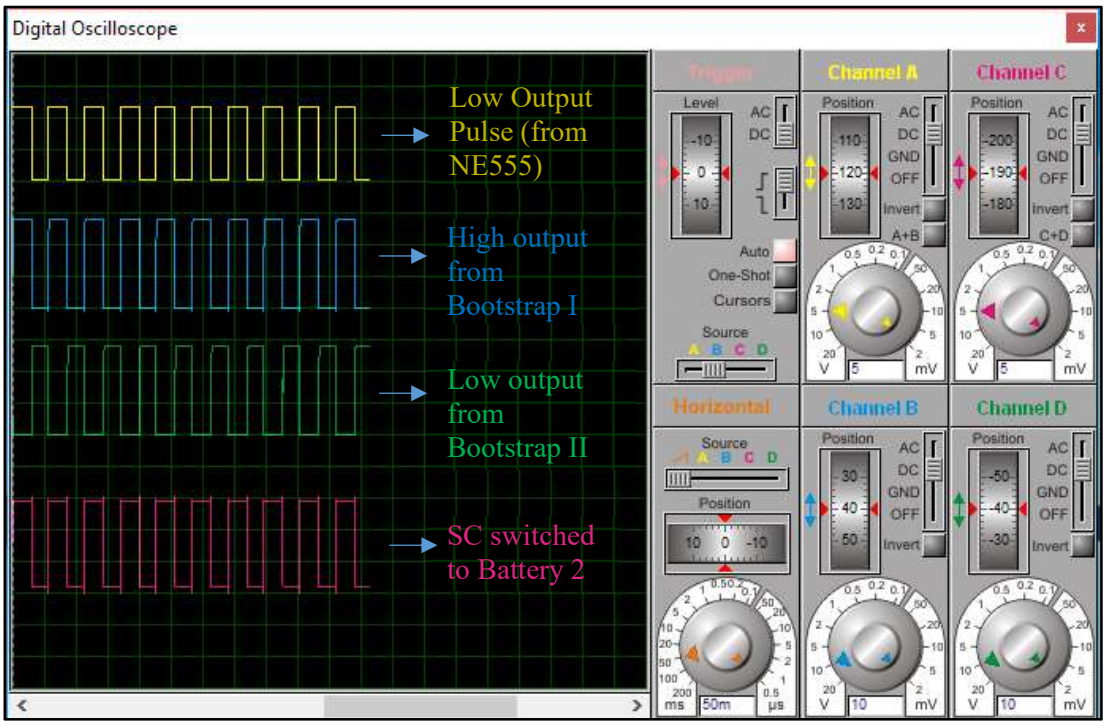


Figure 48: Digital oscilloscope interface indicating the switching of the SC across Battery 2 when Bootstrap I supplies a high gate drive voltage

3.7 PCB TRACE WIDTH CALCULATION AND LAYOUT

Trace width is an important parameter in PCB design, which is necessary to ensure the flow of desired current in a board without overheating or damaging it. The design rule IPC-2221 is widely used to analyse the correlation between temperature rise and the flow of current through copper traces in PCBs (Adam, 2004:292-299, Ling, 2002:1683-1693). A higher current requires wider traces, but when there is a thicker copper weight on the PCB, thinner traces may be appropriated.

The IPC data for PCB external traces were curve fitted by Brooks and the fits are given by the following relation (Brooks, 1998:23-27):

$$I = 0.065\,\Delta T^{\,0.43}\,A^{\,0.68} \tag{40}$$

Where I is the electrical current (measured in amps), ΔT the temperature rise above ambient (measured in ${}^{0}C$) and A is the cross-sectional area of the trace (measured in square mils).

A model from *Design News* data, meanwhile, suggested an improvement to Equation 40 by separating the area term (*A*) into its width *W* and thickness (*Th*) components (Brooks, 1998:23-27). Thus according to Brooks, using his curve-fitting experimental results, this can be given as the expression in Equation 41 below (Brooks, 1998:23-27, Wang *et al.*, 2009:1240-1246).

$$I = 0.028\Delta T^{\,0.46} W^{\,0.76} Th^{\,0.54} \tag{41}$$

Where *W* is measured in inches and *Th* in ounces of copper per square foot $\left(oz/ft^2\right)$.

The IPC-2221 design rule can be used to estimate the temperature rise due to an electrical current using the nomograph from IPC-2221 design rule as shown in Figure 49. Here, the cross-sectional area of the trace is determined first, then the value is used to graphically mark out the data couple of current I and the temperature rise ΔT as indicated by Example 1 or Example 2 in the nomograph.

Otherwise, if the current flow, the temperature rise above ambient and the area of the PCB are pre-determined, then Equation 41 can be used to calculate the trace width of the PCB in respect of these known parameters.

In the design analysis of this work, a single side copper clad laminate board having copper thickness of $1oz$ (0.7257 mil) is used for the PCB design. With respect to prior maximum current flow estimation, a maximum current of 3.0 A is estimated to flow through the power tracks of the PCB external traces, while the temperature rise above ambient ΔT of the board is chosen to be $10^0 C$.

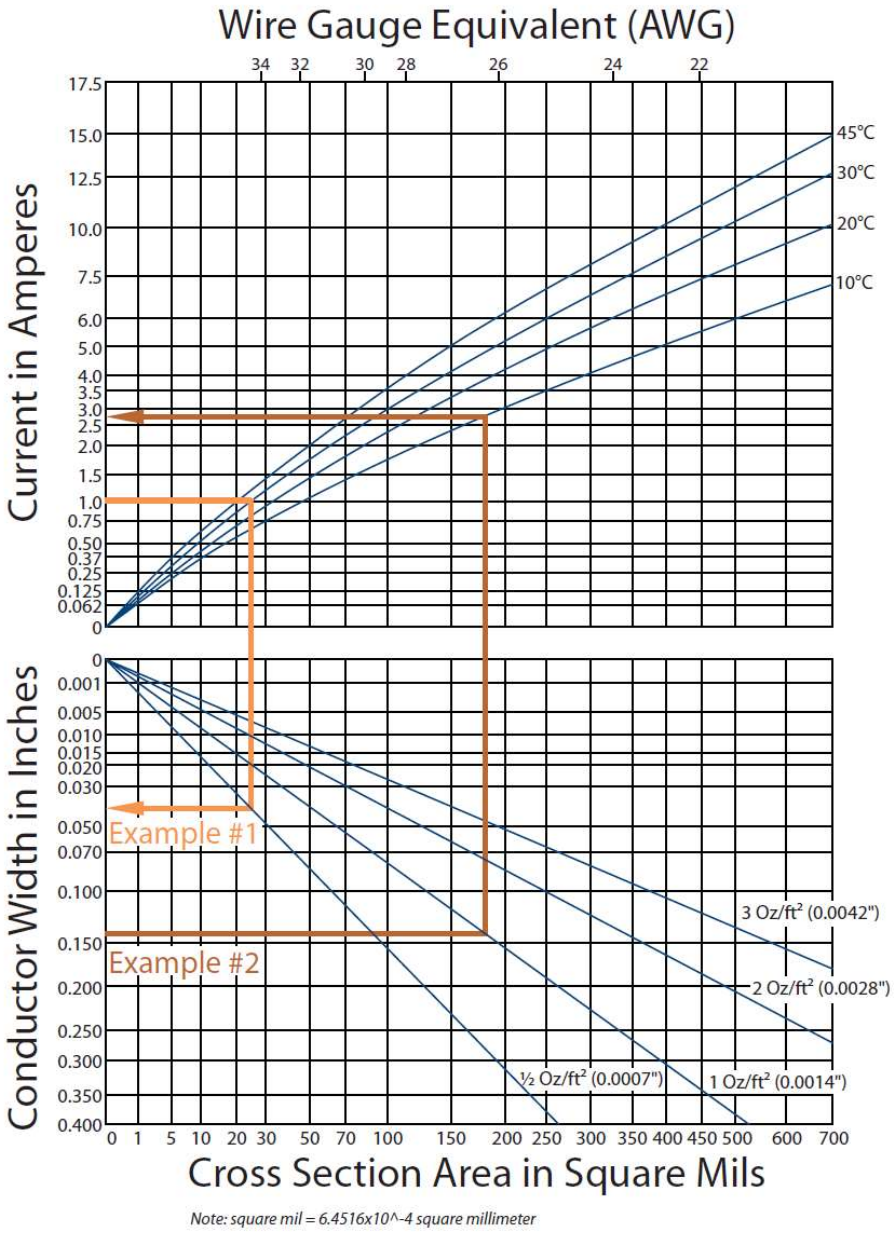


Figure 49: IPC-2221 nomograph for PCB design rule (Brooks, 1998:23-27)

The trace width of the PCB for the SC equalisation circuit designed in this work is calculated based on these determined parameters using the Equation 41.

That is;

$$W^{0.79} = \frac{I}{0.028\Delta T^{0.46} Th^{0.54}} = \frac{3}{0.028\left(10^{0.46}\right)\left(0.7257^{0.54}\right)} = 44.1925\ mils$$

$$\Rightarrow W = \left(44.1925\right)^{1/0.79} = 120.98\ mils = 0.121\ inch \cong 3\,mm$$

Thus, the calculated trace width, 0.121 inch $(\cong 3\,mm)$, which is close in value to 0.15 inch that can be derived when the same parameters are traced out from the nomograph, gives the minimum trace width of the PCB power tracks. However, the use of this trace width $(\cong 3\,mm)$ on Proteus 8.0 software caused design rule error on the terminals of power MOSFETs used for switching the equalisation capacitor between the batteries.

Hence, each battery voltage was divided into half using divider resistors before connecting to the switching circuit. Based on Ohm's law, the current flow to a circuit reduces when the voltage is decreased at the same resistance value. After the division, a maximum estimated current of 1.5 A is expected rather than 3.0 A. With other predetermined parameters still the same, the trace width is then calculated to be 0.06 inch $(\cong 1.5mm)$. The spacing between these traces is also chosen to be approximately the same value for better clearance between the traces.

In Figure 50, the designed printed circuit board (PCB) using Proteus 8.0 software is shown. According to Jacob (2002), the wider the copper thickness and track width of a PCB design, the lower the resistance and thus a smaller voltage drop in the circuit (Jacob, 2002); thus from the PCB layout of this design, the power tracks through which relatively high current would flow was made wider than the signal tracks.

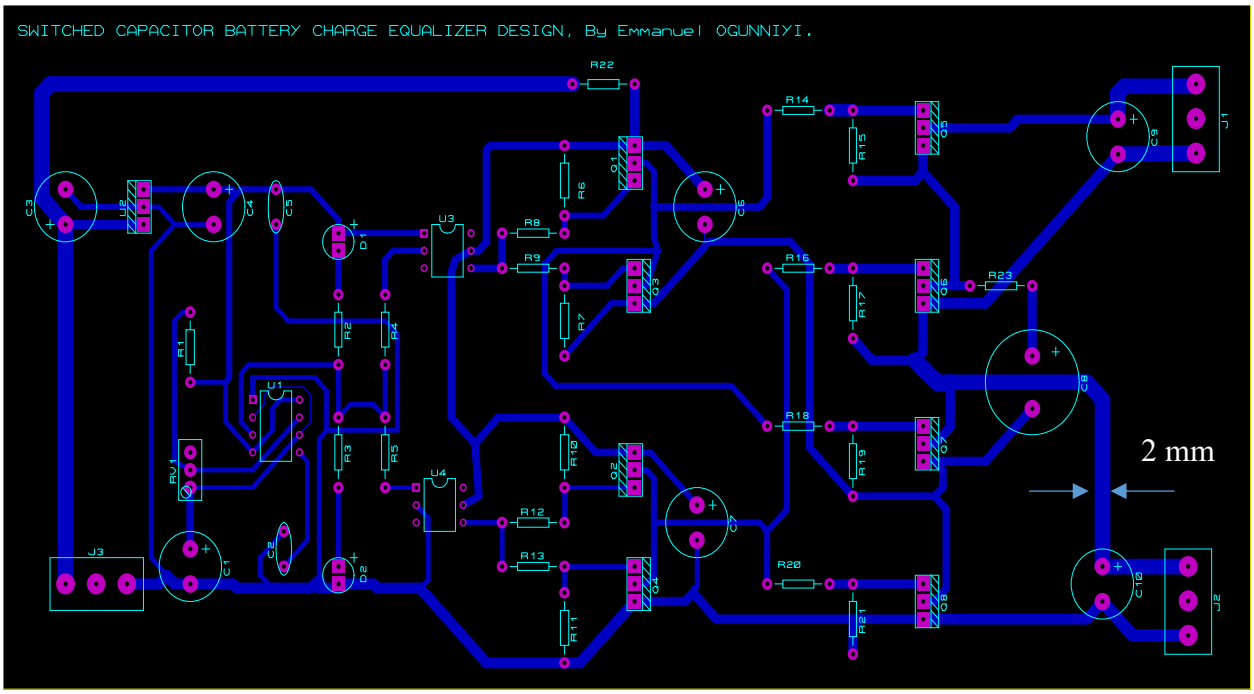


Figure 50: PCB board layout of the designed switched capacitor (SC) equaliser circuit using Proteus 8.0 software

3.8 3D VISUALISATION AND COMPLETE PROTOTYPE MODULE OF THE PCB DESIGN

In Figure 51, the 3D visualisation of the designed PCB as implemented on Proteus 8 software is shown. This 3D view enables the designer to have the imagination and idea of the end view of the design from the start, thus enabling a proper positioning and arrangement of the components.

Figure 52 shows the prototype of the SC active charge equaliser, which was designed and tested in the laboratory. During the operation of the design, additional capacitors were added to the board in a separate Vero board in order for the capacitor to measure up to the desired supercapacitor value required for the design analyses.

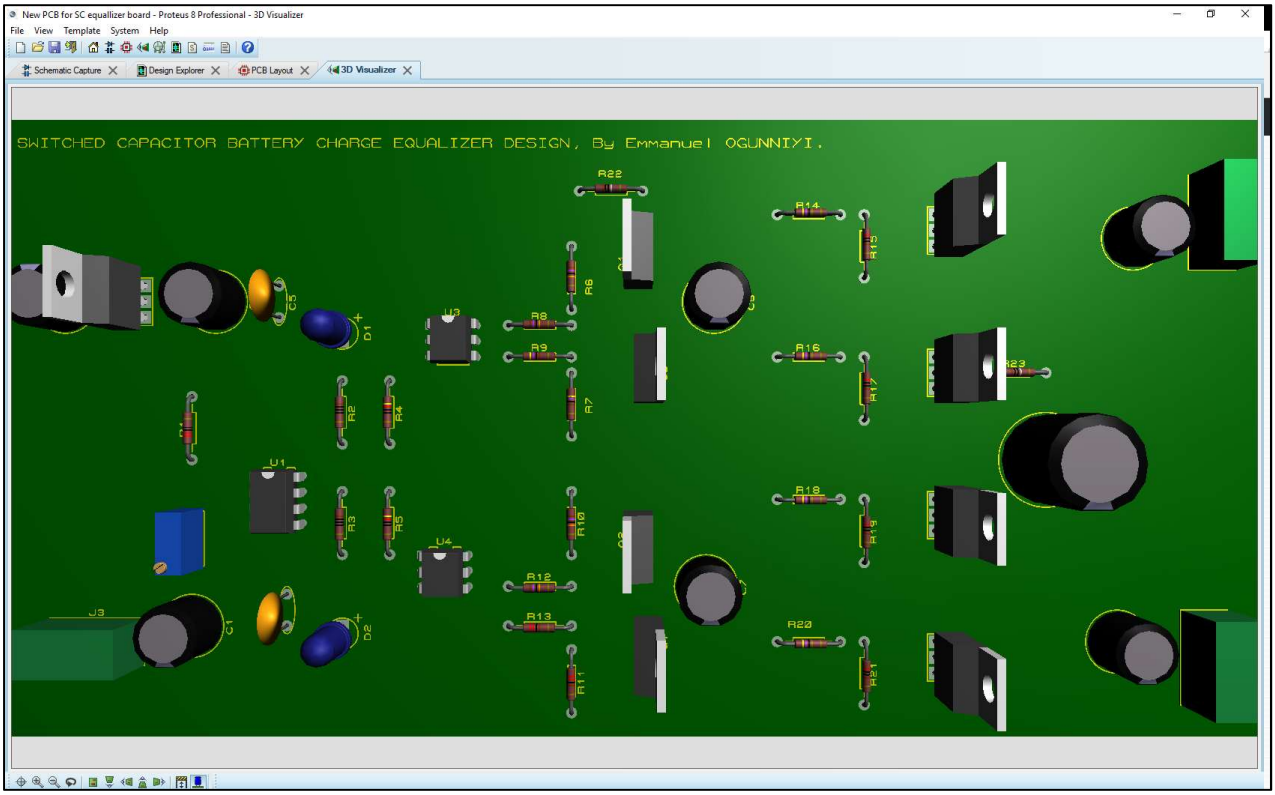


Figure 51: 3D view of the PCB board layout of the designed switched capacitor (SC) equaliser circuit using Proteus 8.0 software

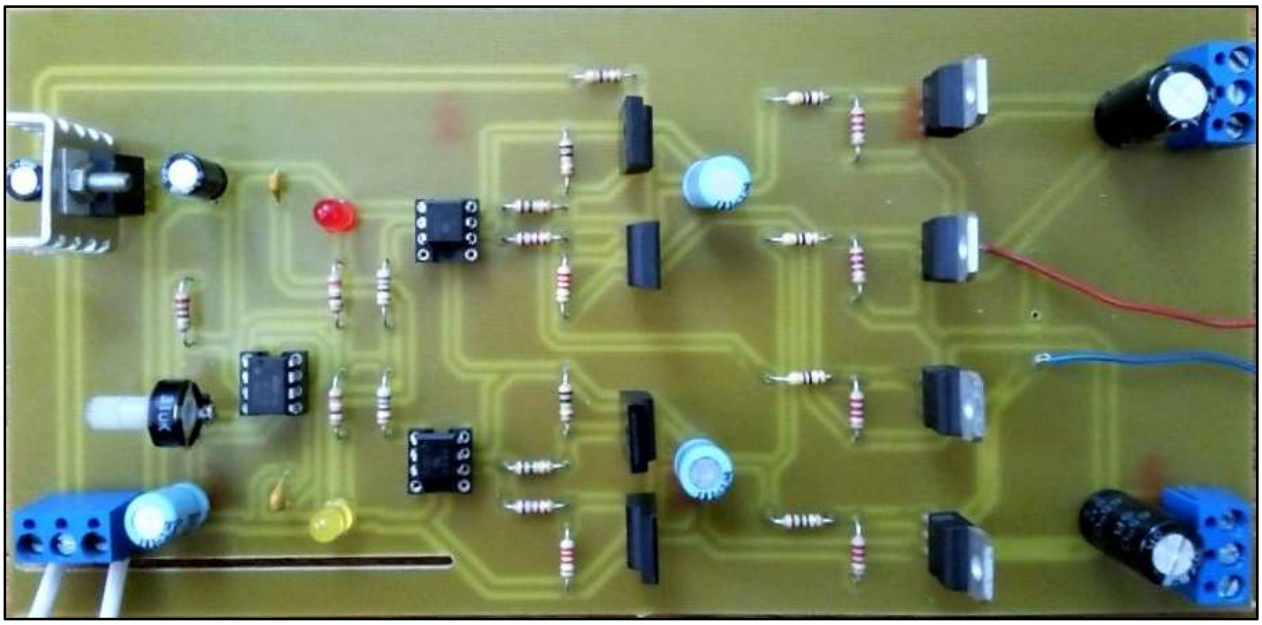


Figure 52: Prototype of the switched capacitor (SC) battery charge equaliser

3.9 DESIGNED EQUALISER INTEGRATION INTO THE BATTERY MANAGEMENT SYSTEM (BMS)

As earlier indicated in the Section 2.4.1, the design consideration of a BMS includes full battery charge equalisation capability among other features such as data acquisition, battery SOC determination, safety management (overcharge- and under voltage protection) and communications. Therefore, to integrate the SC battery charge equaliser designed in this work into a BMS, data acquisition, logging and monitoring devices were introduced. In addition, with the implementation of computer interface, the data were monitored in real-time during the equalisation processes for analysis.

3.10 OPTIMISATION OF THE DESIGNED BATTERY MANAGEMENT SYSTEM (BMS)

The optimisation of the designed BMS was carried out in the following ways:

- Power supply to the circuit was taken from the extra DC output from the solar charge controller. This makes the system to be powered by renewable energy and allows energy efficiency.
- The pulse output from the 555-timer astable multivibrator was utilised to supply both inverting and non-inverting outputs simultaneously to the system without the use of MOSFET drivers. Additionally, this reduces the energy requirement to drive the MOSFETs while also making the circuit less complicated.
- The SC circuit was designed with a unique configuration of low frequency and high capacitance value to reduce the ripple voltage across the capacitor during the shuttling process. The equalisation capacitors value was estimated based on the design parameters and thereafter optimised for usage through calculation based on the chosen optimisation conditions.
- The designed BMS was designed in the SC active charge equalisation technique in order to accommodate other battery technologies and is not restricted to lead acid batteries only.

3.11 PRACTICAL SETUP OF THE BATTERY MANAGEMENT SYSTEM (BMS)

The practical setup of the BMS as designed and analysed in this work is shown in Figure 53.

The setup shows some of the important devices used in the implementation of the BMS, such as the solar charge controller, digital oscilloscope, designed SC active charge equaliser, data loggers and the computer interface for real-time monitoring of the BMS process and operations. Two data loggers were implemented; PicoLog and a designed current logger. These were used simultaneously to log the data from the battery string and SC respectively. More details about the analysis of this design are reported in the following chapter.

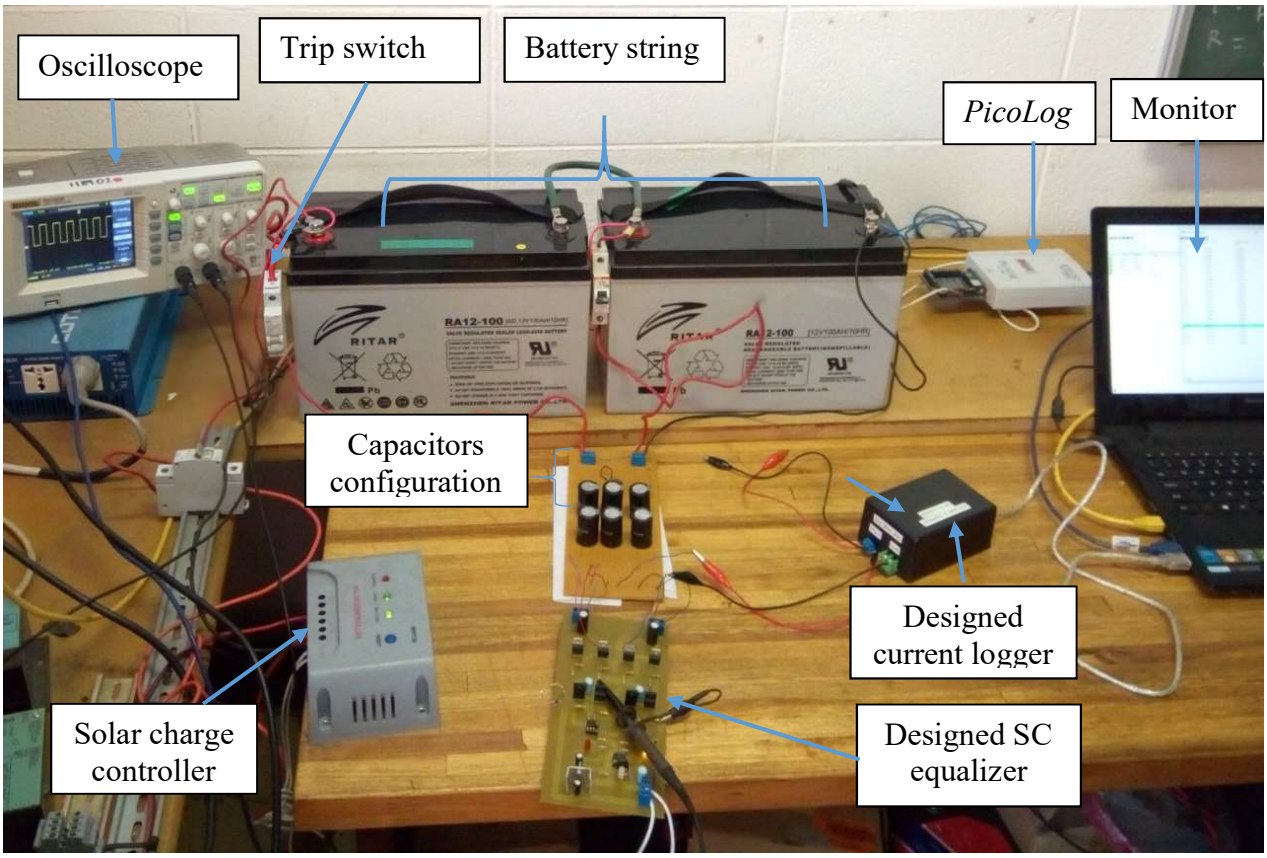


Figure 53: Practical setup of the designed battery management system (BMS)

3.12 SUMMARY

In this chapter, a practical design of a universal BMS in a stand-alone photovoltaic application using a SC equalisation technique was presented. An alternative DC output from a solar charge controller was utilised to power this design and a necessary simulation on the design was done and reported in order to ascertain its practicality. The equalisation capacitor of the SC circuit was mathematically optimised to reduce its ripple voltage and reduce the losses attributed to its impulse charging during each shuttling cycle. The printed circuit board layout of the designed SC charge equaliser both on 3D and prototype views were presented. Lastly, the analysis presented shows a systematic approach in the order of charge flow from the solar panel to the charge controller and to the designed charge equalisation system while the implementation of data logging devices and computer interface for real-time monitoring of the process enable integration into a BMS.

CHAPTER 4: MEASUREMENT AND RESULTS

In the previous chapter, the design of a universal BMS in a stand-alone photovoltaic application using SC active charge equaliser topology was presented. A systematic approach in the order of charge flow from the solar panel to the charge controller, then to the designed charge equalisation system was presented. The extra DC output from the solar charge controller was utilised to power the design and with the introduction of data-logging devices, the charge equaliser was integrated into a BMS through which the operations or data of the batteries during charge equalisation process can be recorded, monitored and illustrated graphically in real time on a computer interface.

This chapter presents the measurements and results obtained when the designed charge equaliser was tested and analysed with different battery types used in photovoltaic applications. These batteries must be of the same nominal ratings to be paired for charge equalisation. The simulation results and oscilloscope measurements are presented for comparison. In addition, the empirical data obtained from the experimental analyses are presented and illustrated graphically for evaluation.

4.1 INTRODUCTION

The designed battery equaliser in this work was integrated into a universal BMS through the introduction of data-logging devices, which record the empirical data obtained in real time on a computer. Two data loggers were used; the first was connected to the equaliser circuit to measure and record the current and voltage data of the SC during equalisation, while the other data logger connects with the batteries terminals to measure and record the voltages and/or the charge equalisation among the batteries.

In this work, charge equalisation was performed on different battery pairs at room temperature during their float charging state when no external load is connected to the batteries. This is because during float charging, charge imbalance is more evidently displayed among the battery pairs (Ogunniyi & Pienaar, 2016:422-427). Also, room temperature does not significantly contribute to any noticeable electrochemical variation or effect that could cause charge imbalance or affect charge equalisation process among batteries such as lead acid (Berndt & Teutsch, 1996:790-798).

4.2 SETUP AND EVALUATION OF THE DESIGNED BMS

The experimental setup of the designed BMS in this research is shown in Figure 54.

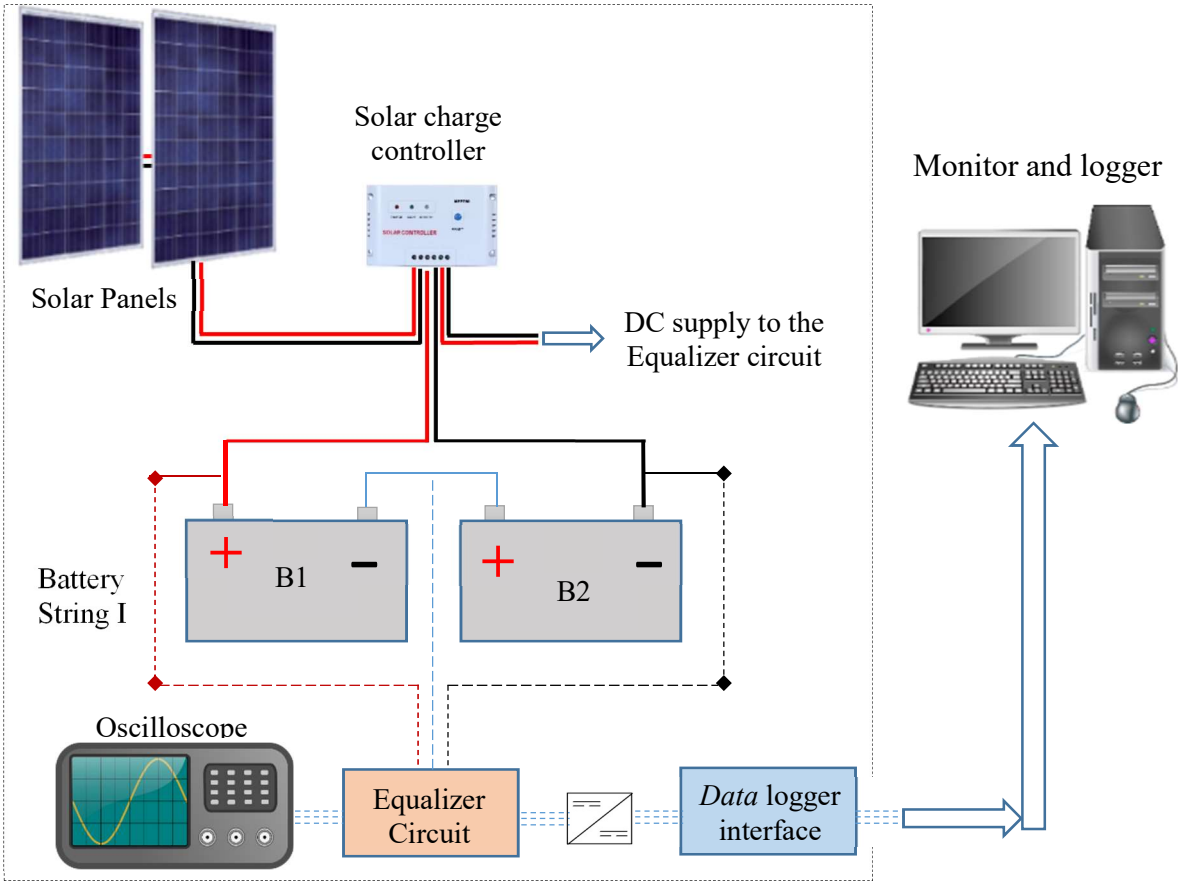


Figure 54: Block diagram of the complete battery management system (BMS) setup

For the evaluation of the design, a simulation of the designed charge equaliser was done using the Proteus 8.0 circuit design suite to ascertain its charge shuttling and equalisation ability. The charge equaliser circuit was then integrated with the data logging device and signal monitoring device, the oscilloscope, which are both captured on the computer interface for analysis.

The BMS was evaluated on four battery types, which can be used in a stand-alone photovoltaic application. These are:

- Absorbent glass mat (AGM) valve-regulated lead acid (VRLA) battery
- Silver calcium battery

- Silver zinc battery
- Lithium ion battery

The simulation results of the circuit during evaluation of the design were then compared with the real-time oscilloscope test results to ascertain the coherence of the circuit's functionality. The empirical data obtained from the BMS were recorded and illustrated graphically and the performance of the system was evaluated with respect to the batteries charge imbalance before and after the equalisation process.

4.3 ELECTRICAL CONFIGURATION AND MONITORING OF THE DESIGNED BMS

The configuration of the designed BMS includes the implementation of the data logging devices, which were configured to ensure precise recordings and the integration of oscilloscope for real-time measurements and comparison with the simulated results.

4.3.1 Data loggers' implementation

- PicoLog 1216 data-logger: PicoLog 1216 was used to record the parameters of the battery pairs during charge equalisation. This data-logger, however, allows a maximum input voltage of 2.5 DC voltage, thus for measurement and logging of 12 V batteries whose voltage supplies are about six times the DC voltage input limit of this device, an intermediate voltage divider circuit, which divides the battery voltage supply by a factor of six, was introduced. In the software configuration of the PicoLog, this input voltage is then multiplied by a factor of six in order to get the actual measurements of the battery voltages. Further details about this PicoLog device are shown in its datasheet as included in Annexure G.

The schematic diagram of the voltage divider circuit, which was implemented to supply the appropriate voltage range to the PicoLog device is shown in Figure 55.

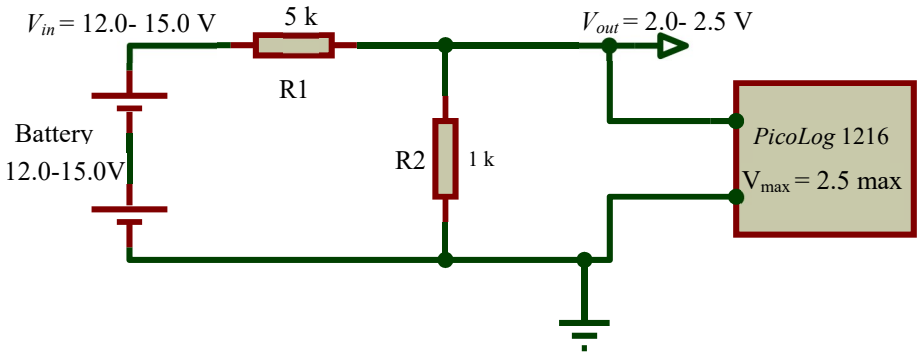


Figure 55: Schematic of voltage divider circuit interface with PicoLog device

A voltage divider expression in Equation 28 was used for the calculation of the appropriate voltage range to the PicoLog device.

$$Vout = Vin\left(\frac{R2}{R1+R2}\right) \tag{28}$$

$$Vout = \left(\frac{1}{6}\right)Vin$$

The cropped screen shot of the PicoLog computer interface during one of the logging periods is shown in Figure 56 below.

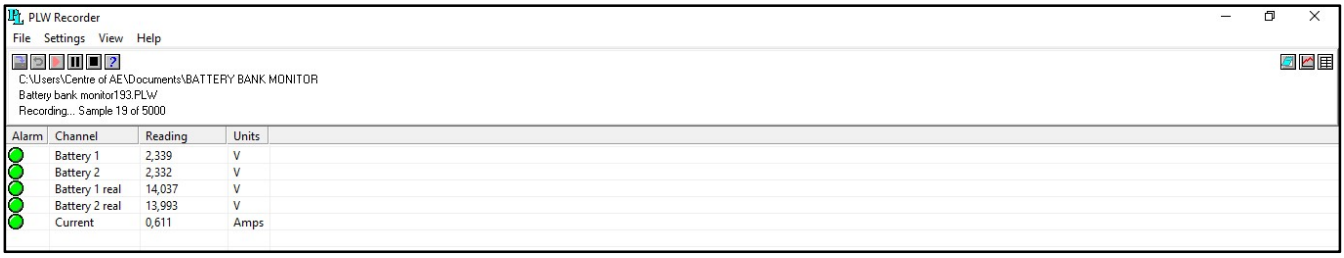


Figure 56: PicoLog computer interface during a typical logging period

In Figure 57, a magnified view of the PicoLog software interface, which shows the battery measurement Battery 1 and Battery 2 from the voltage divider and the calculated measurement Battery 1 real and Battery 2 real after the multiplication factor, has been applied.

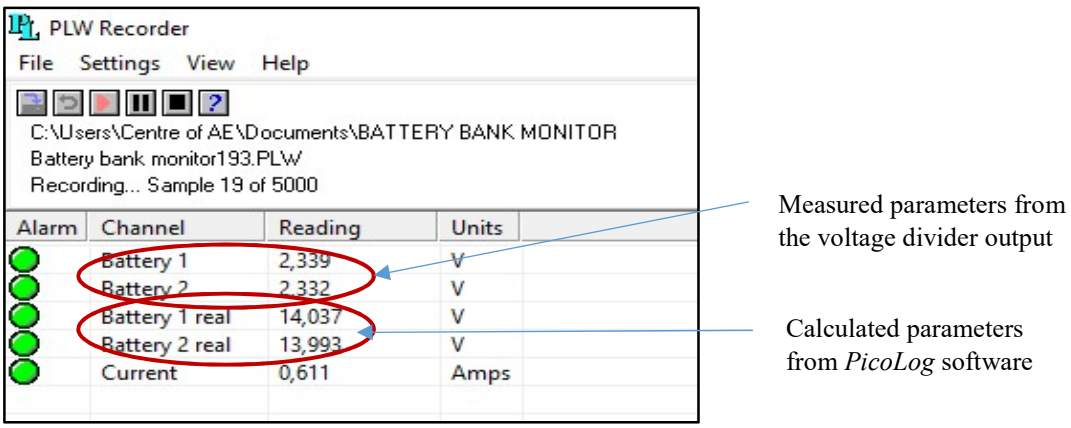


Figure 57: Magnified view of the PicoLog software interface showing the measured parameters from the voltage divider circuit and the calculated parameters

The other data logger used was designed locally for logging the current flow through the SC during the equalisation process. The design was made using Allegro® ACS712 hall effect-based linear current sensor IC incorporated with micro-controller based Arduino UNO REV3 development board for logging of the data detected. The details of the current sensor IC and the development board are attached in the Annexures H and I respectively. The current data-logger was configured to take 40 samples in 1 second, corresponding to the switching frequency. The screen shot of its interface is shown in Figure 58.

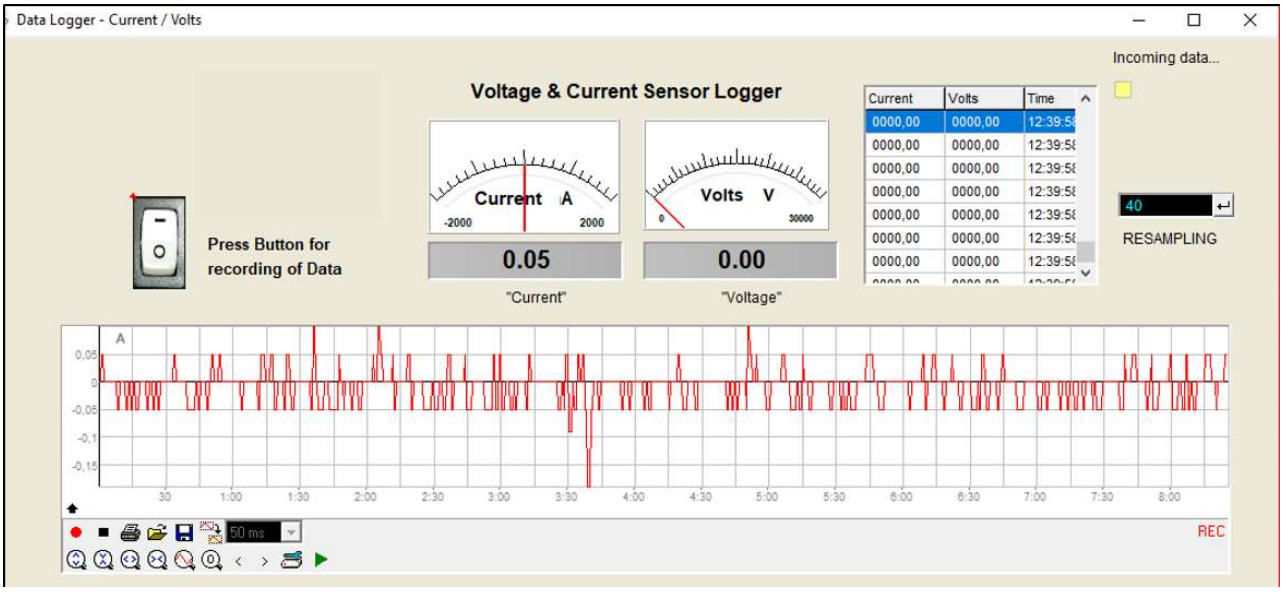


Figure 58: The designed current data logger interface

4.3.2 Simulation results and the oscilloscope real-time measurements

The designed SC equaliser circuit was simulated on the digital oscilloscope interface of Proteus 8.0 software. The results of the simulations at some strategic points in the circuit analysis were compared with the real-time measurement results derived from RIGOL DS1000E digital oscilloscope during the operation design prototype.

From comparison, the simulation results and the oscilloscope real-time results show some consistencies in their signal formations when observed at approximately the same frequency and charge imbalance conditions. Unfortunately, the digital oscilloscope could not display all the parameters' detail as against a normal physical oscilloscope, thus, only the graphical representation of the signals was recorded for comparison to ascertain the consistency of both results. The figures 59 to 66 show the comparison results from both the simulation and the real-time measurements at some indicated strategic points on the circuit.

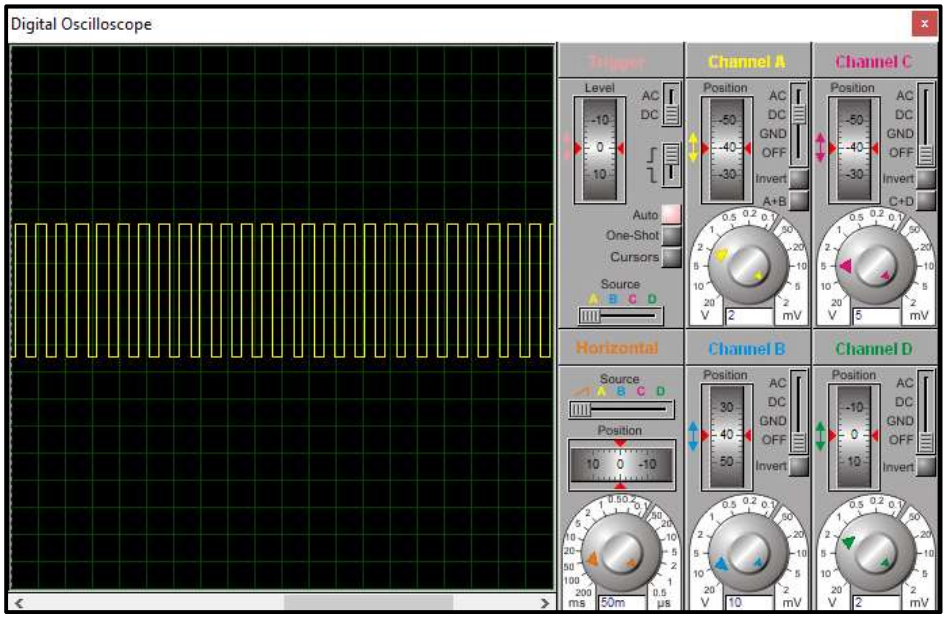


Figure 59: The digital oscilloscope simulation result of the 555 timer output pulse signal

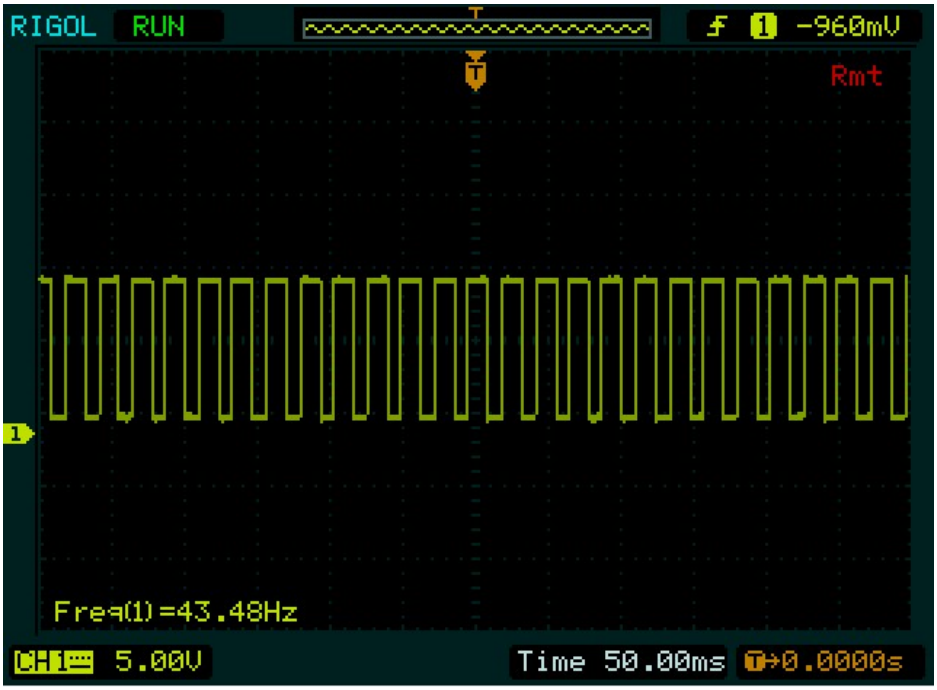


Figure 60: The real-time oscilloscope view of the 555 timer output pulse signal during operation

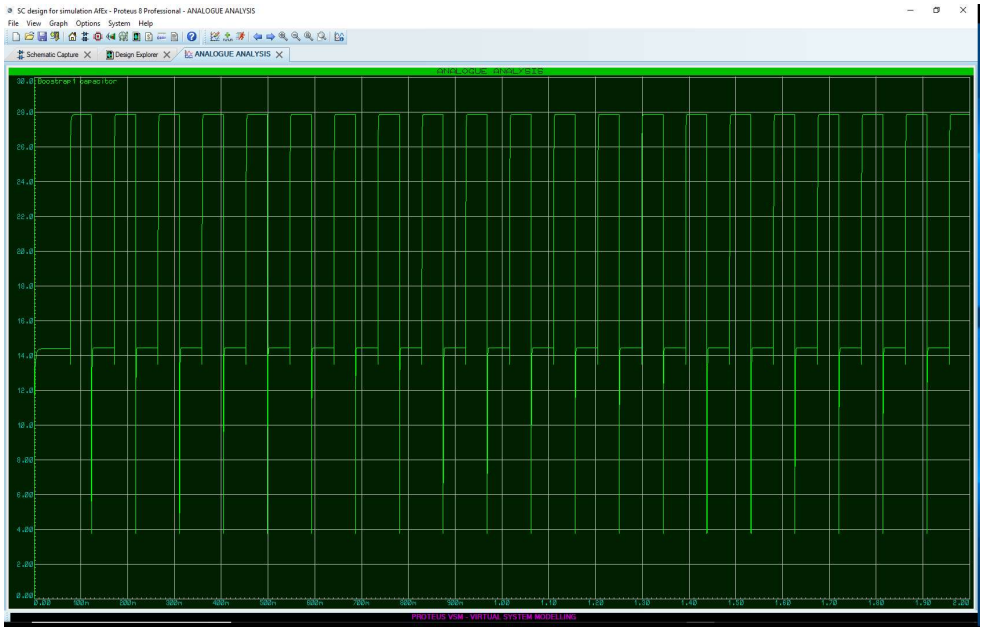


Figure 61: The virtual graphical simulation result of the bootstrap capacitors during charging and discharging

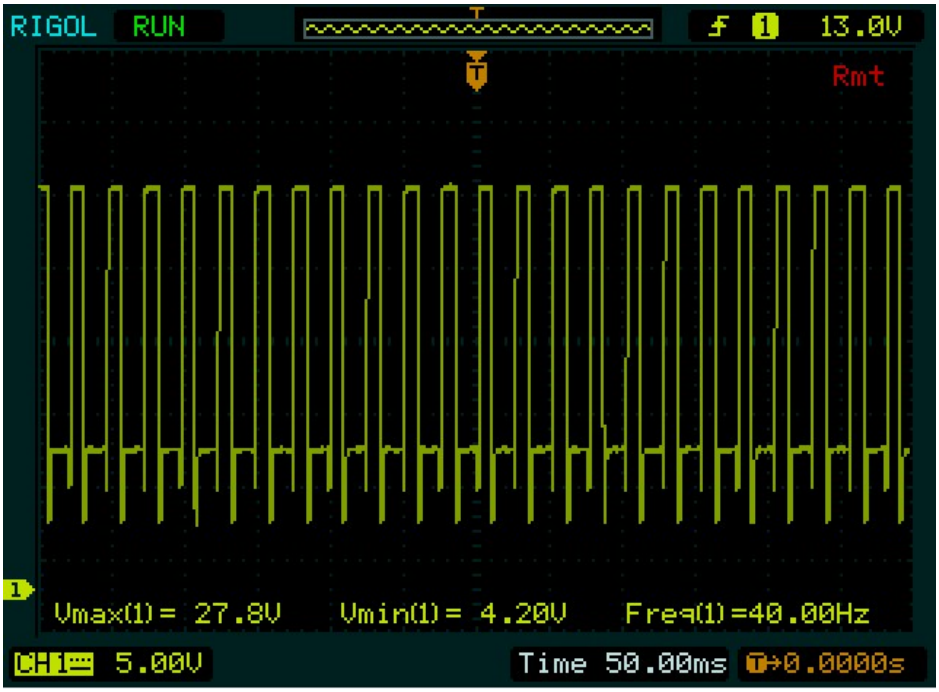


Figure 62: The real-time oscilloscope view of the bootstrap capacitors during operational charging and discharging

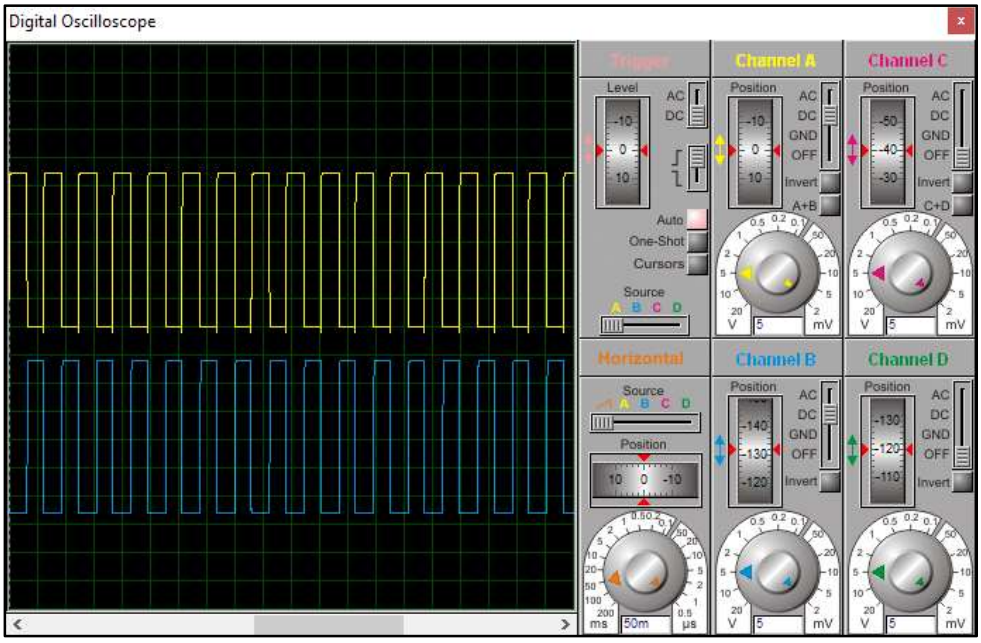


Figure 63: The digital oscilloscope simulation result of the optocouplers I and II pulsating DC voltage outputs

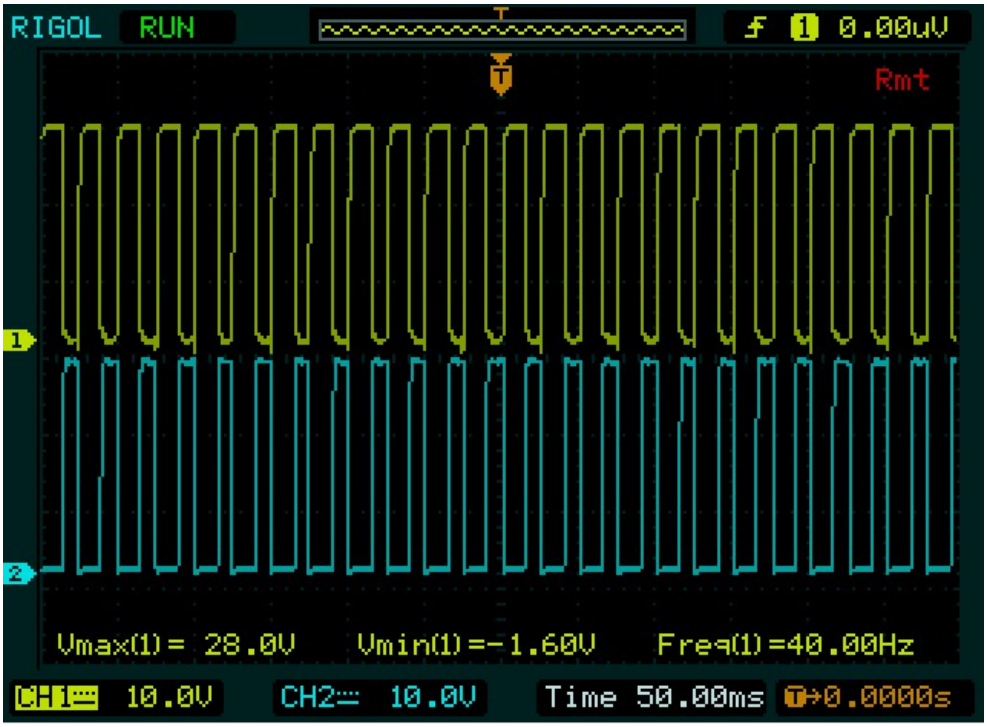


Figure 64: The real-time oscilloscope view of the optocouplers I and II pulsating DC voltage outputs during operation

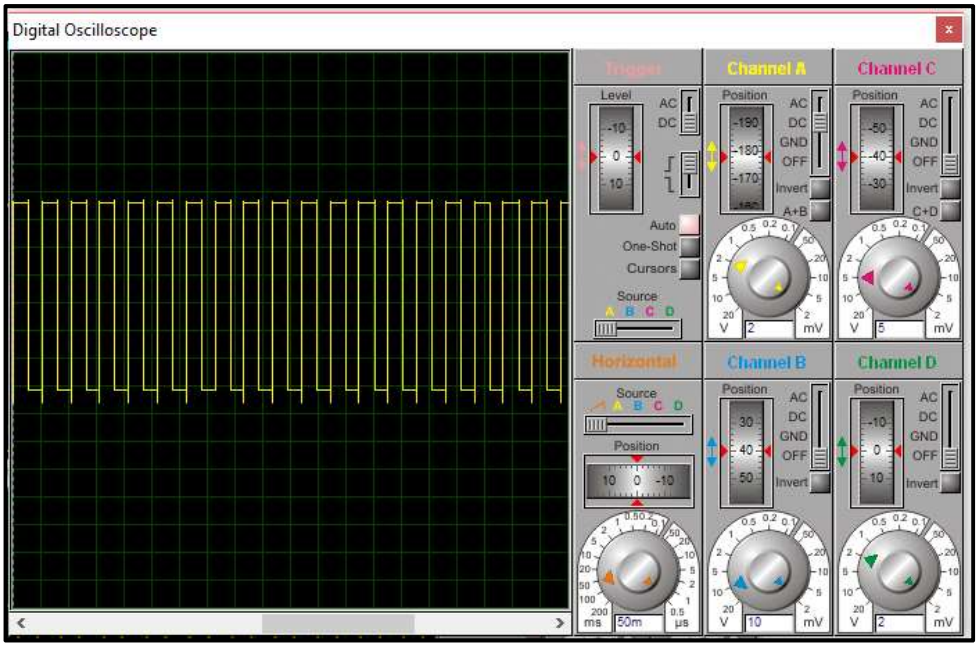


Figure 65: The digital oscilloscope simulation result of the switched capacitor (SC) while switching between two batteries of differential voltages

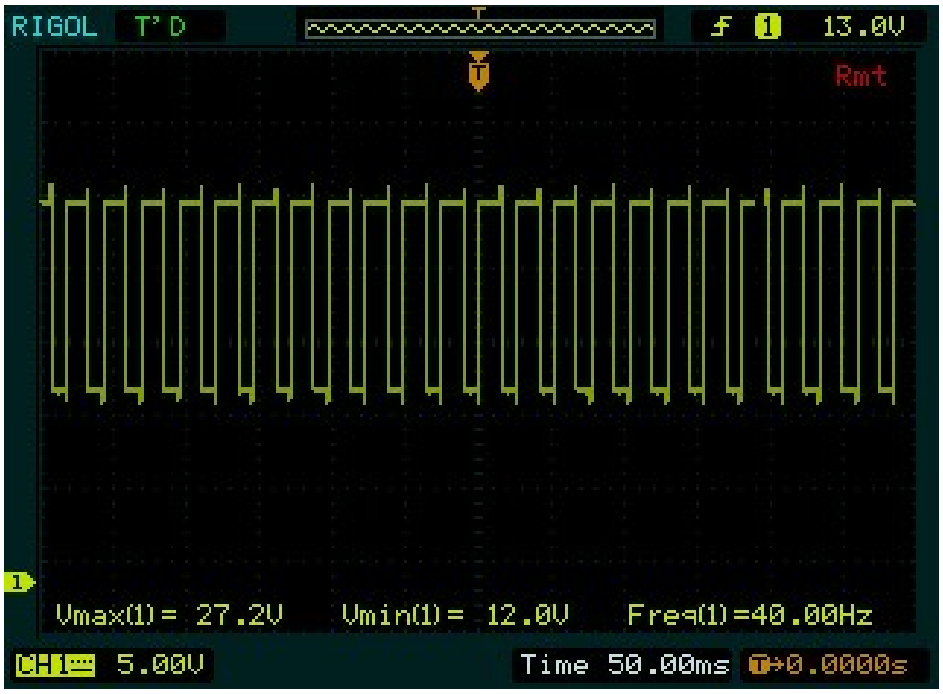


Figure 66: The real-time oscilloscope view of the switched capacitor (SC) while switching between two batteries of differential voltages during operation

4.4 PERFORMANCE EVALUATION OF THE DESIGNED CHARGE EQUALISER ON SELECTED BATTERY TYPES

The designed battery charge equaliser was tested with some battery types used in photovoltaic and deep-cycled applications in order to ascertain its functionality. These selected batteries are absorbent glass mat (AGM) valve-regulated lead acid battery, silver calcium battery, lead calcium battery and lithium-ion battery.

4.4.1 Equalisation test on a lead acid battery

The lead acid battery model used for this test is Ritar 12 V, 100 Ah AGM valve-regulated lead acid (VRLA) battery. This battery type, AGM VRLA, is one of the most commonly used batteries for a stand-alone photovoltaic application. The information about the battery model is included in its datasheet as attached in Annexure J of this study. Table 4 shows the test results when the designed charge equaliser was tested on the battery pair. The charge imbalance before (Δv_{before})

and after the equalisation has been completed (Δv_{after}) as highlighted in Table 4 were recorded and analysed to determine the effectiveness of the system.

Table 4: Equalisation tests results for lead acid battery

Time (minutes)	Δv_{before} = **(1,0272 V)**		Batteries current (A)
	Battery1 (V)	Battery1 (V)	
0	14,5392	13,5120	0,5853
0,5	14,5379	13,5131	0,5825
1	14,5382	13,5117	0,5853
1,5	14,5319	13,5120	0,5805
2	14,5407	13,5103	0,5866
2,5	14,5210	13,5121	0,5746
3	14,5219	13,5173	0,5721
3,5	14,4811	13,5194	0,5481
4	14,4608	13,5408	0,5247
4,5	14,4395	13,5605	0,5018
5	14,4182	13,5802	0,4788
5,5	14,4040	13,5999	0,4598
6	14,3981	13,6106	0,4505
6,5	14,3805	13,6213	0,4347
7	14,3707	13,6320	0,4232
7,5	14,3590	13,6427	0,4106
8	14,3472	13,6534	0,3980
8,5	14,3355	13,6641	0,3854
9	14,3237	13,6748	0,3729
9,5	14,3120	13,6855	0,3603
10	14,3002	13,6962	0,3477
10,5	14,2990	13,7059	0,3416
11	14,2878	13,7099	0,3331
11,5	14,2833	13,7143	0,3280
12	14,2771	13,7184	0,3222
12,5	14,2709	13,7226	0,3164
13	14,2647	13,7268	0,3106
13,5	14,2585	13,7310	0,3047
14	14,2523	13,7352	0,2989
14,5	14,2461	13,7394	0,2930
15	14,2399	13,7436	0,2872
15,5	14,2337	13,7478	0,2814
16	14,2275	13,7520	0,2755
16,5	14,2213	13,7562	0,2697
17	14,2151	13,7604	0,2639
17,5	14,2089	13,7646	0,2580

18	14,2027	13,7688	0,2522
18,5	14,1965	13,7730	0,2463
19	14,1911	13,7772	0,2410
19,5	14,1902	13,7814	0,2381
20	14,1863	13,7856	0,2336
20,5	14,1832	13,7898	0,2294
21	14,1801	13,7940	0,2253
21,5	14,1769	13,7982	0,2212
22	14,1738	13,8024	0,2171
22,5	14,1707	13,8059	0,2134
23	14,1676	13,8099	0,2094
23,5	14,1644	13,8137	0,2055
24	14,1613	13,8175	0,2015
24,5	14,1582	13,8214	0,1976
25	14,1550	13,8252	0,1937
25,5	14,1519	13,8291	0,1898
26	14,1488	13,8329	0,1859
26,5	14,1457	13,8367	0,1820
27	14,1425	13,8406	0,1780
27,5	14,1394	13,8444	0,1741
28	14,1363	13,8483	0,1702
28,5	14,1332	13,8521	0,1663
29	14,1300	13,8559	0,1624
29,5	14,1269	13,8598	0,1584
30	14,1238	13,8636	0,1545
30,5	14,1206	13,8674	0,1506
31	14,1175	13,8713	0,1467
31,5	14,1144	13,8751	0,1428
32	14,1113	13,8790	0,1389
32,5	14,1081	13,8828	0,1349
33	14,1050	13,8866	0,1310
33,5	14,1019	13,8905	0,1271
34	14,0987	13,8943	0,1232
34,5	14,0956	13,8982	0,1193
35	14,0925	13,9020	0,1154
35,5	14,0894	13,9058	0,1114
36	14,0862	13,9097	0,1075
36,5	14,0831	13,9135	0,1036
37	14,0800	13,9173	0,0997
37,5	14,0768	13,9212	0,0958
38	14,0737	13,9250	0,0918
38,5	14,0706	13,9289	0,0879
39	14,0675	13,9327	0,0840
39,5	14,0643	13,9365	0,0801
40	14,0612	13,9404	0,0762

40,5	14,0581	13,9442	0,0723
41	14,0549	13,9480	0,0683
41,5	14,0518	13,9519	0,0644
42	14,0487	13,9557	0,0605
42,5	14,0456	13,9596	0,0566
43	14,0424	13,9634	0,0527
43,5	14,0393	13,9672	0,0488
44	14,0362	13,9711	0,0448
44,5	14,0330	13,9749	0,0409
45	14,0299	13,9788	0,0370
45,5	14,0268	13,9826	0,0331
46	14,0237	13,9864	0,0292
46,5	14,0215	13,9903	0,0258
47	14,0194	13,9941	0,0225
47,5	14,0183	13,9979	0,0197
48	14,0161	14,0018	0,0163
48,5	14,0110	14,0056	0,0113
49	14,0093	14,0035	0,0115
49,5	14,0060	14,0049	0,0088
50	14,0061	14,0052	0,0087
	Δv_{after} = **0,0009 V**		

The graphical illustrations of the equalisation process as plotted from the empirical data obtained in Table 4 are shown in figures 67 and 68.

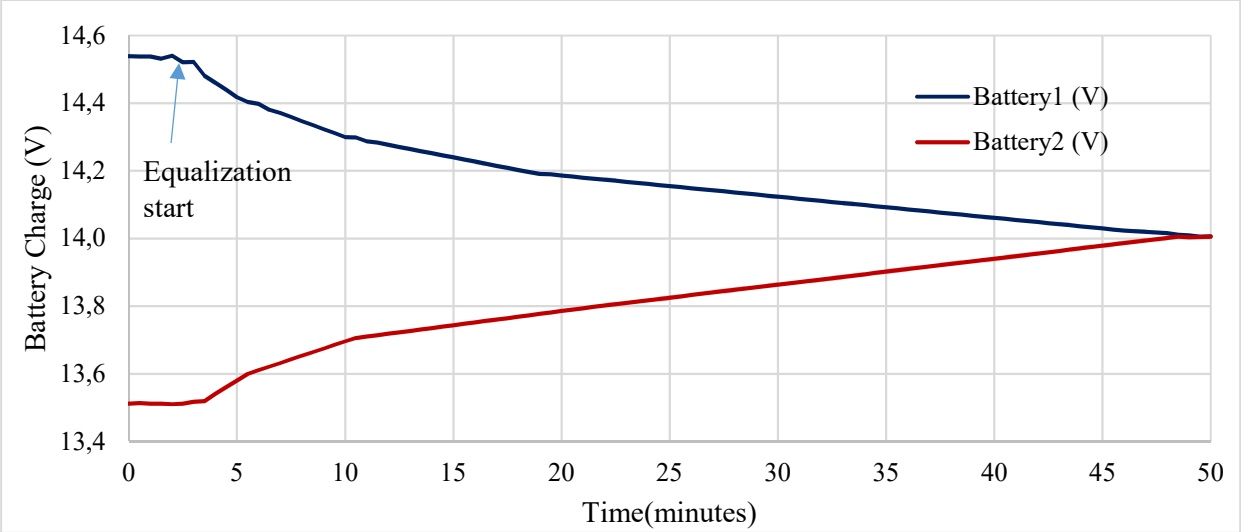


Figure 67: Equalisation tests plot of lead acid battery with charge imbalance

It took about 47 minutes for lead acid battery pair having approximately 1 V charge imbalance to reach equalisation.

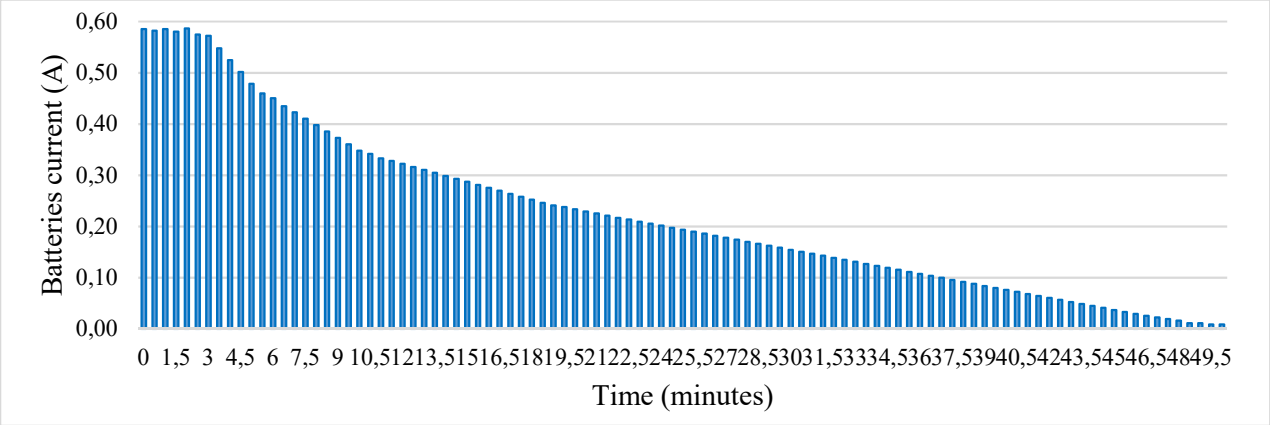


Figure 68: Current flow through lead acid battery string during equalisation

Figure 67 shows the current flow through the battery string tapering off as the equalisation process continues, while in Figure 69 the pulsating current flowing through the SC alternates at the switching frequency while tapering off as the charges were being equalised.

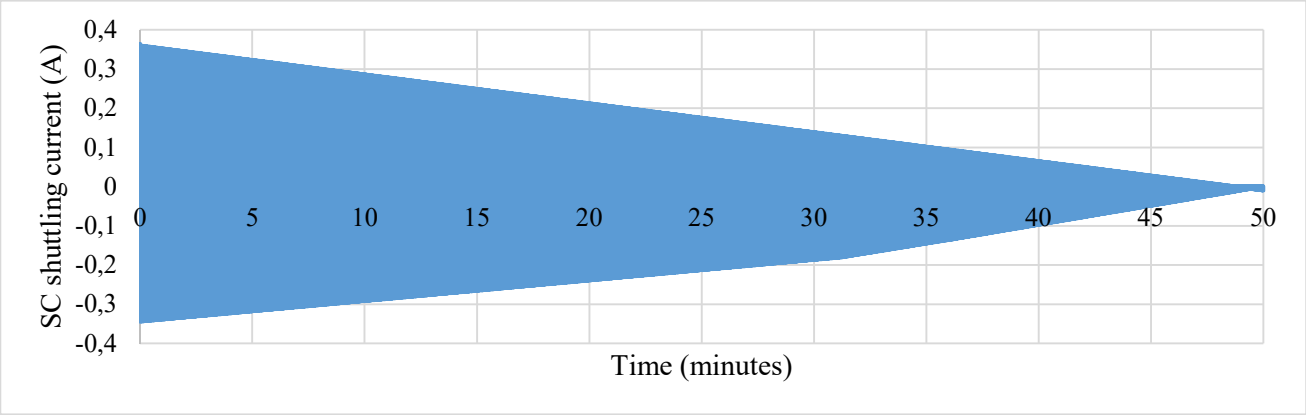


Figure 69: Current flow through switched capacitor (SC) during lead acid battery equalisation

- **SC design efficiency estimation**

According to review on SC systems for battery equalisation (Kobzev, 2000:57-59), the efficiency η of the energy transfer between two adjacent batteries with voltages V_{B1} and V_{B2} (when $V_{B1} < V_{B2}$) during charge equalisation can be calculated using the relation in the Equation 29.

$$\eta = \frac{P_1}{P_2} = \frac{V_{B1}}{V_{B2}} \tag{29}$$

Thus, for a pair of adjacent batteries in a series string, the efficiency in charge equalisation can be related to the percentage ratio of their charge imbalance before and after the equalisation process as given in Equation 30.

$$Efficiency(\eta)\% = \left(\frac{13.6 - \Delta v_{before}(V)}{13.6 - \Delta v_{after}(V)} \right) x100\% \tag{30}$$

The constant 13.6 is a typical float charging voltage of 12 V rated batteries and ΔV represents the charge imbalance among the batteries.

Thus, the efficiency of the design on lead acid battery can be given as a function of the charge imbalance equalised over a time period, calculated as:

$$\eta = \frac{13.6 - \Delta v_{before}(V)}{13.6 - \Delta v_{after}(V)} = \frac{(13.6 - 1.0273)V}{(13.6 - 0.0009)V} x100\% = 92.45\%$$

4.4.2 Equalisation test on silver calcium battery

The SC charge equaliser was tested on MIDAS gold SMF101 12 V 102 Ah silver calcium battery- a hybrid design of lead acid battery that can be used for deep cycle application purposes. Further details about the battery can be found in Annexure K.

The empirical data recorded from the BMS through the data loggers implemented are presented in Table 5. The highlighted values in the Table are the charge imbalance before (Δv_{before}) and after the equalisation has been completed (Δv_{after}).

Table 5: Equalisation tests results for silver calcium battery

Time (minutes)	Δv_{before} **= (0,4068 V)**		Batteries current (A)
	Battery1 (V)	Battery2 (V)	
0	14,2390	13,8322	0,3772
0,5	14,2394	13,8314	0,3784
1	14,2393	13,8324	0,3773
1,5	14,2389	13,8321	0,3772

2	14,2391	13,8285	0,3807
2,5	14,2382	13,8320	0,3766
3	14,2362	13,8313	0,3754
3,5	14,2337	13,8360	0,3688
4	14,2248	13,8407	0,3562
4,5	14,2191	13,8547	0,3379
5	14,2120	13,8622	0,3244
5,5	14,2025	13,8705	0,3078
6	14,1922	13,8832	0,2865
6,5	14,1822	13,8930	0,2682
7	14,1792	13,8947	0,2638
7,5	14,1675	13,9077	0,2409
8	14,1663	13,9029	0,2442
8,5	14,1599	13,9140	0,2280
9	14,1614	13,9109	0,2323
9,5	14,1600	13,9103	0,2315
10	14,1599	13,9225	0,2201
10,5	14,1507	13,9250	0,2093
11	14,1432	13,9327	0,1952
11,5	14,1457	13,9286	0,2013
12	14,1379	13,9317	0,1912
12,5	14,1355	13,9345	0,1864
13	14,1356	13,9361	0,1850
13,5	14,1338	13,9519	0,1687
14	14,1330	13,9535	0,1664
14,5	14,1323	13,9544	0,1650
15	14,1193	13,9567	0,1508
15,5	14,1136	13,9604	0,1420
16	14,1110	13,9616	0,1385
16,5	14,1098	13,9587	0,1401
17	14,1071	13,9597	0,1367
17,5	14,1029	13,9652	0,1277
18	14,1042	13,9647	0,1293
18,5	14,1024	13,9710	0,1218
19	14,1025	13,9728	0,1203
19,5	14,0984	13,9692	0,1198
20	14,0948	13,9752	0,1109
20,5	14,0893	13,9727	0,1081
21	14,0925	13,9760	0,1080
21,5	14,0891	13,9769	0,1040
22	14,0870	13,9805	0,0987
22,5	14,0831	13,9846	0,0913
23	14,0854	13,9857	0,0924
23,5	14,0843	13,9820	0,0949
24	14,0828	13,9830	0,0925
24,5	14,0861	13,9826	0,0960
25	14,0867	13,9846	0,0947
25,5	14,0865	13,9899	0,0896
26	14,0864	13,9929	0,0867

26,5	14,0818	13,9881	0,0869
27	14,0793	13,9909	0,0820
27,5	14,0855	13,9910	0,0876
28	14,0828	13,9912	0,0849
28,5	14,0755	13,9917	0,0777
29	14,0709	13,9938	0,0715
29,5	14,0709	13,9963	0,0692
30	14,0718	13,9981	0,0683
30,5	14,0734	13,9922	0,0753
31	14,0713	13,9935	0,0721
31,5	14,0666	14,0001	0,0617
32	14,0663	13,9955	0,0656
32,5	14,0665	13,9919	0,0692
33	14,0647	13,9937	0,0658
33,5	14,0617	13,9946	0,0622
34	14,0580	13,9961	0,0574
34,5	14,0569	13,9984	0,0542
35	14,0565	13,9964	0,0557
35,5	14,0546	13,9967	0,0537
36	14,0526	13,9967	0,0518
36,5	14,0503	13,9973	0,0491
37	14,0488	13,9989	0,0463
37,5	14,0494	13,9954	0,0501
38	14,0475	13,9949	0,0488
38,5	14,0455	13,9992	0,0429
39	14,0448	14,0014	0,0402
39,5	14,0448	14,0001	0,0414
40	14,0441	13,9974	0,0433
40,5	14,0449	13,9984	0,0431
41	14,0434	14,0006	0,0397
41,5	14,0450	13,9976	0,0439
42	14,0437	13,9976	0,0427
42,5	14,0427	14,0022	0,0375
43	14,0424	13,9990	0,0402
43,5	14,0419	14,0009	0,0380
44	14,0438	14,0008	0,0399
44,5	14,0412	14,0054	0,0332
45	14,0416	14,0023	0,0364
45,5	14,0419	14,0036	0,0355
46	14,0395	14,0034	0,0335
46,5	14,0396	14,0030	0,0339
47	14,0409	14,0047	0,0336
47,5	14,0402	14,0001	0,0372
48	14,0386	14,0073	0,0290
48,5	14,0387	14,0045	0,0317
49	14,0372	14,0050	0,0298
49,5	14,0371	14,0025	0,0321
50	14,0371	14,0051	0,0297
50,5	14,0359	14,0076	0,0262

51	14,0357	14,0052	0,0283
51,5	14,0362	14,0060	0,0280
52	14,0350	14,0057	0,0272
52,5	14,0375	14,0064	0,0288
53	14,0351	14,0069	0,0261
53,5	14,0325	14,0081	0,0226
54	14,0347	14,0083	0,0245
54,5	14,0344	14,0057	0,0266
55	14,0336	14,0082	0,0235
55,5	14,0347	14,0043	0,0282
56	14,0330	14,0065	0,0246
56,5	14,0302	14,0111	0,0177
57	14,0290	14,0122	0,0156
57,5	14,0296	14,0078	0,0202
58	14,0289	14,0109	0,0167
58,5	14,0278	14,0093	0,0171
59	14,0285	14,0096	0,0175
59,5	14,0276	14,0092	0,0171
60	14,0262	14,0090	0,0159
60,5	14,0250	14,0110	0,0130
61	14,0250	14,0109	0,0131
61,5	14,0243	14,0107	0,0126
62	14,0250	14,0089	0,0149
62,5	14,0250	14,0120	0,0120
63	14,0245	14,0112	0,0123
63,5	14,0236	14,0118	0,0109
64	14,0245	14,0111	0,0124
64,5	14,0249	14,0124	0,0116
65	14,0247	14,0118	0,0120
65,5	14,0240	14,0109	0,0121
66	14,0232	14,0110	0,0113
66,5	14,0224	14,0118	0,0098
67	14,0216	14,0110	0,0098
67,5	14,0207	14,0109	0,0091
68	14,0199	14,0108	0,0084
68,5	14,0191	14,0107	0,0078
69	14,0183	14,0106	0,0071
69,5	14,0175	14,0105	0,0064
70	14,0166	14,0104	0,0058
70,5	14,0158	14,0103	0,0051
71	14,0150	14,0102	0,0044
71,5	14,0142	14,0101	0,0038
72	14,0134	14,0100	0,0031
72,5	14,0125	14,0099	0,0024
73	14,0117	14,0098	0,0018
73,5	14,0109	14,0097	0,0011
74	14,0101	14,0096	0,0004
74,5	14,0093	14,0095	0,0009
	Δv_{after} **= 0,0002 V**		0,0005

The graphical illustrations of the equalisation process as plotted from the empirical data obtained in Table 5 are shown in figures 70 and 71.

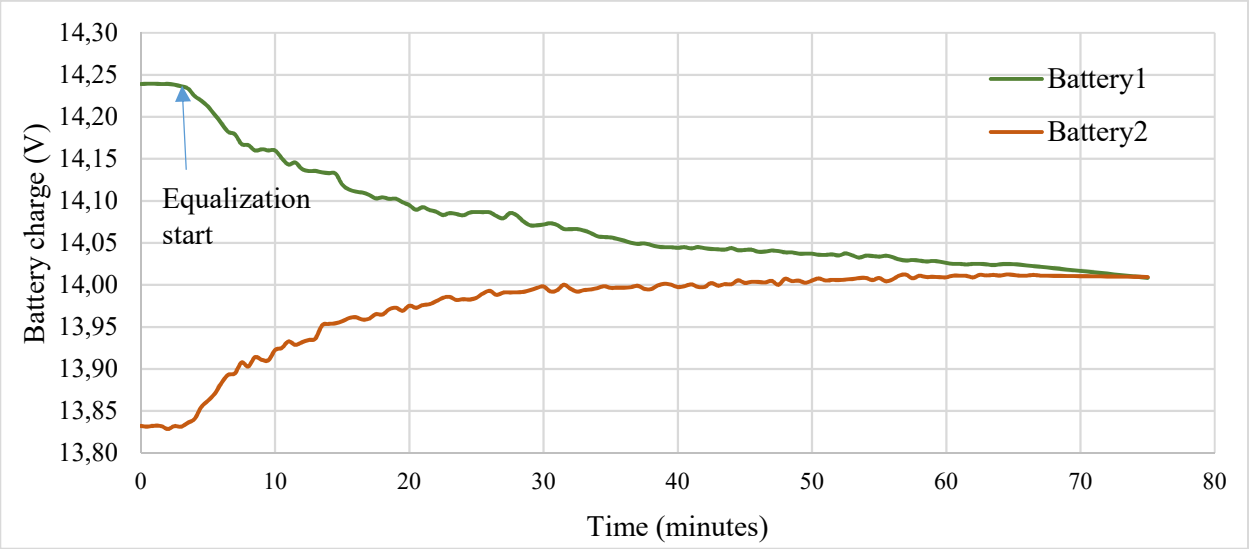


Figure 70: Equalisation tests plot of silver calcium battery with charge imbalance

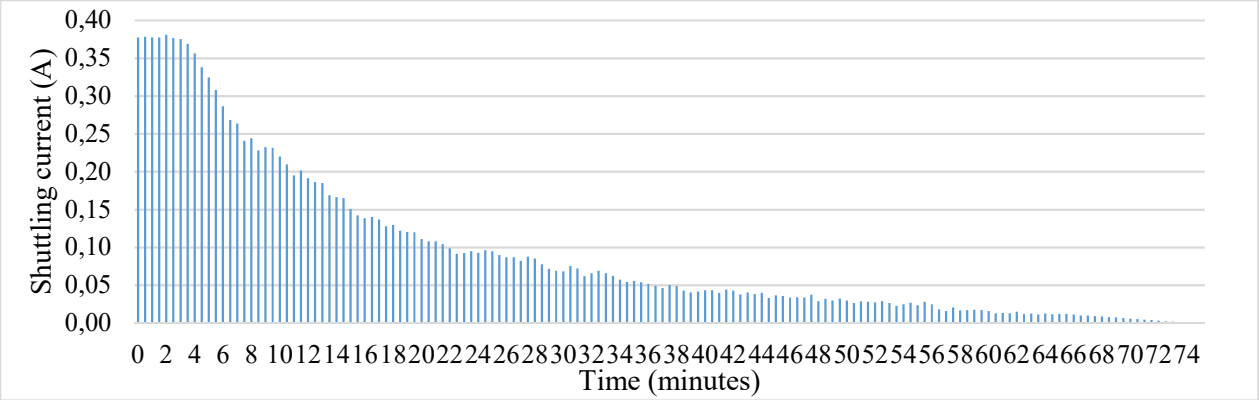


Figure 71: Current flow through silver calcium battery string during equalisation

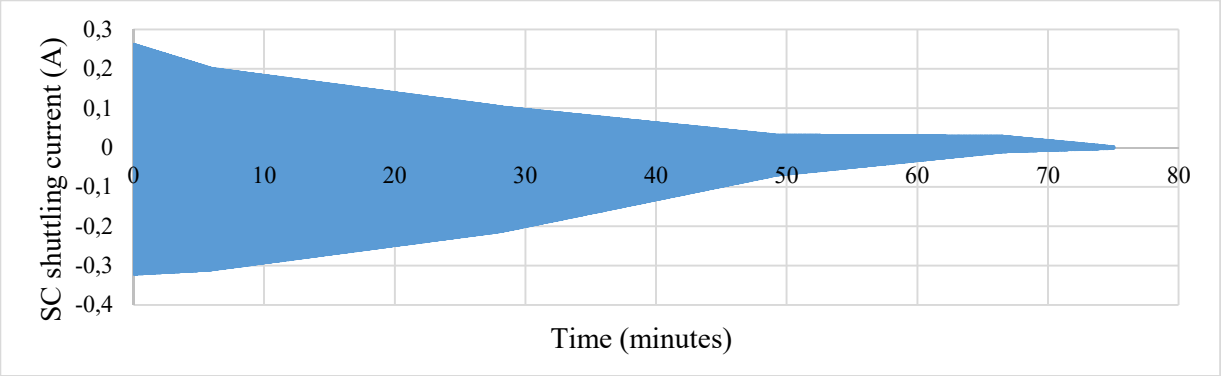


Figure 72: Current flow through switched capacitor (SC) during silver calcium battery equalisation

It took about 70 minutes to equalise 0.41 V charge imbalance among the selected silver calcium batteries. Figure 71 shows the current flow through the battery string tapering off as the equalisation process continues, while in Figure 72 the pulsating current flowing through the SC alternates at the switching frequency while tapering off as the charges were being equalised.

- **SC design efficiency estimation**

As similarly calculated in the analysis of lead acid battery, the efficiency of the design on silver calcium battery can be calculated as shown below:

$$\eta = \frac{13.6 - \Delta v_{before}\,(V)}{13.6 - \Delta v_{after}\,(V)} = \frac{(13.6 - 0.4046)V}{(13.6 - 0.0002)V} x100\% = 97.03\%$$

4.4.3 Equalisation test on lead calcium battery

The equalisation test was also evaluated on lead calcium battery. This battery is a modified form of silver calcium battery, consisting of similar liquid electrolyte as silver calcium but with a replacement of silver electrodes with lead such as in lead-acid batteries. Although, it is mostly used for automotive applications, it was used to further assess the performance evaluation of the designed charge equaliser since it is a deep-cycled battery. The battery model is DELTEC BD1250N 102Ah 12 V sealed lead calcium battery and more information about it is shown in its datasheet as included in the Annexure L of this study.

Table 6 shows the test results when the designed charge equaliser was tested on the battery pair. The charge imbalance before (Δv_{before}) and after the equalisation has been completed (Δv_{after}) as highlighted in the Table were recorded and analysed to determine the effectiveness of the system.

Table 6: Equalisation tests results for lead calcium battery

Time (minutes)	ΔV_{before} = (0,2857 V)		current (A)
	Battery1 (V)	Battery 2 (V)	
0	14,1582	13,8725	0,1779
0,5	14,1589	13,8706	0,1794
1	14,1588	13,8709	0,1792
1,5	14,1591	13,8728	0,1782
2	14,159	13,8733	0,1779
2,5	14,159	13,8726	0,1783
3	14,1476	13,8893	0,1611
3,5	14,1189	13,9258	0,1212
4	14,1035	13,9388	0,1038
4,5	14,0921	13,9553	0,0868
5	14,0837	13,9601	0,0787
5,5	14,0802	13,9601	0,0765
6	14,0726	13,9699	0,0659
6,5	14,0704	13,9759	0,0609
7	14,0629	13,9777	0,0552
7,5	14,0594	13,9858	0,0481
8	14,0514	13,9896	0,0409
8,5	14,0483	13,9922	0,0374
9	14,0454	13,9958	0,0334
9,5	14,0431	14,0006	0,0291
10	14,038	14,003	0,0245
10,5	14,0325	14,0097	0,0170
11	14,0284	14,0175	0,0097
11,5	14,0246	14,02	0,0059
12	14,0198	14,0248	0,0010
12,5	14,0199	14,0228	0,0013
	ΔV_{after} = 0,0029 V		

The graphical illustrations of the equalisation process as plotted from empirical data obtained in Table 6 are shown in figures 73 and 74.

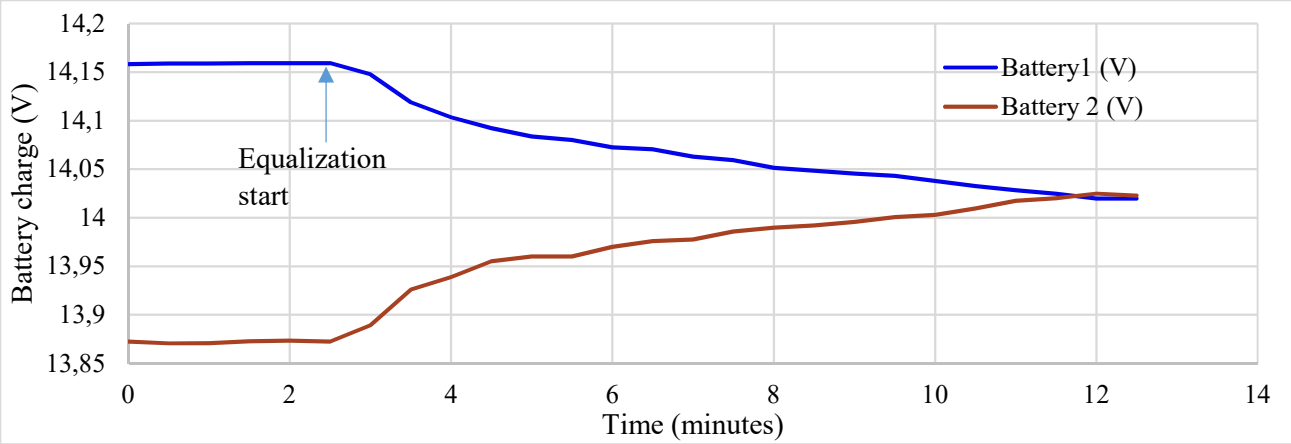


Figure 73: Equalisation tests plot of lead calcium battery with charge imbalance

It took about 10 minutes to equalise 0.29 V charge imbalance among the lead calcium battery.

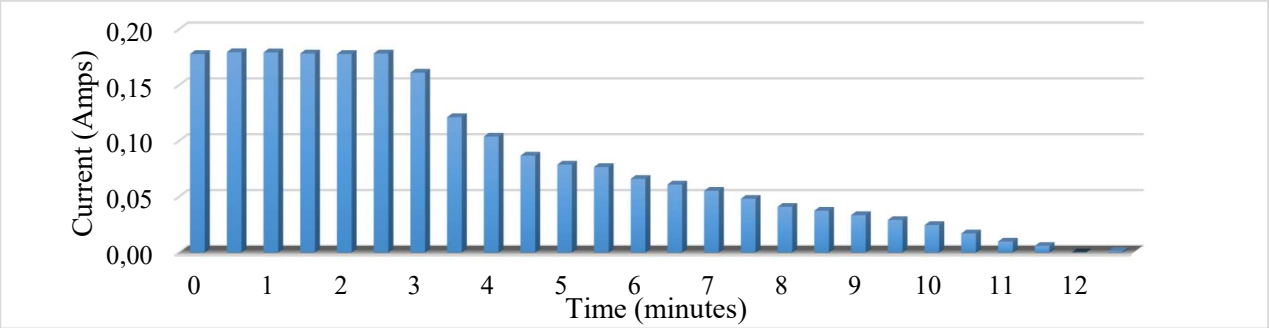


Figure 74: Current flow through lead calcium battery string during equalisation

Figure 74 shows the current flow through the battery string tapering off as the equalisation process continues, while in Figure 75 the pulsating current flowing through the SC alternates at the switching frequency while tapering off as the charges were being equalised.

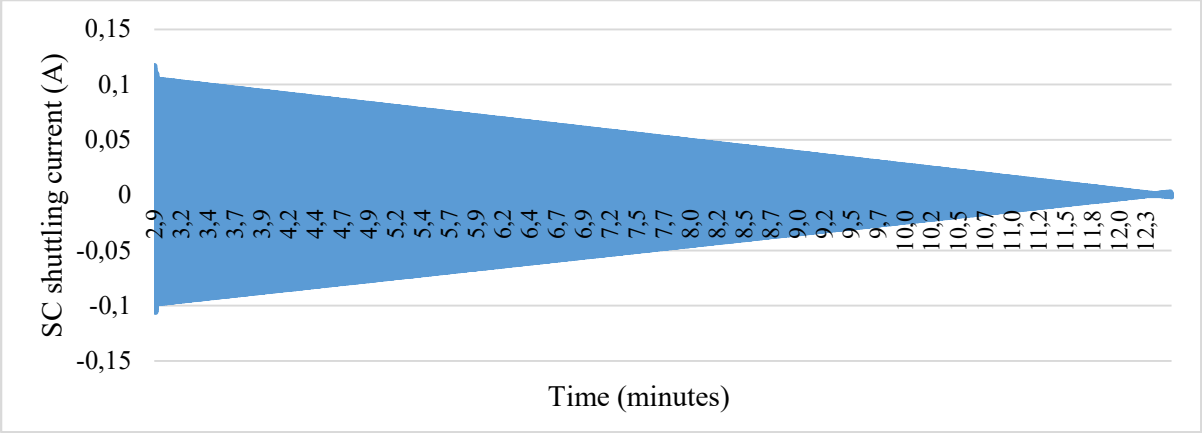


Figure 75: Current flow through switched capacitor (SC) during lead calcium battery equalisation

- **SC design efficiency estimation**

The efficiency of the design on lead calcium battery can be estimated as shown below:

$$\eta = \frac{13.6 - \Delta v_{before}\,(V)}{13.6 - \Delta v_{after}\,(V)} = \frac{(13.6 - 0.2857)V}{(13.6 - 0.0029)V} x100\% = 97.92\%$$

4.4.4 Equalisation test on lithium-ion battery

The designed battery charge equaliser was also evaluated on ZLI012018 12 V 16Ah lithium-ion phosphate ($LiFePO_4$) battery technology. This battery is an improved design of lithium-ion battery, which can be used in photovoltaic applications. Its datasheet is included in the Annexure M of this report. In Table 7, the empirical data obtained during the equalisation test on this battery type are shown with the highlighted values in the Table representing the charge imbalance before and after the equalisation.

Table 7: Equalisation tests results for lithium ion battery

Time (minutes)	ΔV_{before} = (0,299 V)		Batteries current (A)
	Battery1 (V)	Battery2 (V)	
0	13,6091	13,9081	0,1711
0,5	13,6089	13,9085	0,1715
1	13,6090	13,9084	0,1714
1,5	13,6089	13,9079	0,1711
2	13,6089	13,9081	0,1713
2,5	13,6088	13,9080	0,1713
3	13,6088	13,9069	0,1707
3,5	13,6087	13,9069	0,1707
4	13,6087	13,9067	0,1706
4,5	13,6086	13,8998	0,1667
5	13,6086	13,8969	0,1651
5,5	13,6089	13,8956	0,1641
6	13,6190	13,8951	0,1581
6,5	13,6290	13,8969	0,1534
7	13,6398	13,8985	0,1482
7,5	13,6498	13,8995	0,1431
8	13,6775	13,9022	0,1288
8,5	13,6918	13,9017	0,1204
9	13,7059	13,9016	0,1123
9,5	13,7201	13,9012	0,1040
10	13,7346	13,9009	0,0956
10,5	13,7387	13,9006	0,0931
11	13,7427	13,9003	0,0906
11,5	13,7455	13,9000	0,0889
12	13,7565	13,8997	0,0825
12,5	13,7598	13,8994	0,0804
13	13,7670	13,8991	0,0761
13,5	13,7697	13,8988	0,0744
14	13,7741	13,8985	0,0717
14,5	13,7760	13,8982	0,0705
15	13,7789	13,8979	0,0687
15,5	13,7798	13,8976	0,0680
16	13,7817	13,8973	0,0667
16,5	13,7836	13,8970	0,0655
17	13,7855	13,8967	0,0642
17,5	13,7874	13,8964	0,0630
18	13,7893	13,8961	0,0617
18,5	13,7912	13,8958	0,0605
19	13,7931	13,8955	0,0592
19,5	13,7950	13,8952	0,0580

20	13,7969	13,8949	0,0567
20,5	13,7988	13,8946	0,0555
21	13,8007	13,8943	0,0542
21,5	13,8026	13,8940	0,0530
22	13,8045	13,8937	0,0517
22,5	13,8064	13,8934	0,0505
23	13,8073	13,8931	0,0498
23,5	13,8102	13,8928	0,0479
24	13,8118	13,8925	0,0469
24,5	13,8137	13,8922	0,0456
25	13,8156	13,8919	0,0444
25,5	13,8175	13,8916	0,0431
26	13,8194	13,8913	0,0419
26,5	13,8213	13,8910	0,0406
27	13,8232	13,8907	0,0394
27,5	13,8251	13,8904	0,0381
28	13,8273	13,8901	0,0367
28,5	13,8292	13,8898	0,0354
29	13,8298	13,8898	0,0351
29,5	13,8313	13,8896	0,0341
30	13,8325	13,8894	0,0333
30,5	13,8338	13,8893	0,0325
31	13,8350	13,8891	0,0317
31,5	13,8363	13,8890	0,0309
32	13,8375	13,8879	0,0296
32,5	13,8388	13,8869	0,0283
33	13,8400	13,8858	0,0270
33,5	13,8413	13,8848	0,0257
34	13,8425	13,8837	0,0244
34,5	13,8425	13,8827	0,0238
35	13,8434	13,8816	0,0227
35,5	13,8440	13,8806	0,0217
36	13,8446	13,8795	0,0208
36,5	13,8453	13,8785	0,0198
37	13,8459	13,8775	0,0189
37,5	13,8465	13,8764	0,0179
38	13,8472	13,8754	0,0170
38,5	13,8478	13,8743	0,0160
39	13,8484	13,8733	0,0150
39,5	13,8491	13,8722	0,0141
40	13,8497	13,8712	0,0131
40,5	13,8503	13,8701	0,0122
41	13,8509	13,8691	0,0112
41,5	13,8516	13,8680	0,0103
42	13,8522	13,8670	0,0093

42,5	13,8528	13,8659	0,0084
43	13,8535	13,8649	0,0074
43,5	13,8541	13,8639	0,0065
44	13,8547	13,8628	0,0055
44,5	13,8554	13,8618	0,0045
45	13,8554	13,8607	0,0039
45,5	13,8554	13,8597	0,0033
46	13,8554	13,8586	0,0027
46,5	13,8555	13,8576	0,0021
47	13,8555	13,8565	0,0015
47,5	13,8555	13,8555	0,0009
	ΔV_{after} = 0 V		

The graphical representation of the equalisation data in Table 7 is shown in figures 76 and 77. The results shows that the equalisation of 0.29 V charge imbalance among the lithium ion battery pair was completed in about 44 minutes.

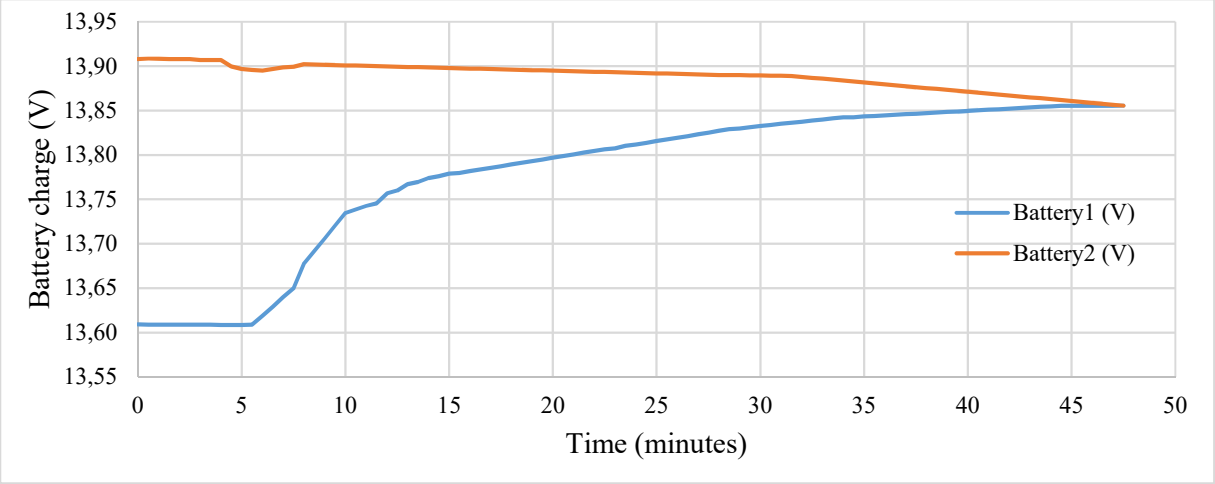


Figure 76: Equalisation tests plot of lithium ion battery with charge imbalance

The equalisation curve of lithium ion batteries displayed a unique pattern as compared to other battery types tested, showing almost constant voltage of one of the batteries. The discharge characteristics of LiFePo batteries are likely responsible for this as they have a very constant voltage curve over a wide capacity range.

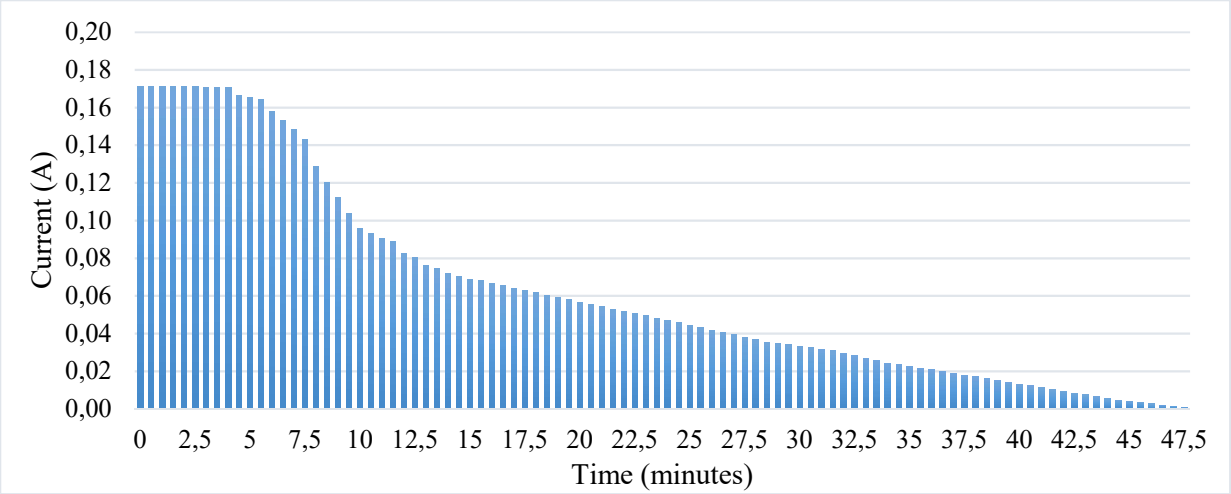


Figure 77: Current flow through lithium ion battery string during equalisation

In Figure 78, the pulsating current through the SC alternates at the switching frequency while tapering off as the charges were being equalised.

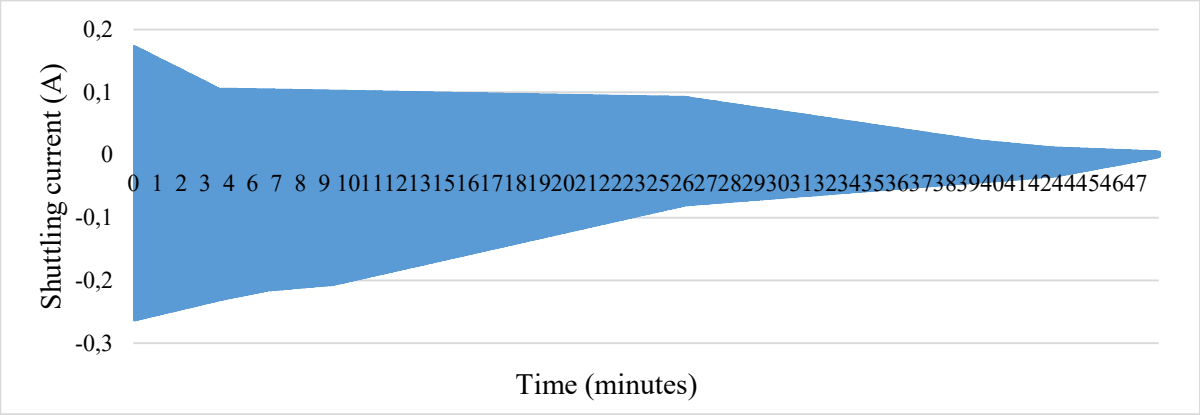


Figure 78: Current flow through switched capacitor (SC) during lithium ion battery equalisation

- **SC design efficiency estimation**

Like in the previous analyses, the efficiency of the design on lithium ion battery can be estimated as below:

$$\eta = \frac{13.6 - \Delta v_{before}\,(V)}{13.6 - \Delta v_{after}\,(V)} = \frac{(13.6 - 0.299)V}{(13.6 - 0.0009)V} x100\% = 97.80\%$$

4.5 SUMMARY OF THE DESIGN ANALYSES

A SC charge equaliser was designed, simulated and tested with different battery types used in stand-alone photovoltaic application. The design was done using simple control and switching strategy, which enable easy fabrication for local usage. The integration of the SC design with other real-time parameters measuring and monitoring devices form the proposed BMS in stand-alone photovoltaic application. To ascertain the performance of the system, the simulation results were compared with the oscilloscope measurements taken during operation of the designed SC circuit and both show some degrees of consistency in their graphical representations.

For analysis, the designed SC charge equaliser was applied and tested on battery strings in their float charging stage. At floating charging stage, especially when no load is connected to battery strings, charge imbalance among them becomes more evident and thus charge equalisation is often commonly applied at this stage. Some observations from the equalisation test results include the following: First, the equalisation current was observed to be proportional to the degree of charge imbalance among the tested battery pairs and this tapers off as the imbalance reduces during equalisation tests. Also, the equalisation time was not exactly consistent with charge imbalance ratio among the batteries as this varies from one battery type to the other.

The efficiency/ effectiveness of the design was evaluated with respect to the percentage ratio of the charge imbalance among the batteries before and after the charge equalisation process. The analysis shows a high performance efficiency of the SC circuit on the selected battery types.

CHAPTER 5: CONCLUSIONS, RECOMMENDATION AND RESEARCH OUTPUTS

5.1 INTRODUCTION

A BMS in stand-alone photovoltaic application was proposed and designed in this work. The system consists of a SC active charge equaliser, designed with a unique configuration of high capacitance and relatively low switching frequency, which can be applicable to common battery types used in stand-alone photovoltaic application. The BMS introduced a simple control strategy and less complicated circuit configuration process, which can allow an easy setup for local usage. The conclusions derived from the experimental setup, design structure and experimental analyses of the BMS system are presented in this chapter alongside some recommendations for future research work.

5.2 CONCLUSIONS

A SC battery charge equaliser was designed, tested and found applicable with some common battery types used in photovoltaic applications. The choice of SC technique was due to its simple control strategy and the possibility of application to different battery types, which allow its integration into a universal BMS. From reviews, charge equalisation at high frequency may expose batteries to current ripples, which could result in accelerated early degradation of the batteries. Thus, the SC equalisation circuit in this work was designed with high capacitance and low switching frequency. The circuit was mathematically optimised to minimise losses attributed to impulsive charging and tested with lead acid, silver calcium, lead calcium and lithium ion batteries being commonly used in stand-alone photovoltaic application. The SC design was verified by comparing its simulation results to the digital oscilloscope results and with both results showing similar values and graphs, the design configuration was validated.

In the design structure of the BMS, the output pulse signals from an astable multivibrator circuit were utilised to power two opto-couplers, which in turn control the alternation of the bootstrap capacitor circuits that drive the MOSFETs used for switching the equalisation capacitor among batteries. Data logging devices were introduced to record the equalisation parameters in the battery string and the SC circuit during the equalisation process. The analysis and evaluation of the system

performance show high efficiency, which was estimated based on the charge imbalance before and after the equalisation process was completed.

5.3 RECOMMENDATION

In this work, lithium ion and VRLA batteries, which are sealed rechargeable batteries with no liquid electrolytes, displayed uniform steady equalisation curve during their equalisation tests unlike others with liquid electrolytes, that is, silver calcium and calcium-calcium. Due to the electrochemical stability displayed by the lithium ion and VRLA batteries, which could improve their performance and SOH, they should be adopted more for use in stand-alone photovoltaic applications.

For future work, more investigation on the battery's step response due to pulse current at high frequency during charge equalisation is still required, especially on how this could affect a battery's SOH over a period of time.

5.4 RESEARCH OUTPUTS

From this research, three conference papers were produced and presented at peer reviewed and accredited conferences. Their references are highlighted below:

- OGUNNIYI, E. & PIENAAR, C. Inverse charge variation: Float charging effect on unbalanced battery strings in photovoltaic applications. *In:* Southern Africa Telecommunication Networks and Applications Conference (SATNAC), 2016, George,Western Cape, South Africa. 422-427.

- OGUNNIYI, E. & PIENAAR, C. Overview of Battery Energy Storage System Advancement for Renewable (Photovoltaic) Energy Applications. *In:* Domestic Use of Energy (DUE) - International Conference Towards sustainable energy solutions for the developing world, 3-5 April 2017 Cape Town, South Africa. 233-239.

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National Semiconductor

July 2006

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

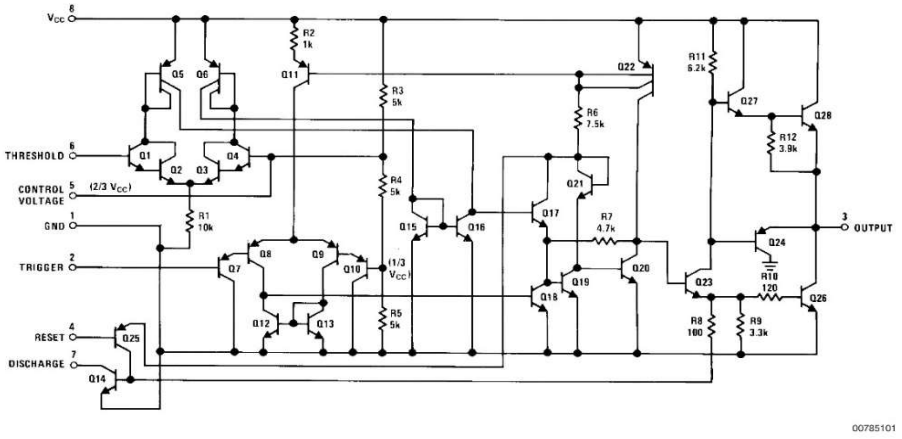
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



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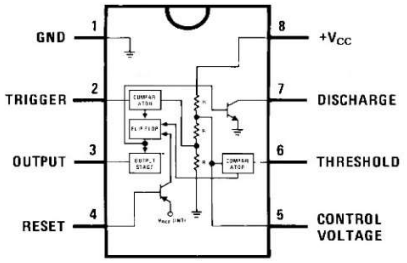
Connection Diagram

Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

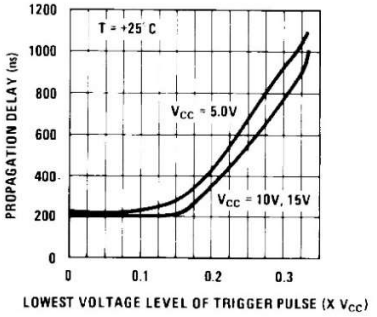
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics (Continued)

Output Propagation Delay vs.
Voltage Level of Trigger Pulse



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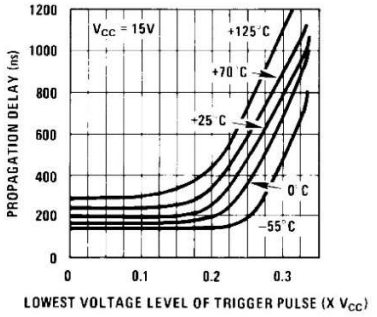
Output Propagation Delay vs.
Voltage Level of Trigger Pulse



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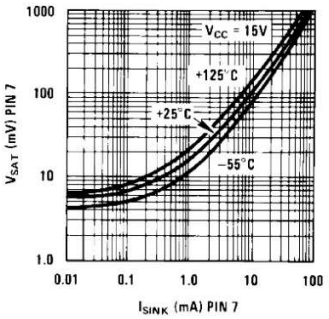
Discharge Transistor (Pin 7)
Voltage vs. Sink Current



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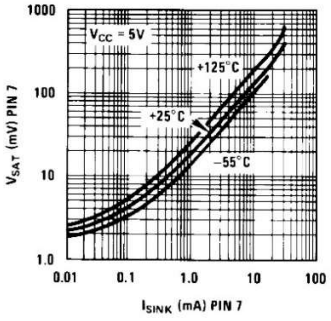
Discharge Transistor (Pin 7)
Voltage vs. Sink Current



00785127

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

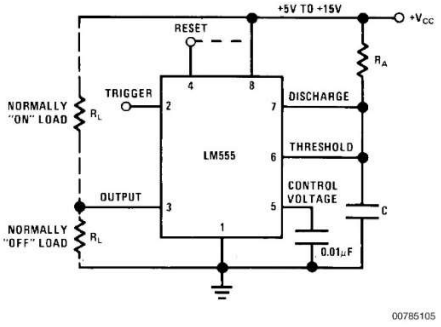
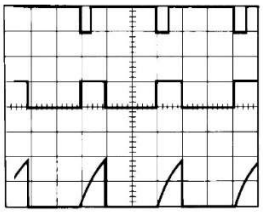


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

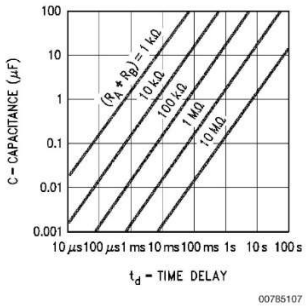


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

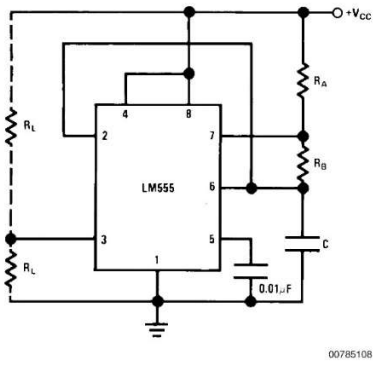
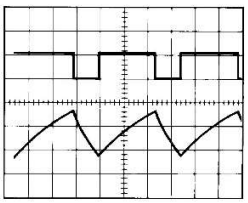


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



00785109

V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

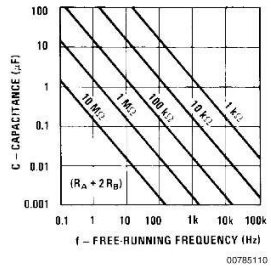
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

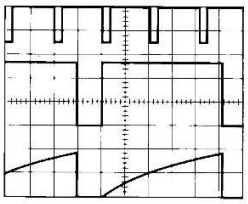


00785110

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



00785111

V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

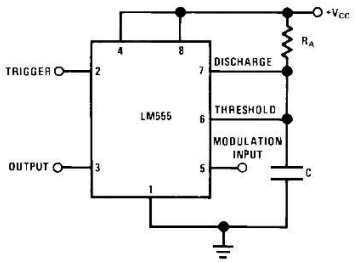


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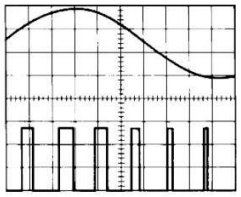
FIGURE 8. Pulse Width Modulator

Applications Information (Continued)



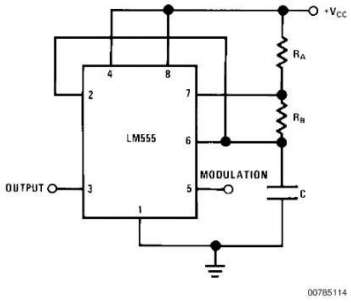
00785113

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01μF

FIGURE 9. Pulse Width Modulator

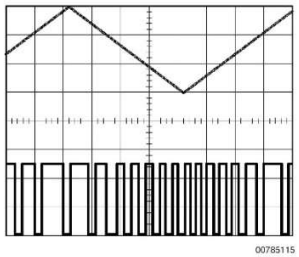
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



00785114

FIGURE 10. Pulse Position Modulator



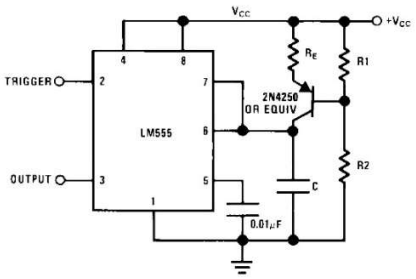
00785115

V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



00785116

FIGURE 12.

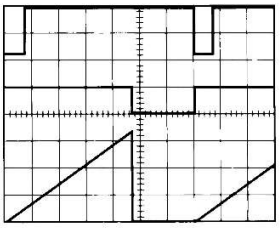
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$V_{BE} \cong 0.6V$

$V_{BE} \simeq 0.6V$

Applications Information (Continued)



00785117

V_{CC} = 5V
TIME = 20µs/DIV.
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

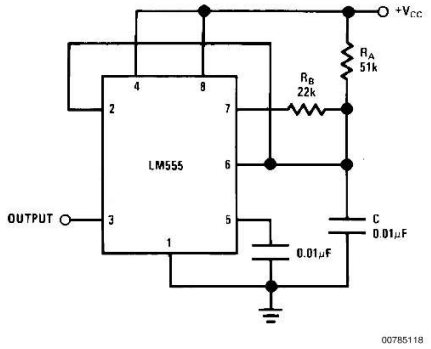
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14.* The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



00785118

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

UTC LM78XX LINEAR INTEGRATED CIRCUIT

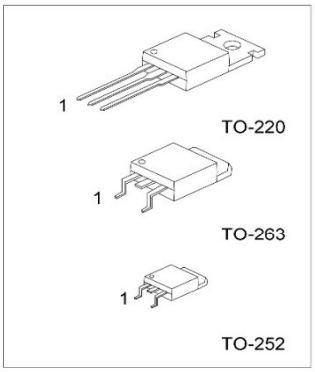
3-TERMINAL 1A POSITIVE VOLTAGE REGULATOR

DESCRIPTION

The UTC 78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

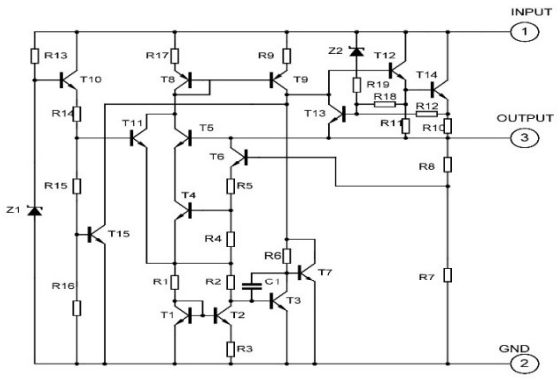
FEATURES

*Output current up to 1.5 A
*Fixed output voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V ,18V and 24V available
*Thermal overload shutdown protection
*Short circuit current limiting
*Output transistor SOA protection



1: Input 2: GND 3: Output

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified)

PARAMETER	SYMBOL	RATING		UNIT
Input voltage(for Vo=5~18V)	V_I		35	V
(for Vo=24V)			40	V
Output Current	I_O		1	A
Power Dissipation	PD	Internally	Limited	W
Operating Junction Temperature Range	T_{OPR}	-20	+150	°C
Storage Temperature Range	T_{STG}	-55	+150	°C

UTC LM7805 ELECTRICAL CHARACTERISTICS

(V_I=10V, I_O=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, I_O=5mA - 1.0A	4.80	5.0	5.20	V
		V_I =7.5V to 20V, I_O=5mA - 1.0A,PD<15W	4.75		5.25	V
Load Regulation	ΔVo	Tj=25°C,I_O=5mA - 1.5A			50	mV
		Tj=25°C,I_O=0.25A - 0.75A			25	mV
Line regulation	ΔVo	V_I =7V to 25V,Tj=25°C			50	mV
		V_I =7.5V to 20V,Tj=25°C,I_O=1A			50	mV
Quiescent Current	Iq	Tj=25°C, I_O=<1A			8.0	mA
Quiescent Current Change	Δlq	V_I =7.5V to 20V			1.0	mA
	Δlq	I_O=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		40		μV
Temperature coefficient of Vo	ΔVo/ΔT	I_O=5mA		-0.6		mV/°C
Ripple Rejection	RR	V_I =8V - 18V,f=120Hz,Tj=25°C	62	80		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	I_{SC}	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7806 ELECTRICAL CHARACTERISTICS

(V_I=11V, I_O=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, I_O=5mA - 1.0A	5.76	6.0	6.24	V
		V_I =8.5V to 21V, I_O=5mA - 1.0A, PD<15W	5.70		6.30	V
Load Regulation	ΔVo	Tj=25°C,I_O=5mA - 1.5A			60	mV
		Tj=25°C,I_O=0.25A - 0.75A			30	mV
Line regulation	ΔVo	V_I =8V to 25V,Tj=25°C			60	mV
		V_I =8.5V to 21V,Tj=25°C,I_O=1A			60	mV
Quiescent Current	Iq	Tj=25°C, I_O=<1A			8.0	mA
Quiescent Current Change	Δlq	V_I =8.5V to 21V			1.0	mA
	Δlq	I_O=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		45		μV
Temperature coefficient of Vo	ΔVo/ΔT	I_O=5mA		-0.7		mV/°C
Ripple Rejection	RR	V_I =9V - 19V,f=120Hz,Tj=25°C	59	75		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	I_{SC}	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7808 ELECTRICAL CHARACTERISTICS

(VI=14V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	7.68	8.0	8.32	V
		VI =10.5V to 23V, Io=5mA - 1.0A, PD<15W	7.60		8.40	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			80	mV
		Tj=25°C,Io=0.25A - 0.75A			40	mV
Line regulation	ΔVo	VI =10.5V to 25V,Tj=25°C			80	mV
		VI =10.5V to 23V,Tj=25°C,Io=1A			80	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =10.5V to 23V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-0.9		mV/°C
Ripple Rejection	RR	VI =11.5V to 21.5V, f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	I_{SC}	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7809 ELECTRICAL CHARACTERISTICS

(VI=15V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	8.64	9.0	9.36	V
		VI =11.5V to 24V, Io=5mA - 1.0A,PD<15W	8.55		9.45	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			90	mV
		Tj=25°C,Io=0.25A - 0.75A			45	mV
Line regulation	ΔVo	VI =11.5V to 25 V, Tj=25°C, PD<15W			90	mV
		VI =11.5V to 24V,Tj=25°C, Io<=1A			90	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =11.5V to 24V			1.0	mA
	ΔIq	Io=5mA – 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.1		mV/°C
Ripple Rejection	RR	VI =12.5V to 22.5V, f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	I_{SC}	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7810 ELECTRICAL CHARACTERISTICS

(VI=16V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, IO=5mA - 1.0A	9.60	10.0	10.40	V
		VI =12.5V to 25V, IO=5mA - 1.0A,PD<=15W	9.50		10.50	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			100	mV
		Tj=25°C,Io=0.25A - 0.75A			50	mV
Line regulation	ΔVo	VI =13V to 25V,Tj=25°C			100	mV
		VI =13V to 25V, Tj=25°C,Io<=1A			100	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =12.6V to 25V			1.0	mA
	ΔIq	IO=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.1		mV/°C
Ripple Rejection	RR	VI =13V - 23V,f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	IPK	Tj=25°C		1.8		A
Short-Circuit Current	ISC	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7812 ELECTRICAL CHARACTERISTICS

(VI=19V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, IO=5mA - 1.0A	11.52	12.0	12.48	V
		VI =14.5V to 27V, IO=5mA - 1.0A,PD<15W	11.40		12.60	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			120	mV
		Tj=25°C,Io=0.25A - 0.75A			60	mV
Line regulation	ΔVo	VI =14.5V to 30V,Tj=25°C			120	mV
		VI =14.6V to 27V,Tj=25°C, Io=1A			120	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =14.5V to 30V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		75		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.5		mV/°C
Ripple Rejection	RR	VI =15V - 25V,f=120Hz,Tj=25°C	55	72		dB
Peak Output Current	IPK	Tj=25°C		1.8		A
Short-Circuit Current	ISC	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7815 ELECTRICAL CHARACTERISTICS

(VI=23V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	14.40	15.0	15.60	V
		VI =17.5V to 30V, Io=5mA - 1.0A,PD<15W	14.25		15.75	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			150	mV
		Tj=25°C,Io=0.25A - 0.75A			75	mV
Line regulation	ΔVo	VI =18.5V to 30V,Tj=25°C			150	mV
		VI =17.7V to 30V, Tj=25°C, Io =1A			150	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =17.5V to 30V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		90		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.8		mV/°C
Ripple Rejection	RR	VI =18.5V to 28.5V f=120Hz,Tj=25°C	54	70		dB
Peak Output Current	IPK	Tj=25°C		1.8		A
Short-Circuit Current	ISC	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7818 ELECTRICAL CHARACTERISTICS

(VI=27V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	17.28	18.0	18.72	V
		VI =21V to 33V,Io=5mA - 1.0A	17.10		18.90	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			180	mV
		Tj=25°C,Io=0.25A - 0.75A			90	mV
Line regulation	ΔVo	VI =21V to 33V,Tj=25°C			180	mV
		VI =21V to 33V, Tj=25°C, Io =<1A,PD<15W			180	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =21.5V to 33V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		110		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-2.2		mV/°C
Ripple Rejection	RR	VI =22V - 32V,f=120Hz,Tj=25°C	53	69		dB
Peak Output Current	IPK	Tj=25°C		1.8		A
Short-Circuit Current	ISC	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7824 ELECTRICAL CHARACTERISTICS

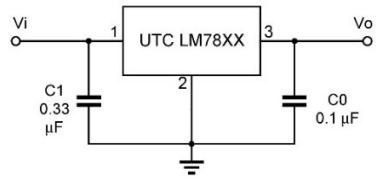
(VI=33V, Io=0.5A, Tj= 0°C - 12°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	23.04	24.0	24.96	V
		VI =27V to 38V,Io=5mA - 1.0A	22.80		25.20	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			240	mV
		Tj=25°C,Io=0.25A - 0.75A			120	mV
Line regulation	ΔVo	VI =27V to 38V,Tj=25°C			240	mV
		VI =27V to 38V,Tj=25°C,Io=1A			240	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =28V to 38V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		170		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-2.8		mV/°C
Ripple Rejection	RR	VI =28V - 38V,f=120Hz,Tj=25°C	50	66		dB
Peak Output Current	IPK	Tj=25°C		1.8		A
Short-Circuit Current	ISC	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

Note 1: The Maximum steady state usable output current are dependent on input voltage, heat sinking, lead length of the package and copper pattern of PCB. The data above represents pulse test conditions with junction temperatures specified at the initiation of test.

Note 2: Power dissipation<0.5W

APPLICATION CIRCUIT



Note 1: To specify an output voltage, substitute voltage value for "XX".

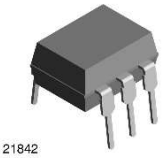
Note 2: Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulators.

VISHAY

4N35, 4N36, 4N37

Vishay Semiconductors

Optocoupler, Phototransistor Output, with Base Connection



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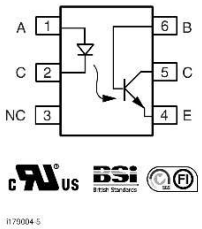


FEATURES

- Isolation test voltage 5000 V_{RMS}
- Interfaces with common logic families
- Input-output coupling capacitance < 0.5 pF
- Industry standard dual-in-line 6 pin package
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Pb-free

e3

RoHS COMPLIANT

APPLICATIONS

- AC mains detection
- Reed relay driving
- Switch mode power supply feedback
- Telephone ring detection
- Logic ground isolation
- Logic coupling with high frequency noise rejection

DESCRIPTION

Each optocoupler consists of gallium arsenide infrared LED and a silicon NPN phototransistor.

AGENCY APPROVALS

- Underwriters laboratory file no. E52744
- BSI: EN 60065:2002, EN 60950:2000
- FIMKO; EN 60065, EN 60335, EN 60950 certificate no. 25156

ORDER INFORMATION	
PART	**REMARKS**
4N35	CTR > 100 %, DIP-6
4N36	CTR > 100 %, DIP-6
4N37	CTR > 100 %, DIP-6

ABSOLUTE MAXIMUM RATINGS (1)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
INPUT				
Reverse voltage		V_R	6	V
Forward current		I_F	50	mA
Surge current	t ≤ 10 µs	I_{FSM}	1	A
Power dissipation		P_{diss}	70	mW
OUTPUT				
Collector emitter breakdown voltage		V_{CEO}	70	V
Emitter base breakdown voltage		V_{EBO}	7	V
Collector current		I_C	50	mA
	t ≤ 1 ms	I_C	100	mA
Power dissipation		P_{diss}	70	mW
COUPLER				
Isolation test voltage		V_{ISO}	5000	V_{RMS}
Creepage			≥ 7	mm
Clearance			≥ 7	mm
Isolation thickness between emitter and detector			≥ 0.4	mm

ABSOLUTE MAXIMUM RATINGS (1)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
COUPLER				
Comparative tracking index	DIN IEC 112/VDE 0303, part 1		175	
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}	Ω
Storage temperature		T_{stg}	- 55 to + 150	°C
Operating temperature		T_{amb}	- 55 to + 100	°C
Junction temperature		T_j	100	°C
Soldering temperature (2)	max.10 s dip soldering: distance to seating plane ≥ 1.5 mm	T_{sld}	260	°C

Notes

(1) T_{amb} = 25 °C, unless otherwise specified.
Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

(2) Refer to wave profile for soldering condditions for through hole devices (DIP).

ELECTRICAL CHARACTERISTICS (1)							
PARAMETER	**TEST CONDITION**	**PART**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
INPUT							
Junction capacitance	V_R = 0 V, f = 1 MHz		C_j		50		pF
Forward voltage (2)	I_F = 10 mA		V_F		1.3	1.5	V
	I_F = 10 mA, T_{amb} = - 55 °C		V_F	0.9	1.3	1.7	V
Reverse current (2)	V_R = 6 V		I_R		0.1	10	µA
Capacitance	V_R = 0 V, f = 1 MHz		C_O		25		pF
OUTPUT							
Collector emitter breakdown voltage(2)	I_C = 1 mA	4N35	BV_{CEO}	30			V
		4N36	BV_{CEO}	30			V
		4N37	BV_{CEO}	30			V
Emitter collector breakdown voltage(2)	I_E = 100 µA		BV_{ECO}	7			V
OUTPUT							
Collector base breakdown voltage (2)	I_C = 100 µA, I_B = 1 µA	4N35	BV_{CBO}	70			V
		4N36	BV_{CBO}	70			V
		4N37	BV_{CBO}	70			V
Collector emitter leakage current (2)	V_{CE} = 10 V, I_F = 0	4N35	I_{CEO}		5	50	nA
		4N36	I_{CEO}		5	50	nA
	V_{CE} = 10 V, I_F = 0	4N37	I_{CEO}		5	50	nA
	V_{CE} = 30 V, I_F = 0, T_{amb} = 100 °C	4N35	I_{CEO}			500	µA
		4N36	I_{CEO}			500	µA
		4N37	I_{CEO}			500	µA
Collector emitter capacitance	V_{CE} = 0		C_{CE}		6		pF
COUPLER							
Resistance, input output (2)	V_{IO} = 500 V		R_{IO}	10^{11}			Ω
Capacitance, input output	f = 1 MHz		C_{IO}		0.6		pF

Notes

(1) T_{amb} = 25 °C, unless otherwise specified.
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

(2) Indicates JEDEC registered value.

CURRENT TRANSFER RATIO							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN	TYP.	MAX	UNIT
DC current transfer ratio (1)	V_{CE} = 10 V, I_F = 10 mA	4N35	CTR_{DC}	100			%
		4N36	CTR_{DC}	100			%
		4N37	CTR_{DC}	100			%
	V_{CE} = 10 V, I_F = 10 mA, T_A = - 55 °C to + 100 °C	4N35	CTR_{DC}	40	50		%
		4N36	CTR_{DC}	40	50		%
		4N37	CTR_{DC}	40	50		%

Note
(1) Indicates JEDEC registered values.

SWITCHING CHARACTERISTICS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Switching time (1)	V_{CC} = 10 V, I_C = 2 mA, R_L = 100 Ω	t_{on}, t_{off}		10		µs

Note
(1) Indicates JEDEC registered values.

TYPICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specied

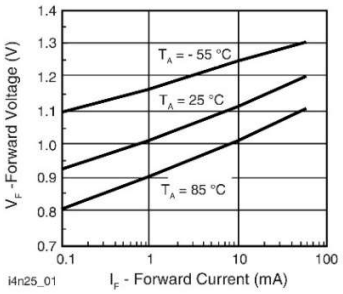


Fig. 1 - Forward Voltage vs. Forward Current

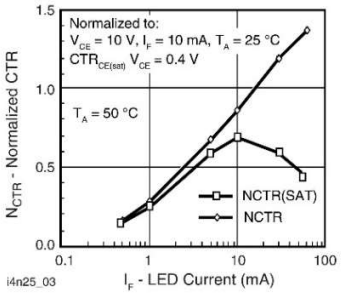


Fig. 3 - Normalized Non-Saturated and Saturated CTR vs. LED Current

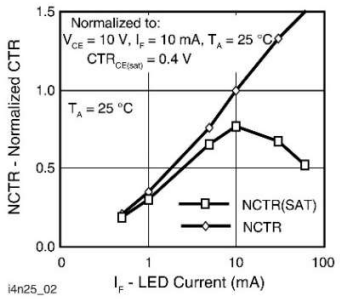


Fig. 2 - Normalized Non-Saturated and Saturated CTR vs. LED Current

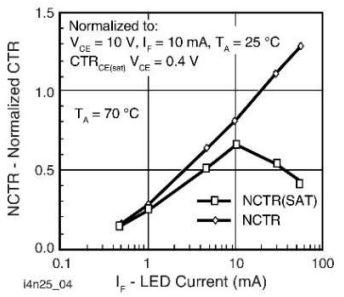


Fig. 4 - Normalized Non-Saturated and Saturated CTR vs. LED Current

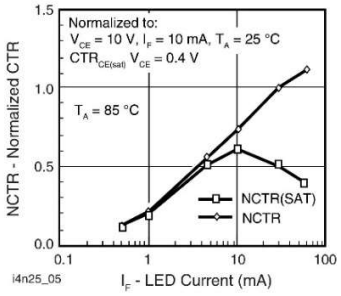


Fig. 5 - Normalized Non-Saturated and Saturated CTR vs. LED Current

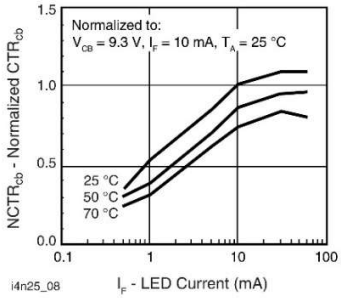


Fig. 8 - Normalized CTR_{cb} vs. LED Current and Temperature

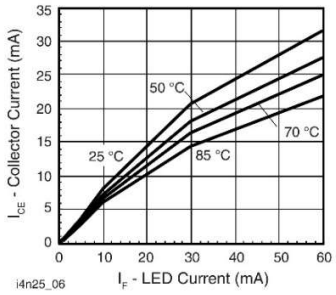


Fig. 6 - Collector Emitter Current vs. Temperature and LED Current

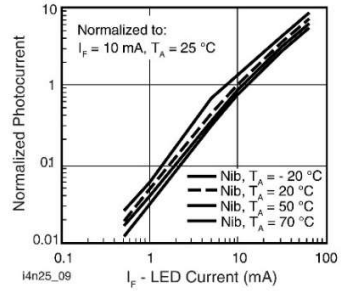


Fig. 9 - Normalized Photocurrent vs. I_F and Temperature

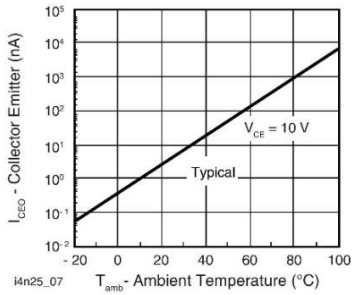


Fig. 7 - Collector Emitter Leakage Current vs. Temperature

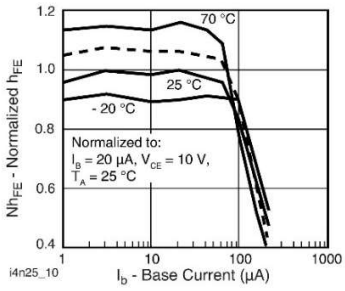


Fig. 10 - Normalized Non-Saturated h_{FE} vs. Base Current and Temperature

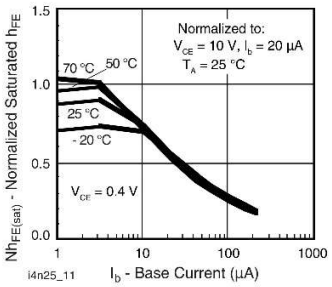


Fig. 11 - Normalized h_{FE} vs. Base Current and Temperature

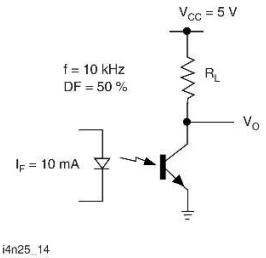


Fig. 14 - Switching Schematic

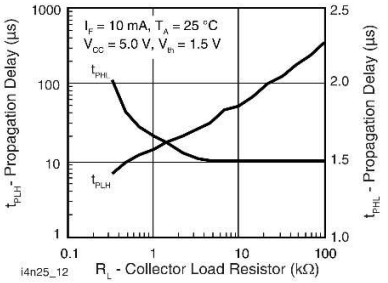


Fig. 12 - Propagation Delay vs. Collector Load Resistor

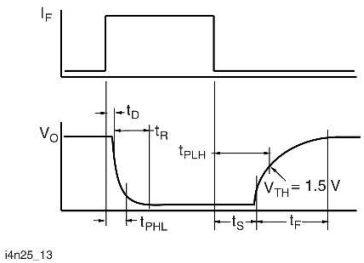
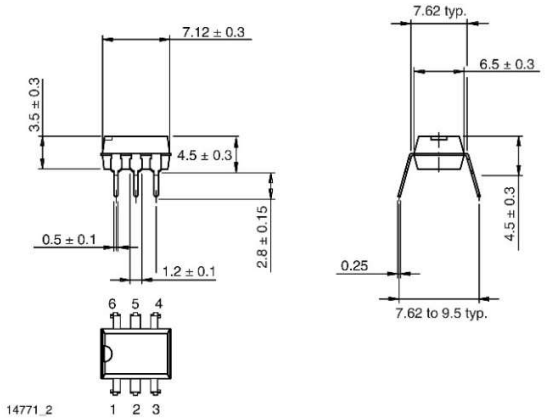
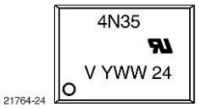


Fig. 13 - Switching Timing

PACKAGE DIMENSIONS in millimeters



PACKAGE MARKING



FAIRCHILD SEMICONDUCTOR®

QFET®

FQPF11P06

FQPF11P06

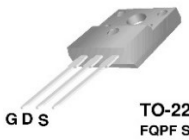
60V P-Channel MOSFET

General Description

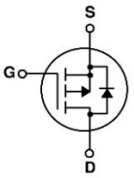
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

Features

- -8.6A, -60V, $R_{DS(on)}$ = 0.175Ω @V_{GS} = -10 V
- Low gate charge (typical 13 nC)
- Low Crss (typical 45 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



TO-220F
FQPF Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQPF11P06	Units
V_{DSS}	Drain-Source Voltage		-60	V
I_D	Drain Current - Continuous (T_C = 25°C)		-8.6	A
	- Continuous (T_C = 100°C)		-6.08	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-34.4	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	160	mJ
I_{AR}	Avalanche Current	(Note 1)	-8.6	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		30	W
	- Derate above 25°C		0.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Rev. B4, March 2004

Elerical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C	--	-0.07	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V	--	--	-1	µA
		V_{DS} = -48 V, T_C = 150°C	--	--	-10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -4.3 A	--	0.14	0.175	Ω
g_{FS}	Forward Transconductance	V_{DS} = -30 V, I_D = -4.3 A (Note 4)	--	4.75	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	420	550	pF
C_{oss}	Output Capacitance		--	195	250	pF
C_{rss}	Reverse Transfer Capacitance		--	45	60	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -5.7 A, R_G = 25 Ω (Note 4, 5)	--	6.5	25	ns
t_r	Turn-On Rise Time		--	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	15	40	ns
t_f	Turn-Off Fall Time		--	45	100	ns
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -11.4 A, V_{GS} = -10 V (Note 4, 5)	--	13	17	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	6.3	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-8.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-34.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -8.6 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -11.4 A, dI_F / dt = 100 A/µs (Note 4)	--	83	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.26	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 2.5mH, I_{AS} = -8.6A, V_{DD} = -25V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -11.4A, di/dt ≤ 300A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

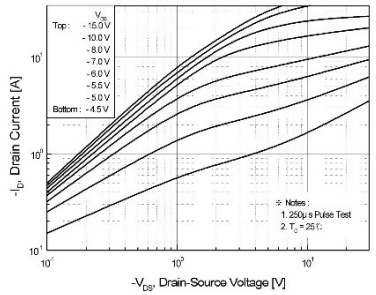


Figure 1. On-Region Characteristics

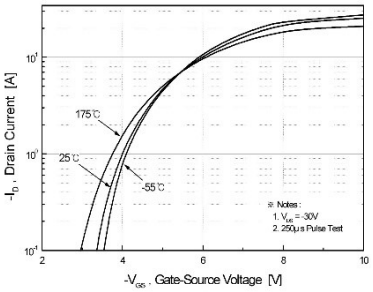


Figure 2. Transfer Characteristics

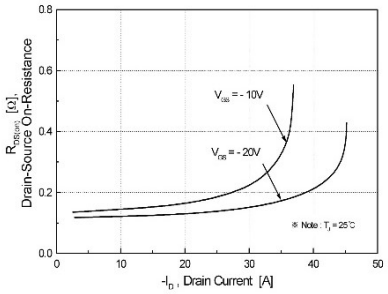


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

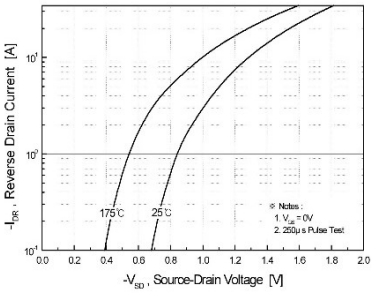


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

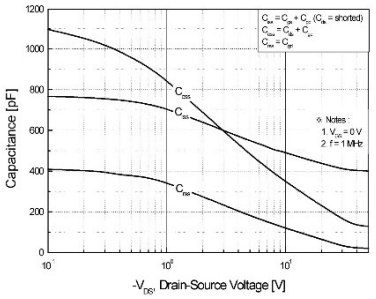


Figure 5. Capacitance Characteristics

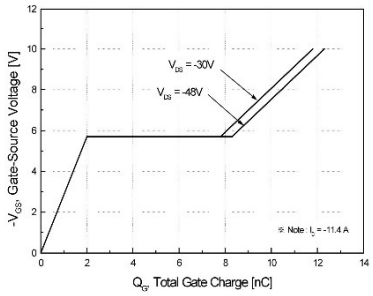


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

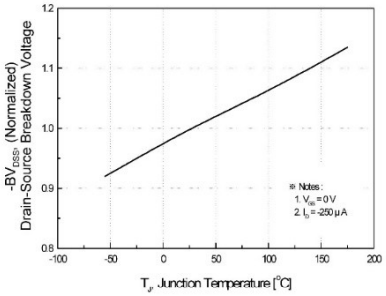


Figure 7. Breakdown Voltage Variation vs. Temperature

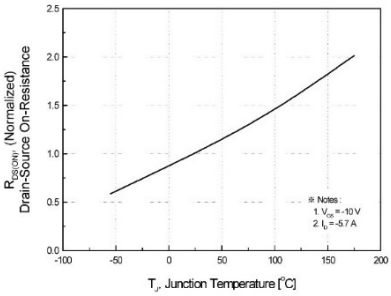


Figure 8. On-Resistance Variation vs. Temperature

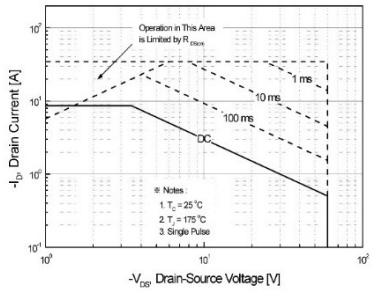


Figure 9. Maximum Safe Operating Area

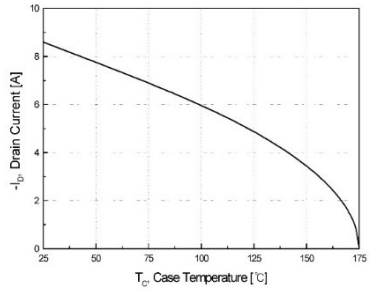


Figure 10. Maximum Drain Current vs. Case Temperature

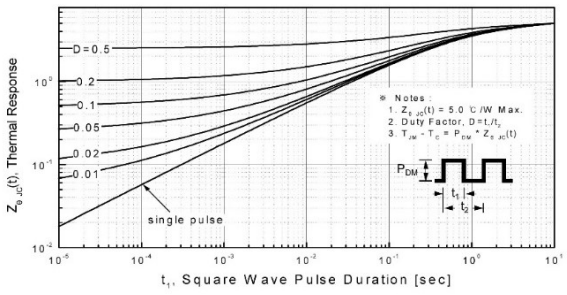
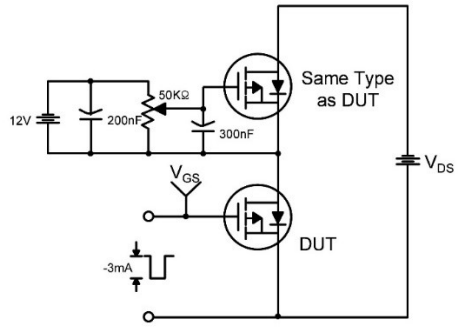
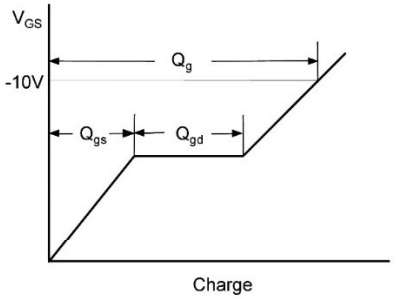


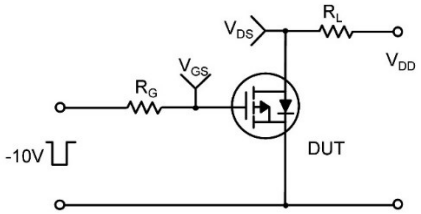
Figure 11. Transient Thermal Response Curve

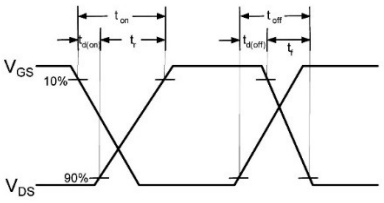
Gate Charge Test Circuit & Waveform



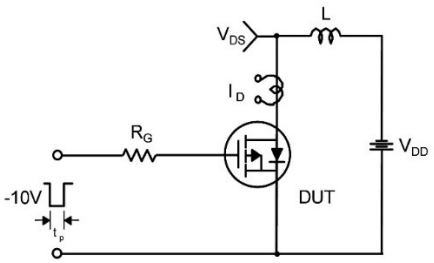


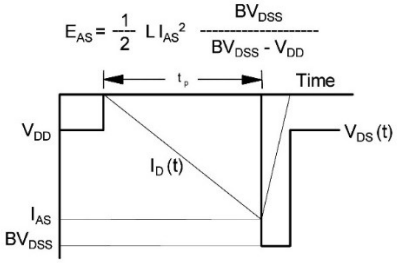
Resistive Switching Test Circuit & Waveforms



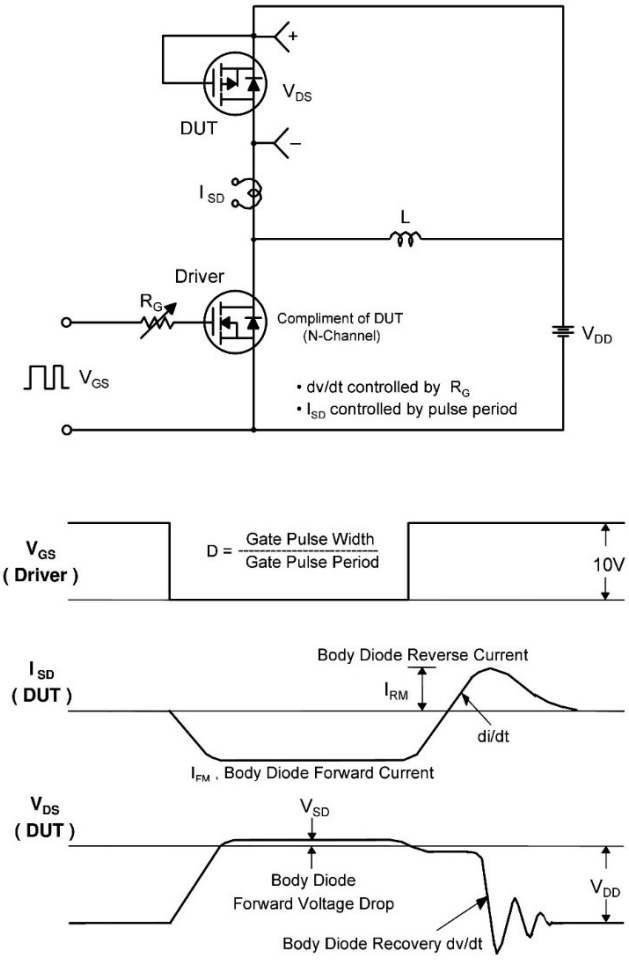


Unclamped Inductive Switching Test Circuit & Waveforms



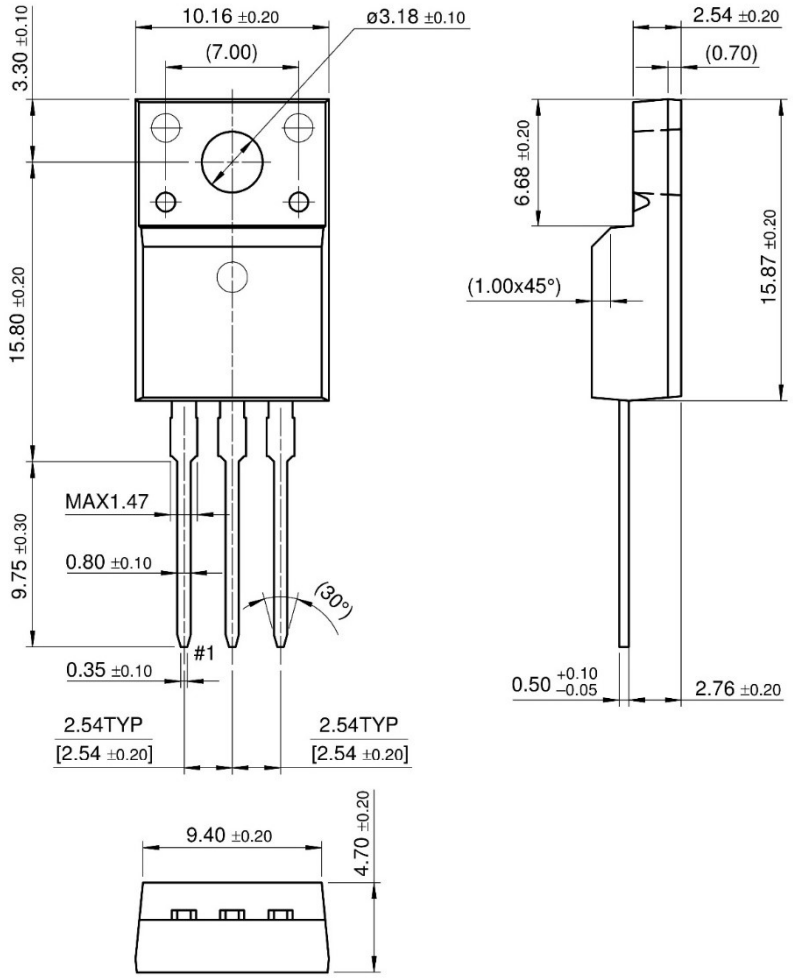


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220F



Dimensions in Millimeters

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CoolFET™	FPS™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET®	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E²CMOS™	HiSeC™	MSXPro™	Quiet Series™	TINYOPTO™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I9

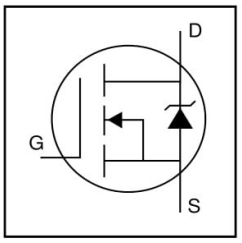
International
IOR Rectifier

PD - 9.1498A

IRLIZ44N

HEXFET® Power MOSFET

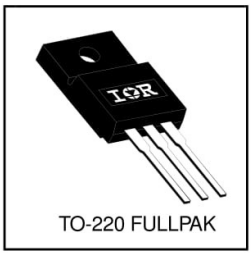
- Logic-Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated



V_{DSS} = 55V

$R_{DS(on)}$ = 0.022Ω

I_D = 30A



TO-220 FULLPAK

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	22	
I_{DM}	Pulsed Drain Current ①⑥	160	
P_D @T_C = 25°C	Power Dissipation	45	W
	Linear Derating Factor	0.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②⑥	210	mJ
I_{AR}	Avalanche Current①⑥	25	A
E_{AR}	Repetitive Avalanche Energy①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.070	—	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.022	Ω	V_{GS} = 10V, I_D = 17A ④
		—	—	0.025		V_{GS} = 5.0V, I_D = 17A ④
		—	—	0.035		V_{GS} = 4.0V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	21	—	—	S	V_{DS} = 25V, I_D = 25A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	48	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	—	—	8.6		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	25		V_{GS} = 5.0V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 28V
t_r	Rise Time	—	84	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	26	—		R_G = 3.4Ω, V_{GS} = 5.0V
t_f	Fall Time		15			R_D = 1.1Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1700	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	400	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 17A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	80	120	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse RecoveryCharge	—	210	320	µC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 15V, starting T_J = 25°C, L = 470µH R_G = 25Ω, I_{AS} = 25A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 270A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ t=60s, f=60Hz

⑥ Uses IRLZ44N data and test conditions

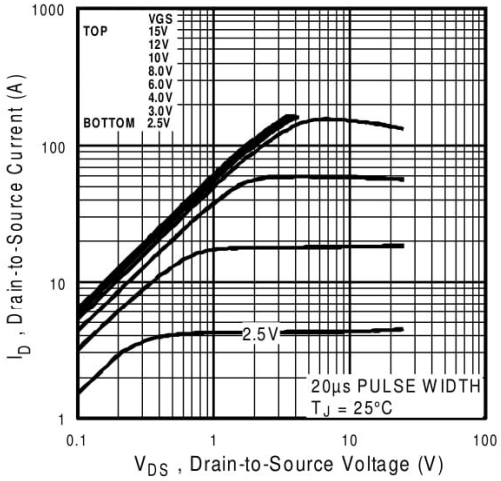


Fig 1. Typical Output Characteristics

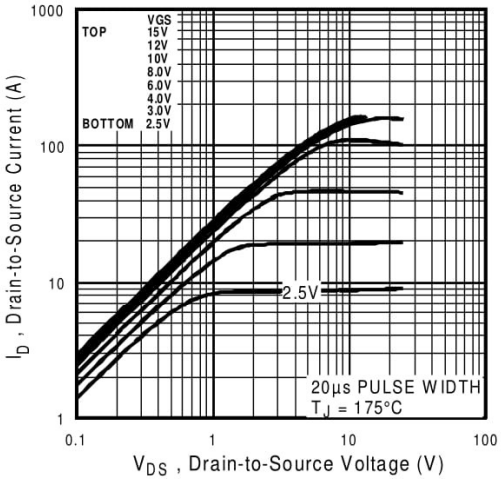


Fig 2. Typical Output Characteristics

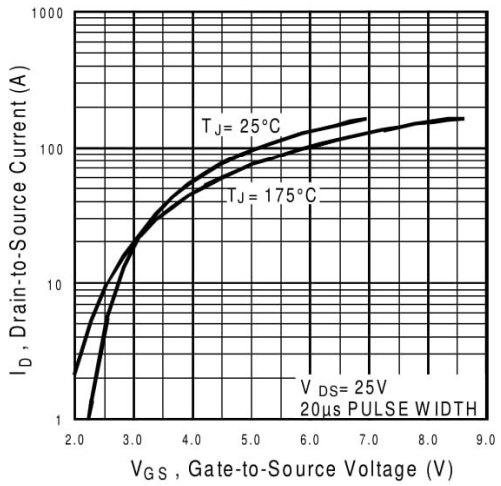


Fig 3. Typical Transfer Characteristics

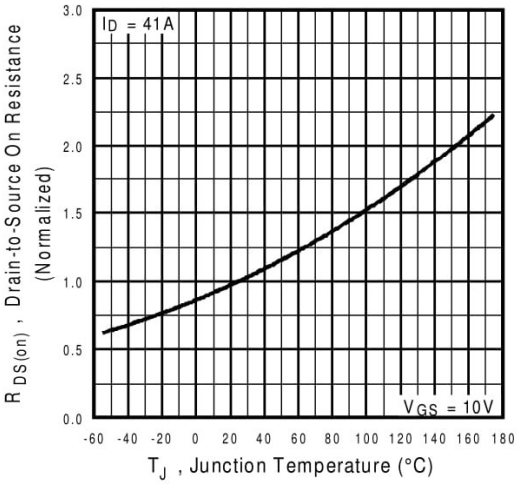


Fig 4. Normalized On-Resistance Vs. Temperature

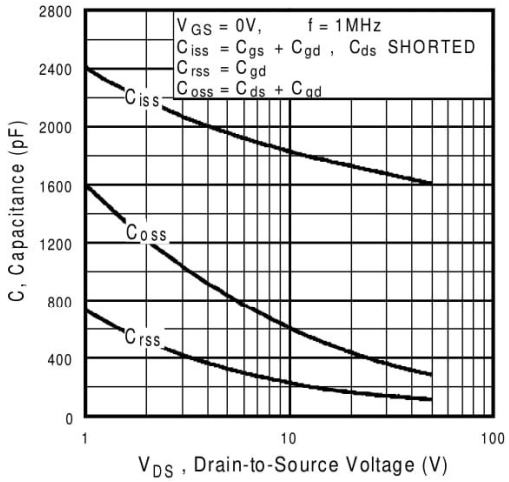


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

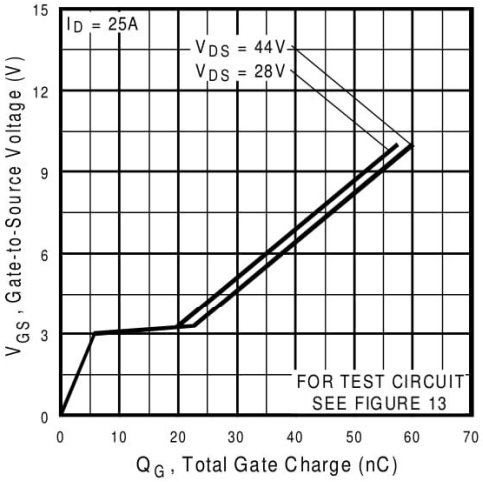


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

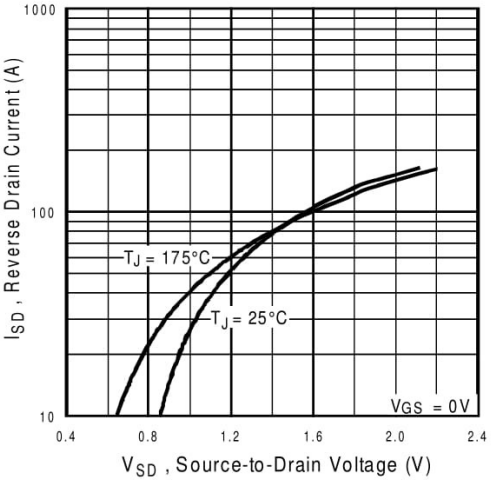


Fig 7. Typical Source-Drain Diode Forward Voltage

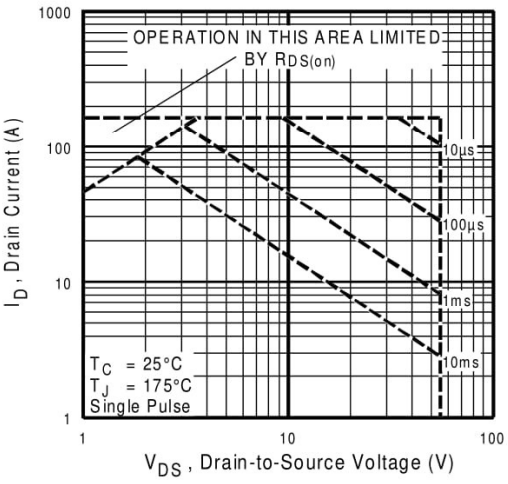


Fig 8. Maximum Safe Operating Area

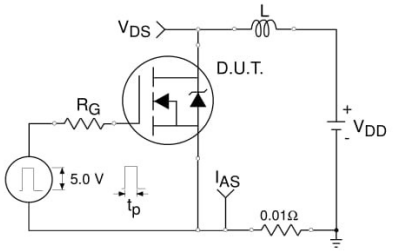


Fig 12a. Unclamped Inductive Test Circuit

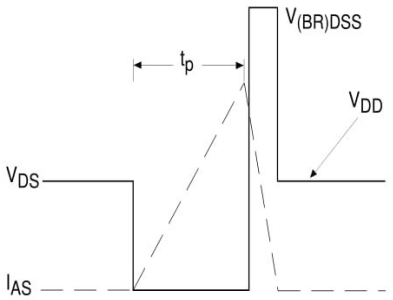


Fig 12b. Unclamped Inductive Waveforms

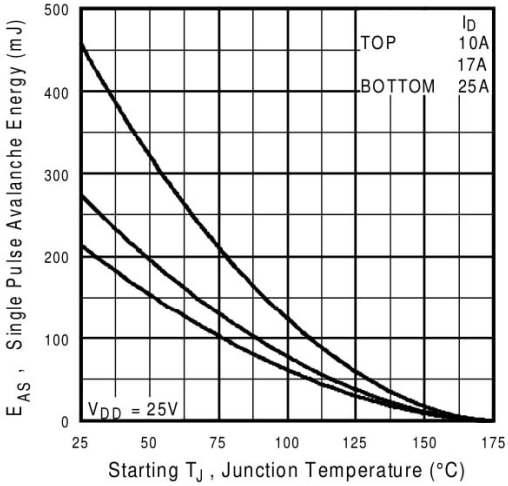


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

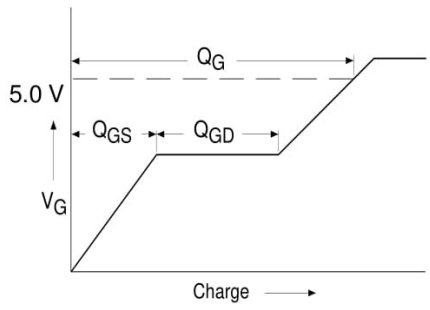


Fig 13a. Basic Gate Charge Waveform

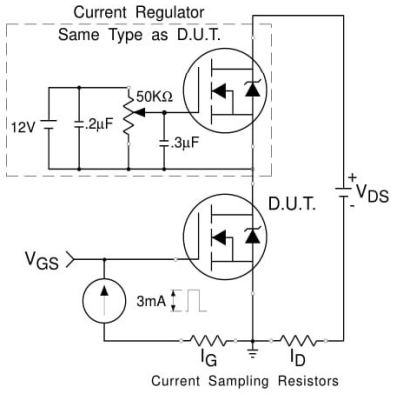


Fig 13b. Gate Charge Test Circuit

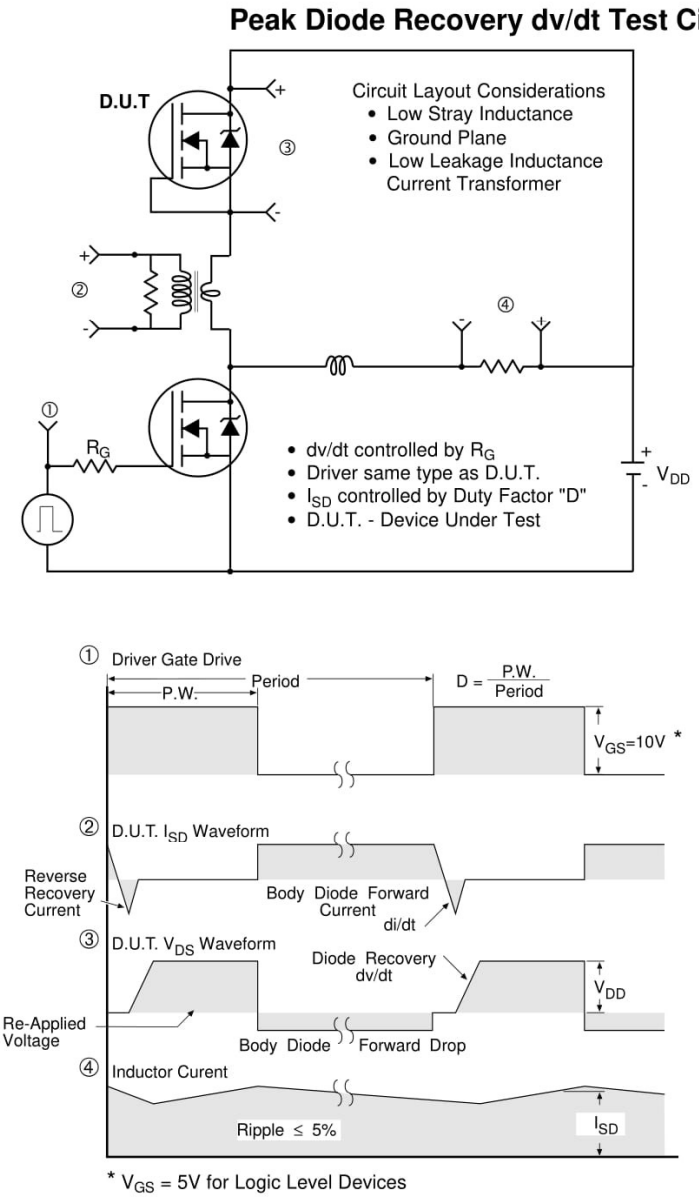
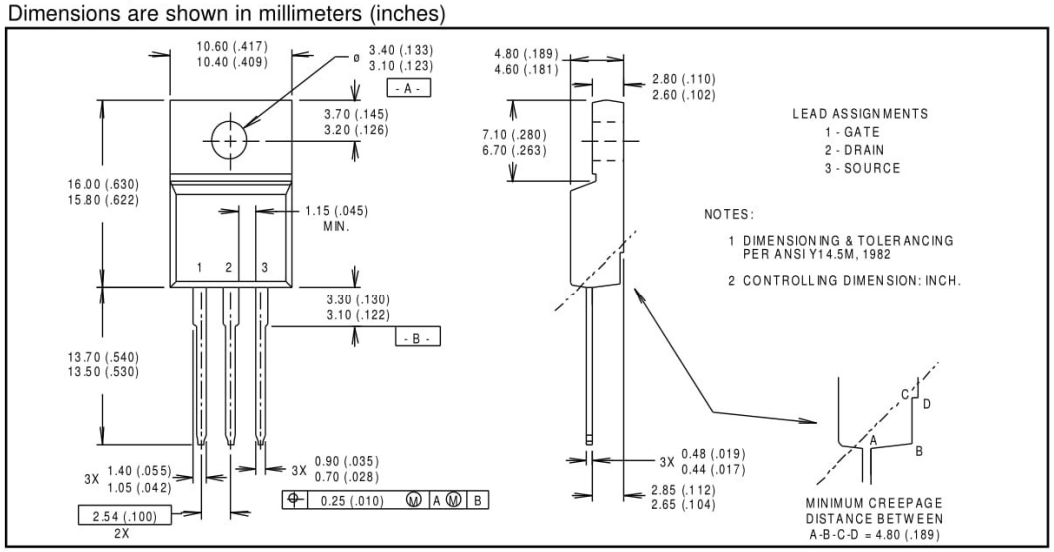


Fig 14. For N-Channel HEXFETS

Package Outline

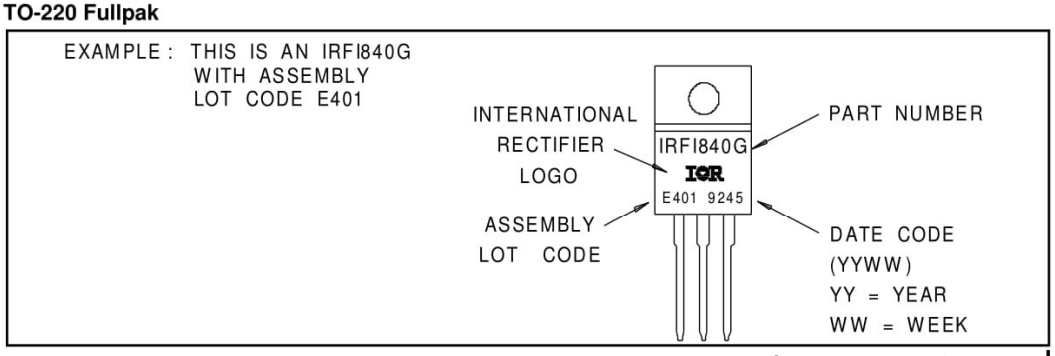
TO-220 Fullpak Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220 Fullpak



International
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EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

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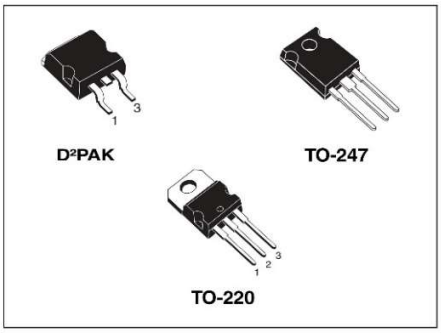
STP120NF10 - STB120NF10
STW120NF10

N-channel 100V - 0.009Ω - 110A - TO-247 - TO-220 - D²PAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STW120NF10	100V	<0.0105Ω	110A
STP120NF10	100V	<0.0105Ω	110A
STB120NF10	100V	<0.0105Ω	110A

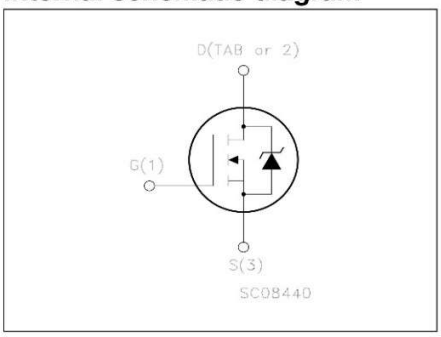
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization



Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize the on-resistance. It is therefore suitable as primary switch in advanced high-efficiency,high-frequency isolated DC-DC converters for Telecom and Computer application. It is also intended for any applications with low gate drive requirements.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STW120NF10	W120NF10	TO-247	Tube
STP120NF10	P120NF10	TO-220	Tube
STB120NF10	B120NF10	D²PAK	Tape & reel

October 2006 Rev 6 1/15
www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	110	A
I_D	Drain current (continuous) at T_C=100°C	77	A
I_{DM} (1)	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at T_C = 25°C	312	W
	Derating factor	2.08	W/°C
dv/dt (2)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (3)	Single pulse avalanche energy	550	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C
T_L	Maximum lead temperature for soldering purpose	300	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 120A$, di/dt ≤ 300A/µs, $V_{DD} = 80\%V_{(BR)DSS}$
3. Starting Tj = 25°C, I_D = 60A, V_{DD} = 50V

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.48	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating@125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 60A		0.009	0.0105	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =25V, I_D = 60A		90		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		5200 785 325		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=80V, I_D = 120A V_{GS} =10V *(see Figure 13)*		172 32 64	233	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=50V, I_D= 60A, R_G=4.7Ω, V_{GS}=10V *(see Figure 12)*		25 90 132 68		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				110	A
I_{SDM}(1)	Source-drain current (pulsed)				440	A
V_{SD}(2)	Forward on voltage	I_{SD}=120A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=120A, di/dt = 100A/µs, V_{DD}=40V, Tj=150°C *(see Figure 17)*		152 760 10		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

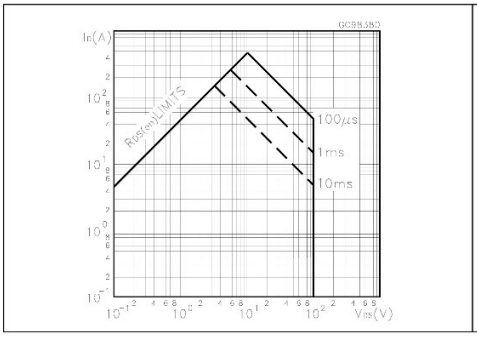


Figure 2. Thermal impedance

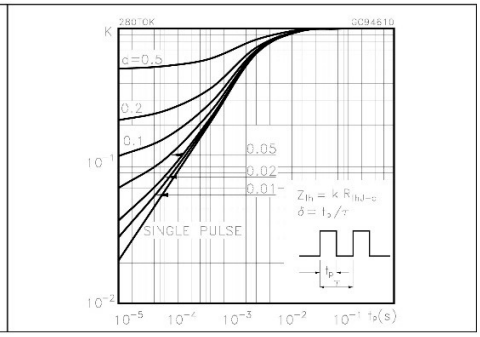


Figure 3. Output characterisics

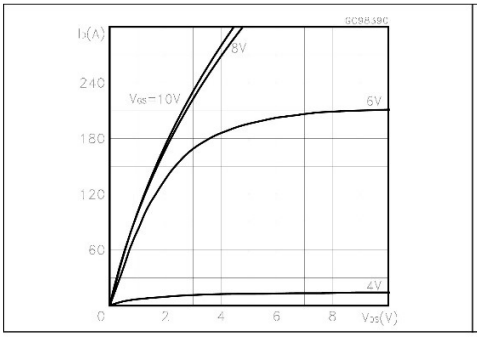


Figure 4. Transfer characteristics

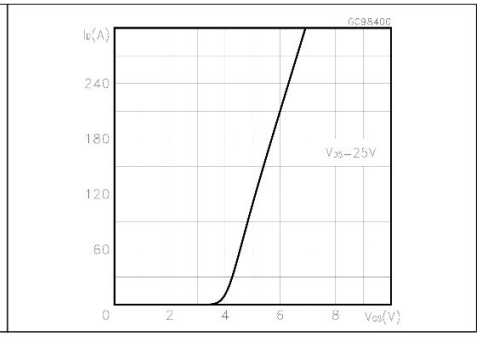


Figure 5. Normalized B_{VDSS} vs temperature

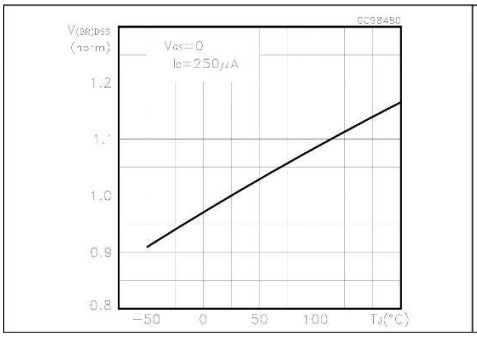


Figure 6. Static drain-source on resistance

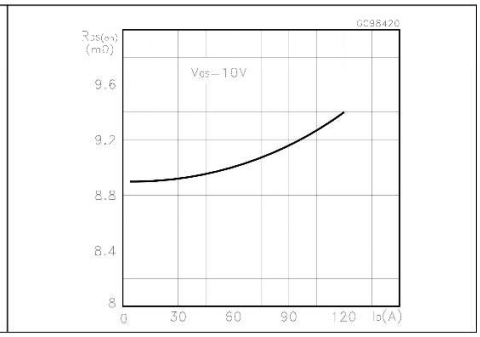


Figure 7. Gate charge vs gate-source voltage

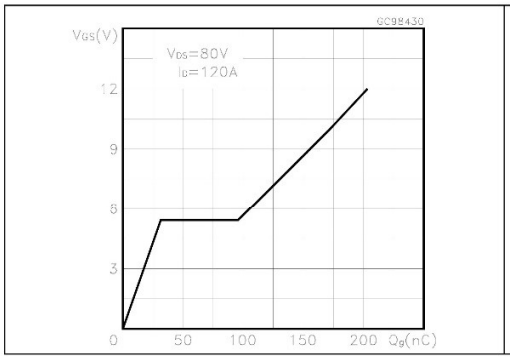


Figure 8. Capacitance variations

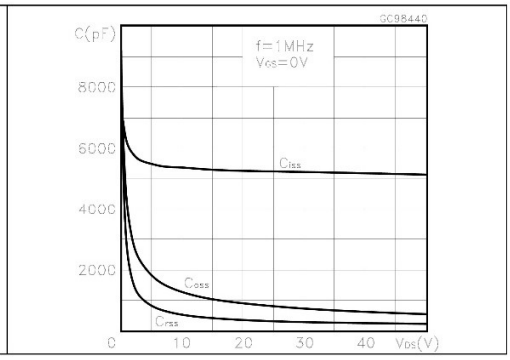


Figure 9. Normalized gate threshold voltage vs temperature

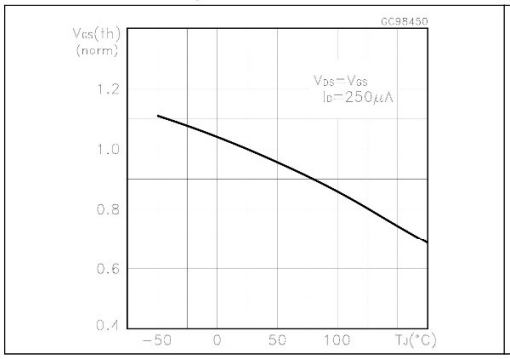


Figure 10. Normalized on resistance vs temperature

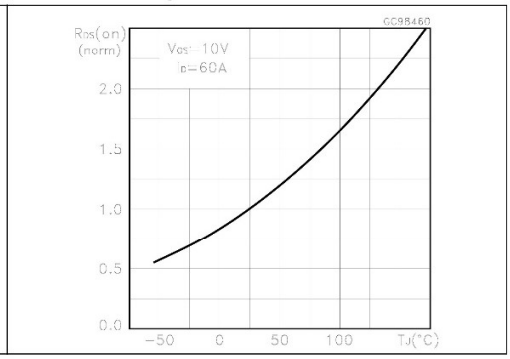
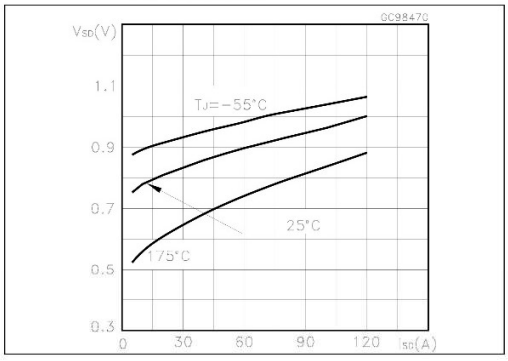


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

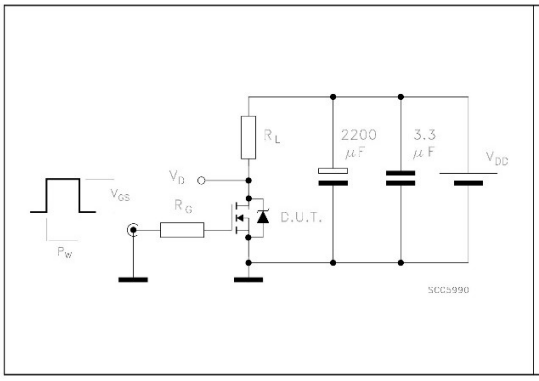


Figure 13. Gate charge test circuit

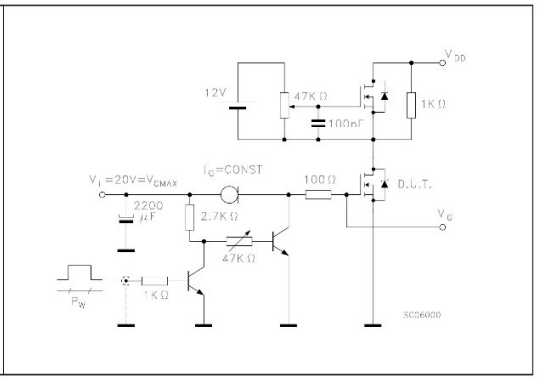


Figure 14. Test circuit for inductive load switching and diode recovery times

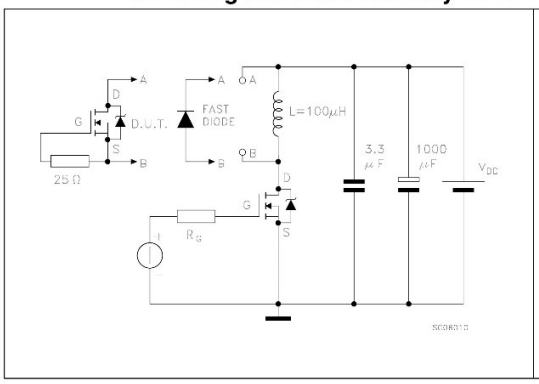


Figure 15. Unclamped inductive load test circuit

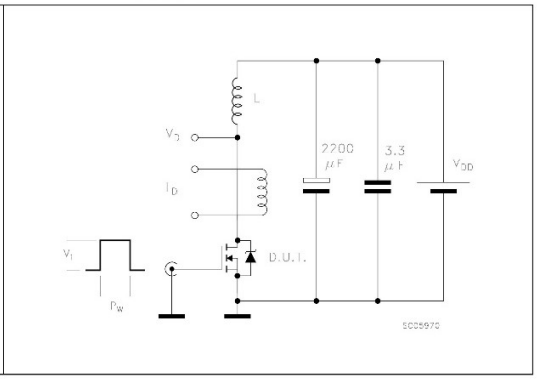


Figure 16. Unclamped inductive waveform

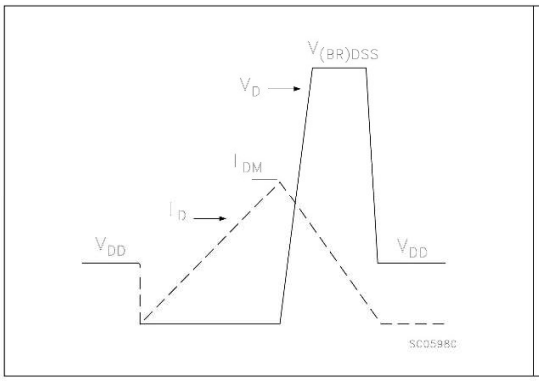
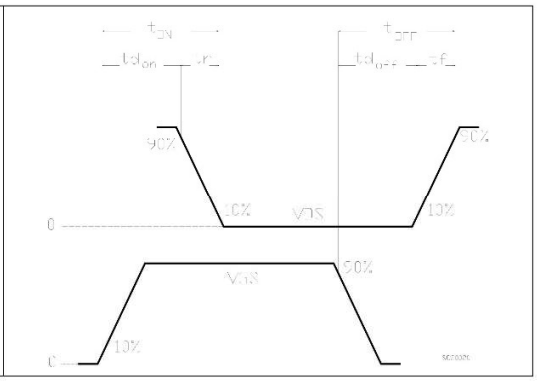
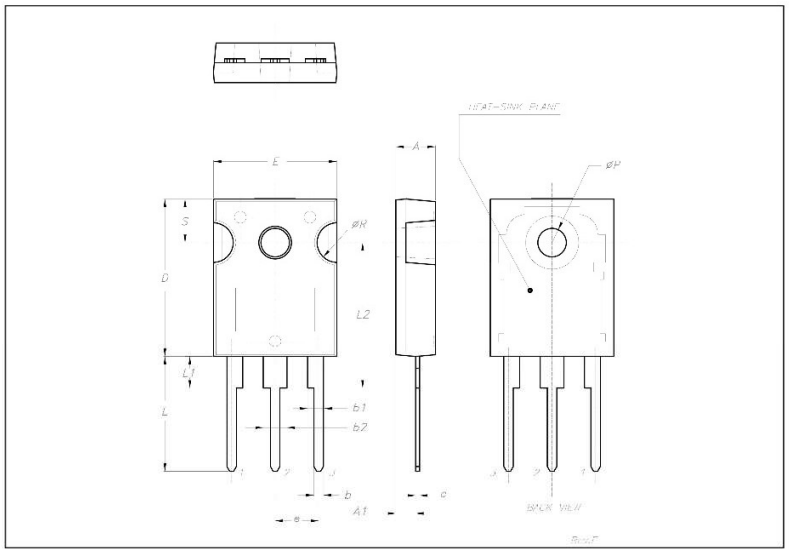


Figure 17. Switching time waveform



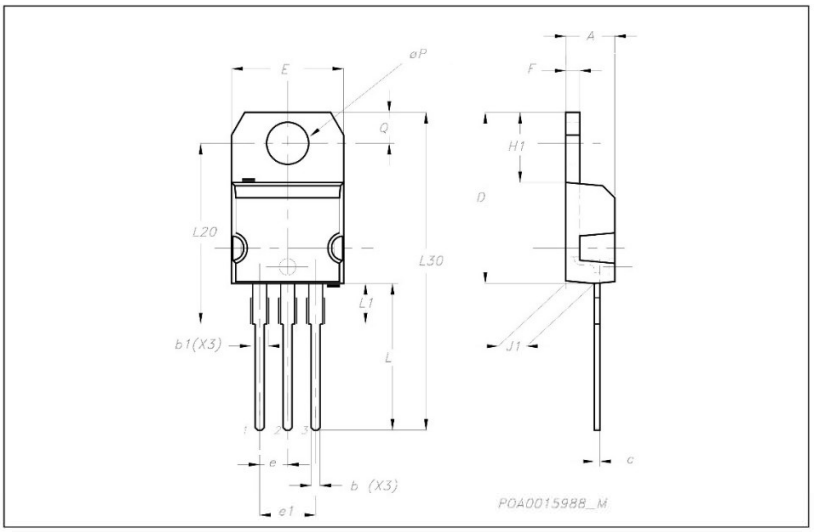
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



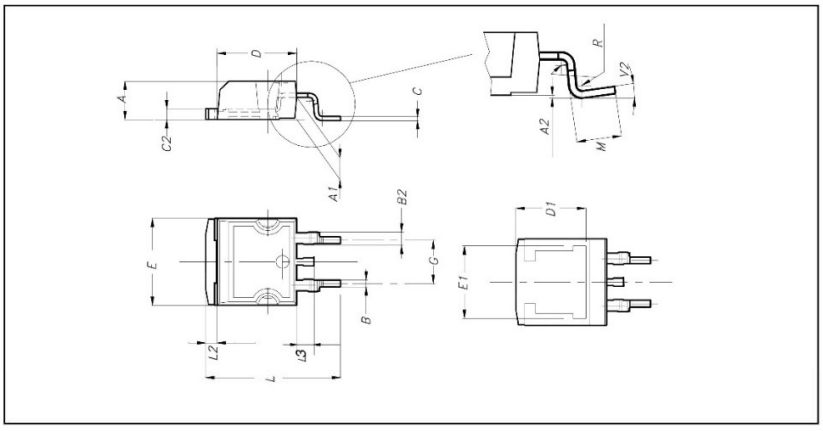
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



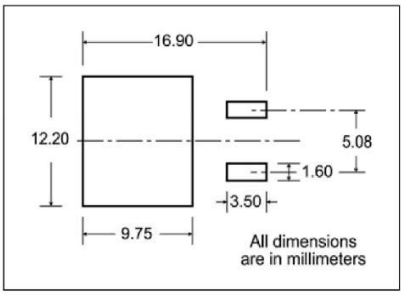
D^2PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			

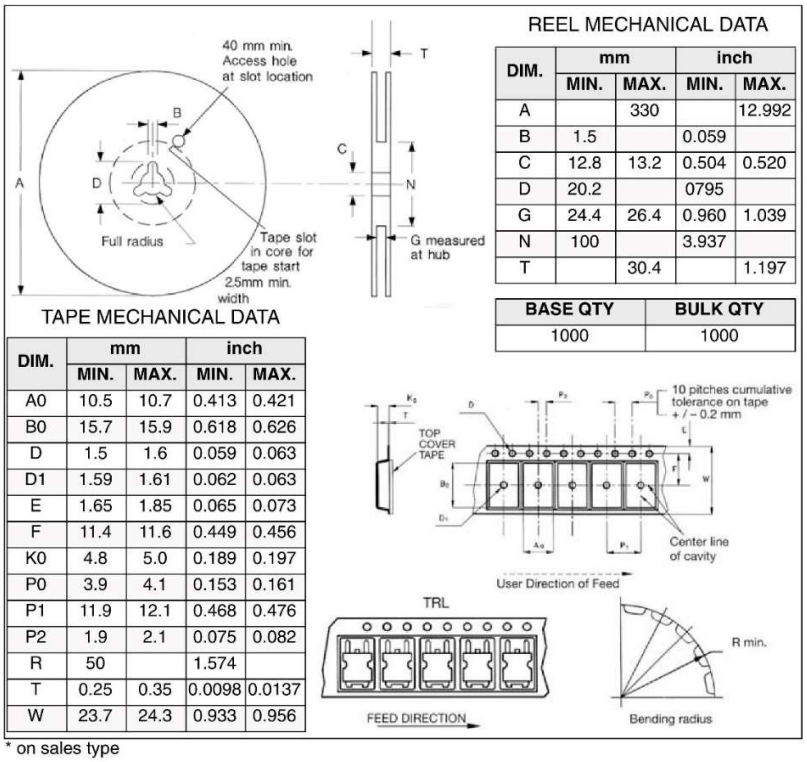


5 Packaging mechanical data

D^2PAK FOOTPRINT



TAPE AND REEL SHIPMENT



REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

* on sales type

pico Technology

PicoLog® 1000 Series

Multi-channel data acquisition

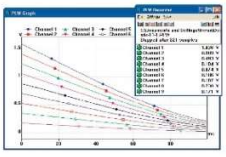
Up to 16 unipolar analog input channels
Up to 12-bit resolution with 0.5% accuracy
Up to 4 software-configurable digital output lines
Up to 1 MS/s sample rate
USB connected and powered
Complete with ready-to-go data logging software
Includes API and examples for C, Excel (VBA), LabVIEW

All you need

Designed to meet the needs of a wide range of general-purpose voltage, sensor and transducer logging applications, the PicoLog 1216 and 1012 feature independent software-configurable channels, ranges, scaling and control outputs. An optional external terminal board allows for easy range extension and ease of terminating wires.

Ready-to-go

The PicoLog 1000 Series multi-channel voltage data loggers include everything needed for immediate use and are complemented by a full suite of software including the PicoLog data logging package, the PicoScope oscilloscope package and a software development kit (SDK) for writing user programs.



Flexible sampling modes

Both loggers feature 3 sampling modes to meet most data logging needs: streaming, real-time continuous and block mode. Streaming allows channel voltage readings to be logged continuously at 1 kS/s on any number of channels, while real-time continuous provides averaged, time-accurate readings with automatic measurements available in PicoLog. Block mode captures at the full 1 MS/s sample rate of the logger into available memory.

www.picotech.com

	PicoLog 1216	PicoLog 1012
INPUTS		
Analog inputs	16 channels	12 channels
Resolution (bits)	12 bits	10 bits
Sampling rate, streaming	1 kS/s per channel in PicoLog, 100 kS/s using API	
Sampling rate, block mode	1 MS/s using PicoScope and API	
Sampling rate, real-time continuous	1 kS/s or greater	
Capture size	8k sample internal buffer shared by all channels; 1 million sample limit using SDK	
Input type	Single-ended, unipolar	
Voltage range	0 - 2.5 V	
Accuracy	0.5% @ 12 bits	1.0% @ 10 bits
Overload protection	±30 V	
AC/DC coupling	DC coupling	
Input impedance	1MΩ fixed – buffered inputs	
OUTPUTS		
Digital outputs	4 digital outputs	2 digital outputs
Output power for sensors	2.5 V @ 10 mA. Current-limited	
Other outputs	PWM output (PicoScope 6 and API)	None
GENERAL		
PC connectivity	USB 2.0 full speed	
Power requirements	Powered from USB port, < 200 mA operating, < 100 mA on startup	
Input/output connector	25-way D Type, female (pin-compatible with USB ADC-11)	
Dimensions	45 mm x 100 mm x 140 mm (1.77" x 3.94" x 5.51")	
Weight	< 200 g (7.05 oz)	
Temperature range	Operating: 0 °C to 70 °C (20 °C to 50 °C for stated accuracy)	
Humidity range	Operating: 5 % to 85 % RH non-condensing	
Compliance	CE (EMC) Class A emissions & immunity. FCC emissions	
PC requirements	Windows 7, Windows 8 (not RT) or Windows 10, 32 or 64 bit	
- PicoLog FEATURES		
Multiple views	View data as a graph, spreadsheet or text	
Parameter scaling	Convert raw data into standard engineering units	
Math functions	Use mathematical equations to calculate additional parameters	
Alarm limits	Program an alert if a parameter goes out of a specified range	
- PicoScope 6 FEATURES		
Capture modes	Oscilloscope, spectrum and persistence modes	
Channel maths	Calculate the sum, difference, product, inverse or create your own custom function using standard arithmetic, exponential and trigonometric functions	
Automated measurements	15 scope measurements and 11 spectrum measurements	
DEVELOPMENT KIT		
SDK	Supports all C-compatible languages. Example code provided in C, Visual Basic for Applications (Microsoft Excel) and National Instruments LabVIEW	
Compatibility mode	Drop-in replacement of USB ADC-11	

Ordering information

ORDER CODE	DESCRIPTION	GBP*	USD*	EUR*
PP547	PicoLog 1216 with terminal board	£159	$259	€219
PP546	PicoLog 1012 with terminal board	£109	$179	€149
PP545	Terminal board only	£15	$25	€21

* Prices are correct at the time of publication. VAT not included.
Please contact Pico Technology for the latest prices before ordering.

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Tyler
Texas 75702
United States

☎ +1 800 591 2796
+1 620 272 0981
sales@picotech.com

www.picotech.com

pico Technology

ACS712

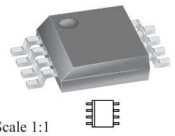
Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at T_A = 25°C
- Small footprint, low-profile SOIC8 package
- 1.2 mΩ internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 66 to 185 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis
- Ratiometric output from supply voltage

TÜV America
Certificate Number:
U8V 06 05 54214 010

Package: 8 Lead SOIC (suffix LC)



Approximate Scale 1:1

Description

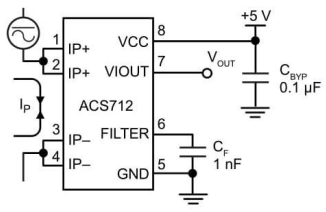
The Allegro® ACS712 provides economical and precise solutions for AC or DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope (>$V_{IOUT(Q)}$) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 mΩ typical, providing low power loss. The thickness of the copper conductor allows survival of

Continued on the next page…

Typical Application



Application 1. The ACS712 outputs an analog signal, V_{OUT}, that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I_P, within the range specified. C_F is recommended for noise management, with values that depend on the application.

Description (continued)

the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS712 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS712 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Selection Guide

Part Number	Packing*	T_A (°C)	Optimized Range, I_P (A)	Sensitivity, Sens (Typ) (mV/A)
ACS712ELCTR-05B-T	Tape and reel, 3000 pieces/reel	–40 to 85	±5	185
ACS712ELCTR-20A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±20	100
ACS712ELCTR-30A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±30	66

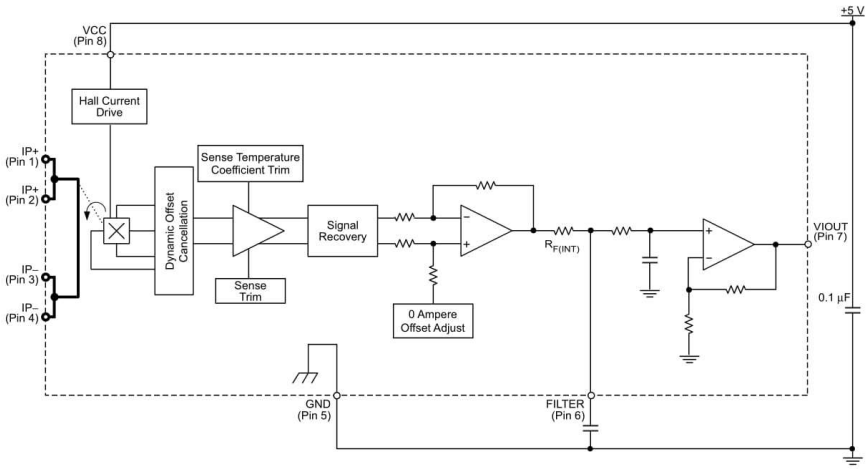
*Contact Allegro for additional packing options.

Absolute Maximum Ratings

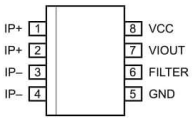
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		8	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Reinforced Isolation Voltage	V_{ISO}	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	2100	VAC
		Maximum working voltage according to UL60950-1	184	V_{peak}
Basic Isolation Voltage	$V_{ISO(bsc)}$	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	1500	VAC
		Maximum working voltage according to UL60950-1	354	V_{peak}
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		10	mA
Overcurrent Transient Tolerance	I_P	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Parameter	Specification
Fire and Electric Shock	CAN/CSA-C22.2 No. 60950-1-03 UL 60950-1:2003 EN 60950-1:2001

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP–	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

COMMON OPERATING CHARACTERISTICS[1] over full range of T_A, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	–	10	13	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.2	–	mΩ
Rise Time	t_r	I_P = I_P(max), T_A = 25°C, C_{OUT} = open	–	5	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C; I_P is 10 A peak-to-peak	–	80	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	1.5	–	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional; I_P = 0 A, T_A = 25°C	–	V_{CC} × 0.5	–	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_J = 25°C, 20 A present on leadframe	–	35	–	µs
Magnetic Coupling[2]			–	12	–	G/A
Internal Filter Resistance[3]	$R_{F(INT)}$			1.7		kΩ

[1]Device may be operated at higher primary current levels, I_P, and ambient, T_A, and internal leadframe temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]1G = 0.1 mT.

[3]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.

COMMON THERMAL CHARACTERISTICS[1]

			Min.	Typ.	Max.	Units
Operating Internal Leadframe Temperature	T_A	E range	–40	–	85	°C
					Value	Units
Junction-to-Lead Thermal Resistance[2]	$R_{\theta JL}$	Mounted on the Allegro ASEK 712 evaluation board			5	°C/W
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro 85-0322 evaluation board, includes the power consumed by the board			23	°C/W

[1]Additional thermal information is available on the Allegro website.

[2]The Allegro evaluation board has 1500 mm^2 of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.

x05B PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–5	–	5	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	180	185	190	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 185 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	21	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.26	–	mV/°C
		T_A = 25°C to 150°C	–	–0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.054	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.008	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P =±5 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, $T_{J(max)}$, is not exceeded.

[2]Percentage of I_P, with I_P = 5 A. Output filtered.

x20A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–20	–	20	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	96	100	104	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 100 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	11	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.34	–	mV/°C
		T_A = 25°C to 150°C	–	–0.07	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.017	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.004	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P =±20 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 20 A. Output filtered.

x30A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–30	–	30	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	63	66	69	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 66 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	7	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.35	–	mV/°C
		T_A = 25°C to 150°C	–	–0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.007	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.002	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±30 A, T_A = 25°C	–	±1.5	–	%

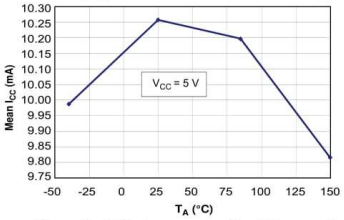
[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 30 A. Output filtered.

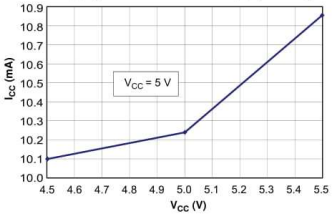
Characteristic Performance

I_P = 5 A, unless otherwise specified

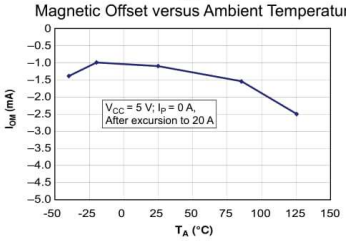
Mean Supply Current versus Ambient Temperature



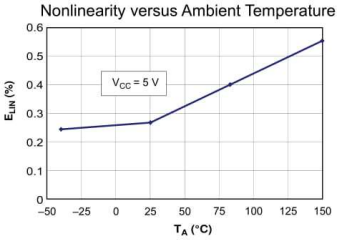
Supply Current versus Supply Voltage



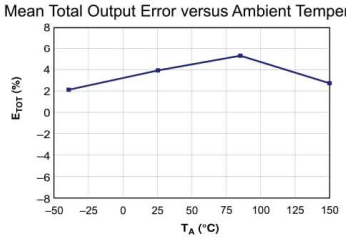
Magnetic Offset versus Ambient Temperature



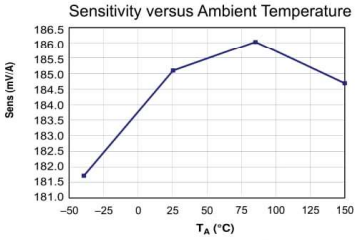
Nonlinearity versus Ambient Temperature



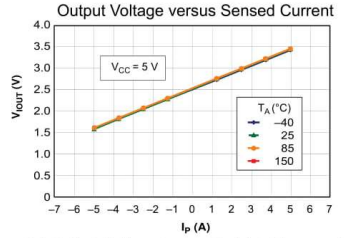
Mean Total Output Error versus Ambient Temperature



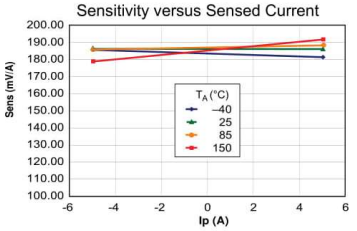
Sensitivity versus Ambient Temperature



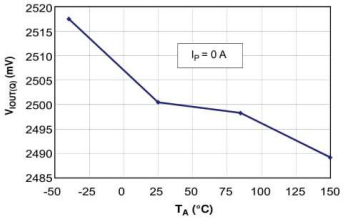
Output Voltage versus Sensed Current



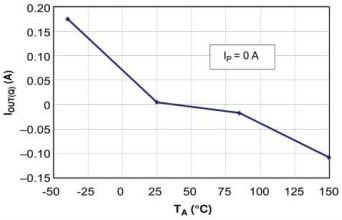
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta\text{ gain}\times\%\text{ sat}\,(V_{IOUT\_\text{full-scale amperes}}-V_{IOUT(Q)})}{2\,(V_{IOUT\_\text{half-scale amperes}}-V_{IOUT(Q)})}\right]\right\}$$

where $V_{IOUT\ \text{full-scale amperes}}$ = the output voltage (V) when the sampled current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+\text{ full-scale amperes}}-V_{IOUT(Q)}}{V_{IOUT(Q)}-V_{IOUT\_-\text{full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

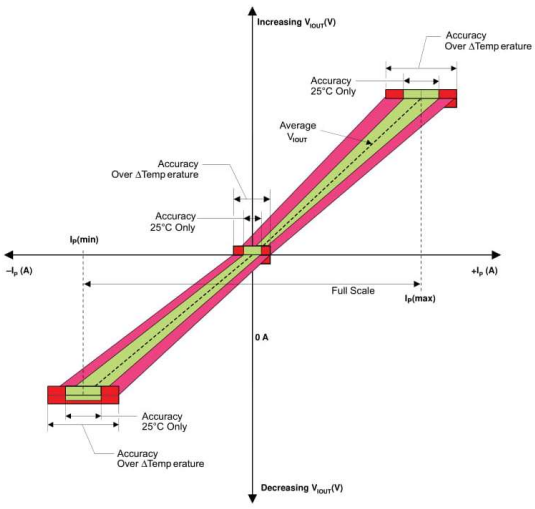
Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

$$100\left(\frac{V_{IOUT(Q)VCC}/V_{IOUT(Q)5V}}{V_{CC}/5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

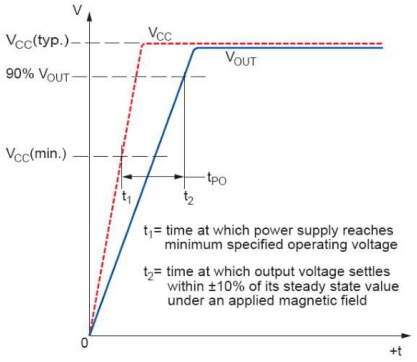
$$100\left(\frac{Sens_{VCC}/Sens_{5V}}{V_{CC}/5\text{ V}}\right)$$

Output Voltage versus Sampled Current
Accuracy at 0 A and at Full-Scale Current

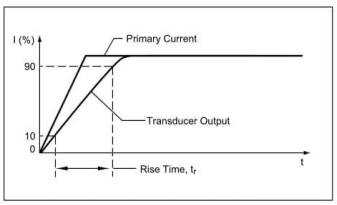


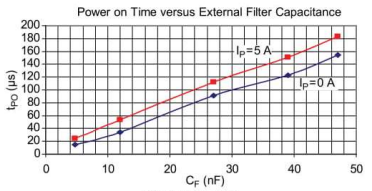
Definitions of Dynamic Response Characteristics

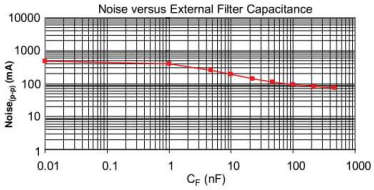
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

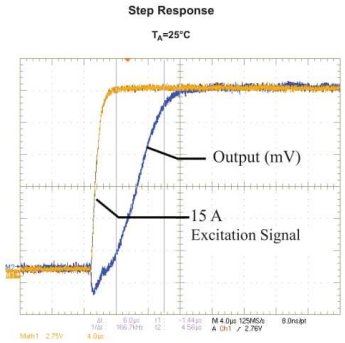


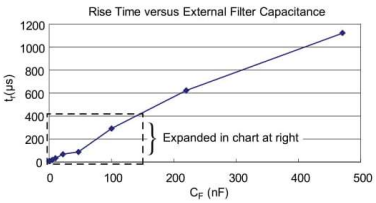
Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



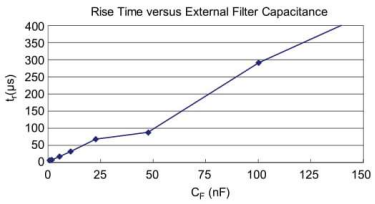




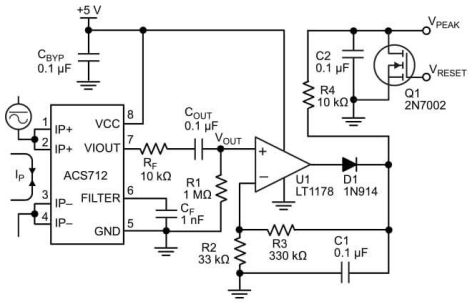




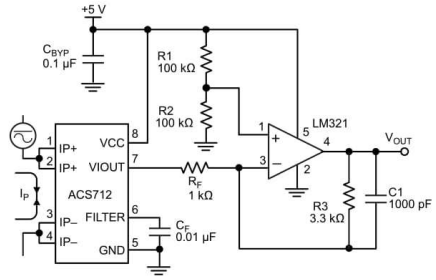
C_F (nF)	t_r (µs)
0	6.6
1	7.7
4.7	17.4
10	32.1
22	68.2
47	88.2
100	291.3
220	623.0
470	1120.0



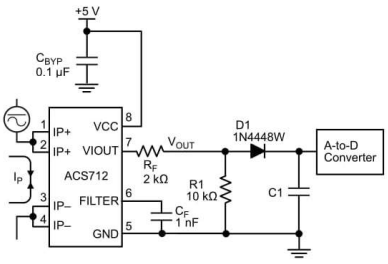
Typical Applications



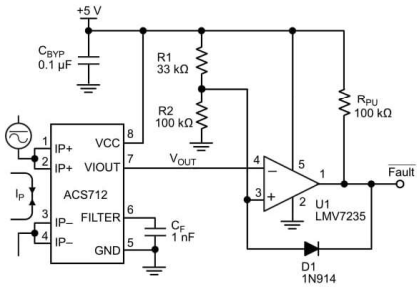
Application 2. Peak Detecting Circuit



Application 3. This configuration increases gain to 610 mV/A (tested using the ACS712ELC-05A).



Application 4. Rectified Output. 3.3 V scaling and rectification application for A-to-D converters. Replaces current transformer solutions with simpler ACS circuit. C1 is a function of the load resistance and filtering desired. R1 can be omitted if the full range is desired.



Application 5. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.

Improving Sensing System Accuracy Using the FILTER Pin

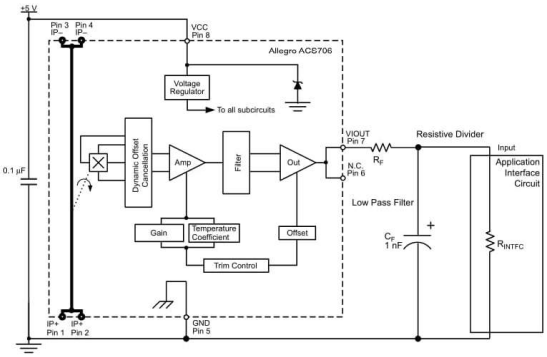
In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, ΔV_{ATT}, is a result of the resistive divider effect between the resistance of the external filter, R_F (see Application 6), and the input impedance and resistance of the customer interface circuit, R_{INTFC}. The transfer function of this resistive divider is given by:

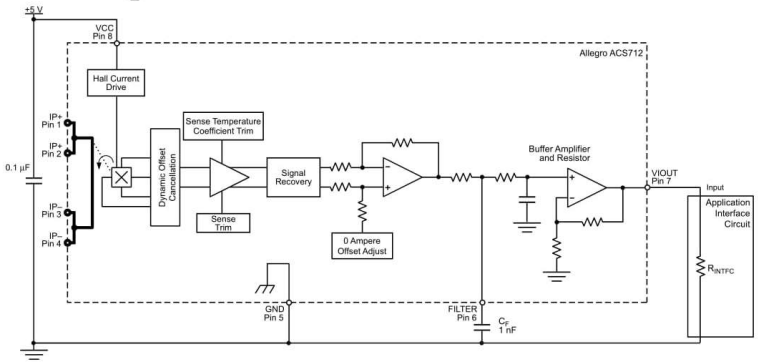
$$\Delta V_{ATT} = V_{IOUT}\left(\frac{R_{INTFC}}{R_F + R_{INTFC}}\right) .$$

Even if R_F and R_{INTFC} are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance, R_{INTFC}, of a typical analog-to-digital converter (ADC) can be as low as 10 kΩ.

The ACS712 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, C_F (see Application 7) from the FILTER pin to ground. The buffer amplifier inside of the ACS712 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for ΔV_{ATT}. Therefore, the ACS712 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.

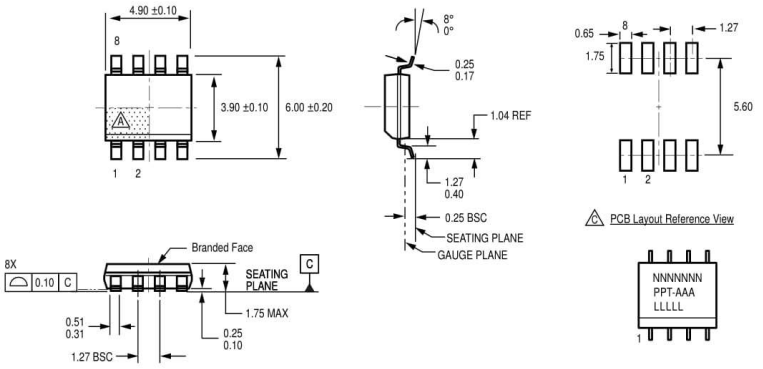


Application 6. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, R_F, and the resistance of the customer interface circuit, R_{INTFC}. This resistive divider will cause excessive attenuation, as given by the transfer function for ΔV_{ATT}.



Application 7. Using the FILTER pin provided on the ACS712 eliminates the attenuation effects of the resistor divider between R_F and R_{INTFC}, shown in Application 6.

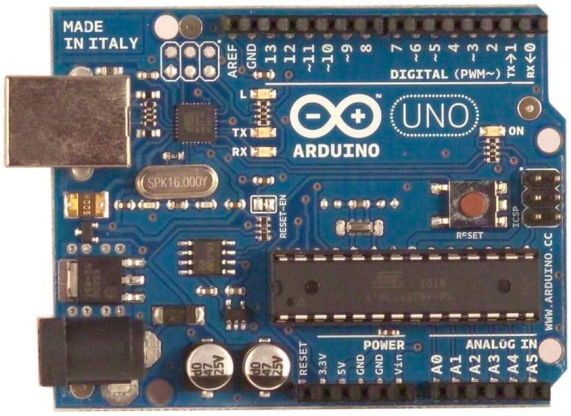
Package LC, 8-pin SOIC



For Reference Only; not for tooling use (reference MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Branding scale and appearance at supplier discretion
C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Arduino UNO



Product Overview

The Arduino Uno is a microcontroller board based on the ATmega328 (datasheet). It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

"Uno" means one in Italian and is named to mark the upcoming release of Arduino 1.0. The Uno and version 1.0 will be the reference versions of Arduno, moving forward. The Uno is the latest in a series of USB Arduino boards, and the reference model for the Arduino platform; for a comparison with previous versions, see the index of Arduino boards.

Index

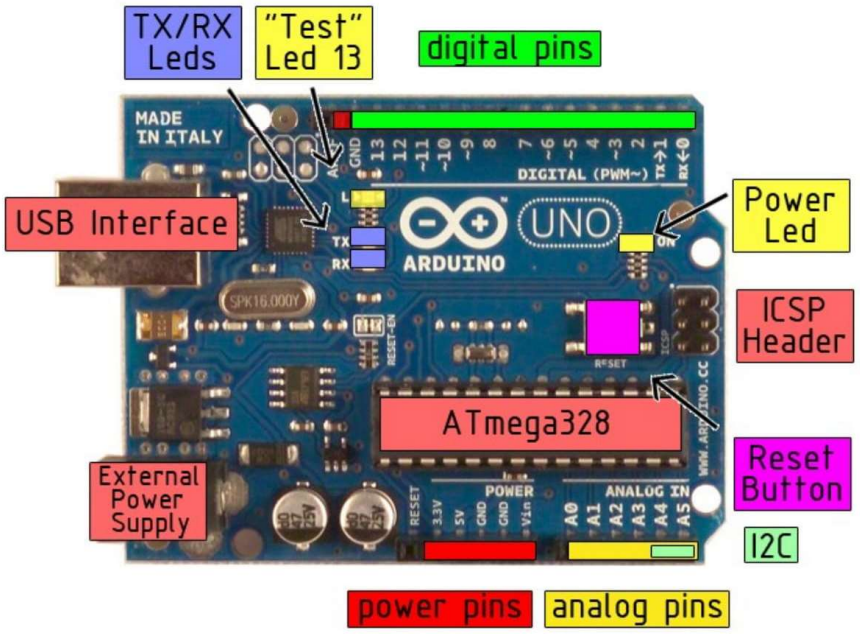
Technical Specification

EAGLE files: arduino-duemilanove-uno-design.zip Schematic: arduino-uno-schematic.pdf

Summary

Microcontroller	ATmega328
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limits)	6-20V
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	6
DC Current per I/O Pin	40 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	32 KB of which 0.5 KB used by bootloader
SRAM	2 KB
EEPROM	1 KB
Clock Speed	16 MHz

the board



Power

The Arduino Uno can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The power pins are as follows:

- **VIN.** The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V.** The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.
- **3V3.** A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND.** Ground pins.

Memory

The Atmega328 has 32 KB of flash memory for storing code (of which 0,5 KB is used for the bootloader); It has also 2 KB of SRAM and 1 KB of EEPROM (which can be read and written with the EEPROM library).

Input and Output

Each of the 14 digital pins on the Uno can be used as an input or output, using pinMode(), digitalWrite(), and digitalRead() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. TThese pins are connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip .
- **External Interrupts: 2 and 3.** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the attachInterrupt() function for details.
- **PWM: 3, 5, 6, 9, 10, and 11.** Provide 8-bit PWM output with the analogWrite() function.
- **SPI: 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK).** These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.

- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Uno has 6 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and the analogReference() function. Additionally, some pins have specialized functionality:

- **I²C: 4 (SDA) and 5 (SCL).** Support I²C (TWI) communication using the Wire library.

There are a couple of other pins on the board:

- **AREF.** Reference voltage for the analog inputs. Used with analogReference().
- **Reset.** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

See also the mapping between Arduino pins and Atmega328 ports.

Communication

The Arduino Uno has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega328 provides UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An ATmega8U2 on the board channels this serial communication over USB and appears as a virtual com port to software on the computer. The '8U2 firmware uses the standard USB COM drivers, and no external driver is needed. However, on Windows, an *.inf file is required..

The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the USB-to-serial chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A SoftwareSerial library allows for serial communication on any of the Uno's digital pins.

The ATmega328 also support I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the documentation for details. To use the SPI communication, please see the ATmega328 datasheet.

Programming

The Arduino Uno can be programmed with the Arduino software (download). Select "Arduino Uno w/ ATmega328" from the **Tools > Board** menu (according to the microcontroller on your board). For details, see the reference and tutorials.

The ATmega328 on the Arduino Uno comes preburned with a bootloader that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).

You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see these instructions for details.

The ATmega8U2 firmware source code is available . The ATmega8U2 is loaded with a DFU bootloader, which can be activated by connecting the solder jumper on the back of the board (near the map of Italy) and then resetting the 8U2. You can then use Atmel's FLIP software (Windows) or the DFU programmer (Mac OS X and Linux) to load a new firmware. Or you can use the ISP header with an external programmer (overwriting the DFU bootloader).

Automatic (Software) Reset

Rather than requiring a physical press of the reset button before an upload, the Arduino Uno is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Uno is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Uno. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

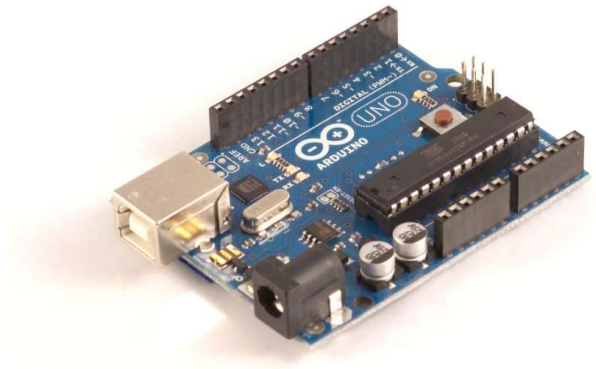
The Uno contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see this forum thread for details.

USB Overcurrent Protection

The Arduino Uno has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

Physical Characteristics

The maximum length and width of the Uno PCB are 2.7 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.



How to use Arduino

Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the Arduino programming language (based on Wiring) and the Arduino development environment (based on Processing). Arduino projects can be stand-alone or they can communicate with software on running on a computer (e.g. Flash, Processing, MaxMSP).

Arduino is a cross-platoform program. You'll have to follow different instructions for your personal OS. Check on the Arduino site for the latest instructions. *http://arduino.cc/en/Guide/HomePage*

Linux Install Windows Install Mac Install

Once you have downloaded/unzipped the arduino IDE, you can Plug the Arduino to your PC via USB cable.

Blink led

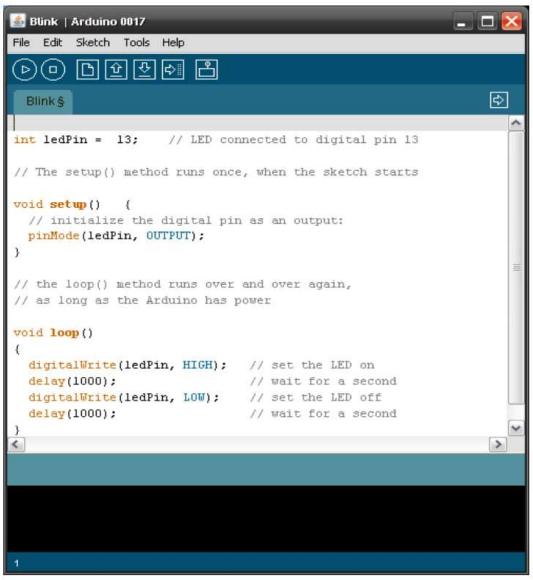
Now you're actually ready to "burn" your first program on the arduino board. To select "blink led", the physical translation of the well known programming "hello world", select

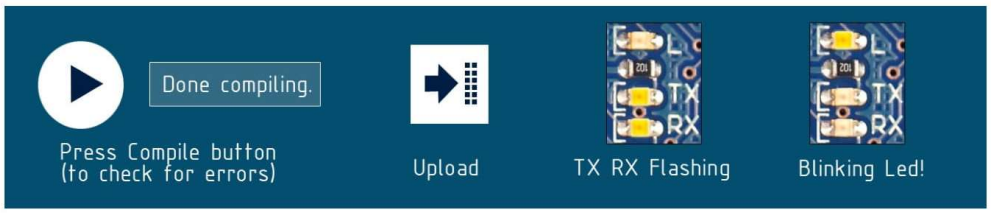
File>Sketchbook>
Arduino-0017>Examples>
Digital>Blink

Once you have your skecth you'll see something very close to the screenshot on the right.

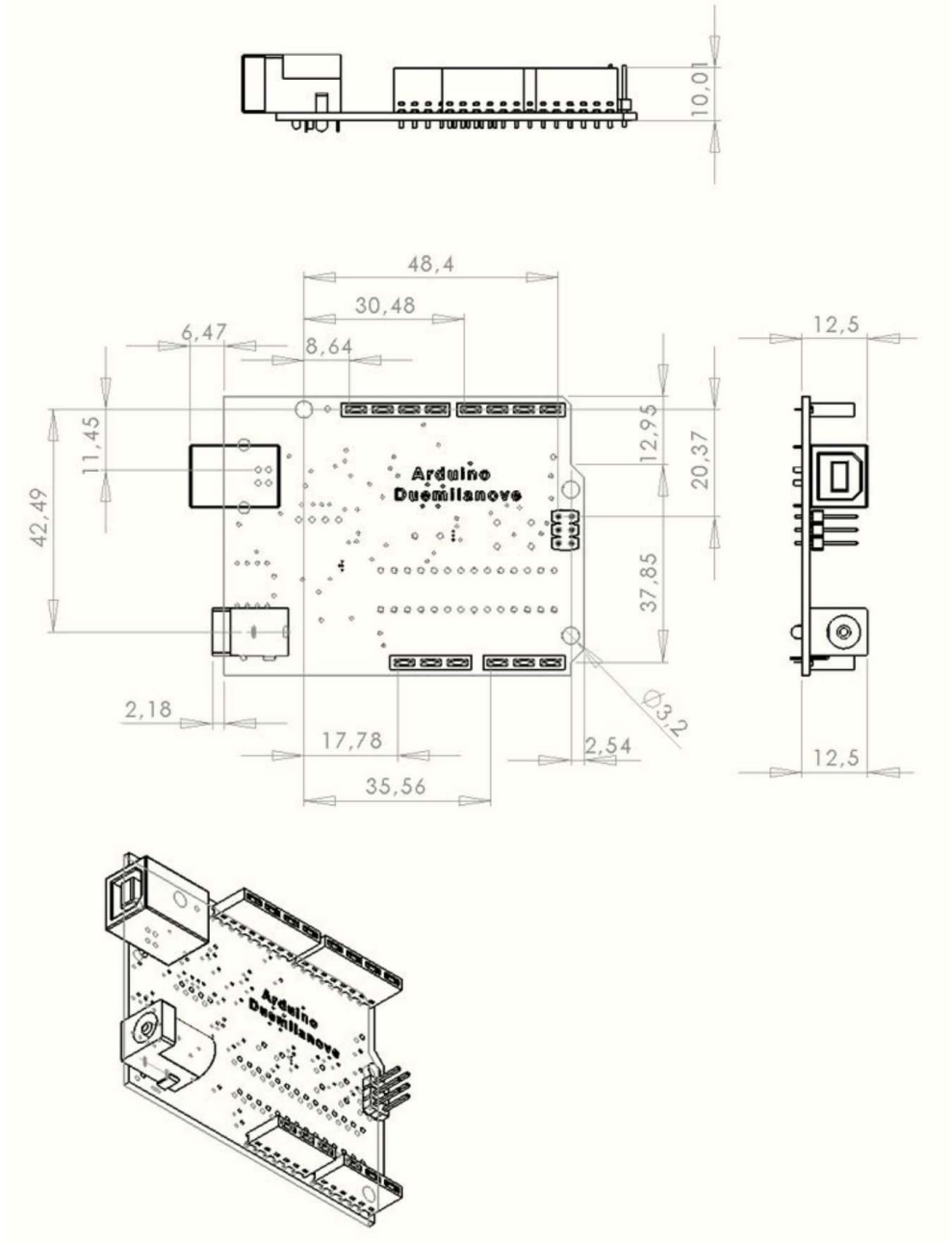
In **Tools>Board** select

Now you have to go to
Tools>SerialPort
and select the right serial port, the one arduino is attached to.





Dimensioned Drawing



RA12-100D (12V100Ah)

RA12-100D is AGM Deep cycle battery with 10 years floating design life, specially designed for frequent cyclic discharge usage. By using strong grid and specific paste plate, it makes battery have 30% more cyclic life time than standby series. It is applicable for solar energy system, golf cart, electric wheelchair, etc..

RITAR®

Specification

Cells Per Unit	6
Voltage Per Unit	12
Capacity	100Ah@10hr-rate to 1.75V per cell @25°C
Weight	Approx. 30.0 Kg
Max. Discharge Current	1000 A (5 sec)
Internal Resistance	Approx. 5 mΩ
Operating Temperature Range	Discharge: -20°C~60°C Charge: 0°C~50°C Storage: -20°C~60°C
Normal Operating Temperature Range	25°C±5°C
Float charging Voltage	13.6 to 13.8 VDC/unit Average at 25°C
Recommended Maximum Charging Current Limit	30 A
Equalization and Cycle Service	14.6 to 14.8 VDC/unit Average at 25°C
Self Discharge	RITAR batteries can be stored for more than 6 months at 25°C. Self-discharge ratio less than 3% per month at 25°C. Please charge batteries before using.
Terminal	Terminal F5/F12
Container Material	A.B.S. (UL94-HB) , Flammability resistance of UL94-V1 can be available upon request.

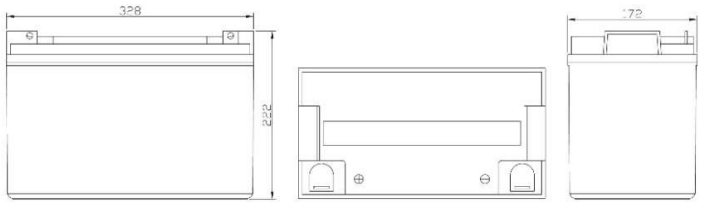
MH28539

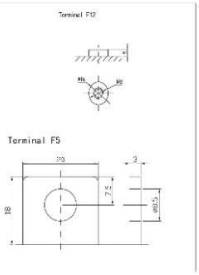
GHM20206-0910-E-16

ISO9001:2000 Certificate

Dimensions

Unit: mm Dimension: 328(L)×172(W)×222(H)





Constant Current Discharge Characteristics: A (25°C)

F.V/Time	5MIN	10MIN	15MIN	30MIN	1HR	2HR	3HR	4HR	5HR	8HR	10HR	20HR
9.60V	344.7	247.0	179.7	110.4	62.40	35.39	25.06	20.74	16.32	11.92	10.083	5.332
10.0V	335.5	235.0	176.0	108.6	62.11	35.12	24.96	20.64	16.22	11.83	9.986	5.235
10.2V	316.1	226.7	173.3	107.6	61.54	34.84	24.77	20.54	16.13	11.73	9.889	5.138
10.5V	283.9	209.2	165.0	104.9	60.96	34.57	24.67	20.35	15.94	11.63	9.792	5.041
10.8V	256.2	190.8	152.1	100.3	59.52	33.93	24.00	19.87	15.65	11.44	9.695	4.944
11.1V	223.0	170.5	136.4	93.98	56.54	33.38	22.94	18.91	14.98	10.96	9.404	4.654

Constant Power Discharge Characteristics: W (25°C)

F.V/Time	5MIN	10MIN	15MIN	30MIN	1HR	2HR	3HR	4HR	5HR	8HR	10HR	20HR
9.60V	3592	2626	1934	1246	713.7	418.6	289.2	239.6	188.9	138.4	113.4	59.89
10.0V	3518	2509	1894	1230	710.2	417.0	288.6	239.0	187.8	137.8	112.2	59.30
10.2V	3321	2425	1868	1216	705.0	413.1	286.8	237.9	187.2	136.6	111.6	58.72
10.5V	2991	2241	1781	1188	698.1	409.3	285.1	236.2	185.5	135.5	110.5	58.14
10.8V	2690	2035	1637	1134	680.8	403.3	278.2	229.8	182.6	132.6	109.3	57.56
11.1V	2322	1807	1461	1063	645.1	384.7	264.4	218.9	173.4	127.9	105.8	55.23

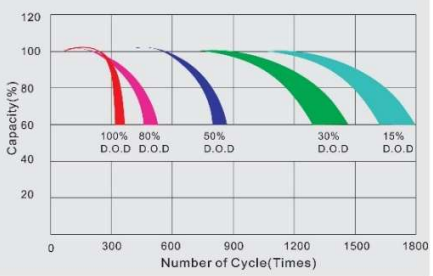
All mentioned values are average values.

RA12-100D

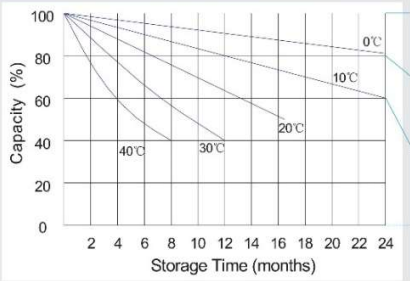
12V100Ah

RITAR®

Life characteristics of cyclic use



Storage characteristic



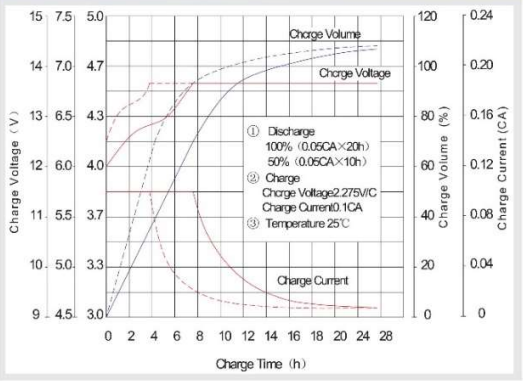
Supplementary charge required (Carry out supplementary charge before use if 100% capacity is required)

Supplementary charge required before use. This supplementary charge will help to recover the capacity and should be made as early as possible.

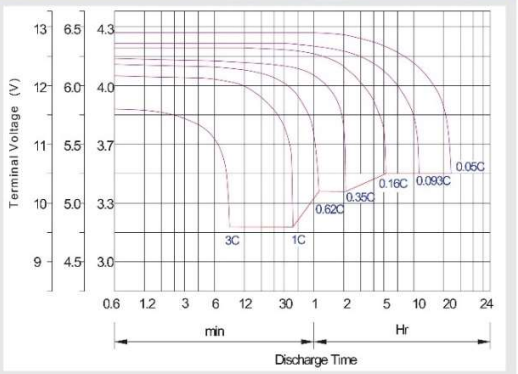
Supplementary charge may often fail to recover the capacity. The battery should never be left standing till this state is reached

Supplementary charge and storage guidelines

Charge characteristic Curve for standby use



Discharge characteristic Curve



Capacity Factors With Different Temperature

Battery Type		-20℃	-10℃	0℃	5℃	10℃	20℃	25℃	30℃	40℃	45℃
GEL Battery	6V&12V	50%	70%	83%	85%	90%	98%	100%	102%	104%	105%
	2V	60%	75%	85%	88%	92%	99%	100%	103%	105%	106%
AGM Battery	6V&12V	46%	66%	76%	83%	90%	98%	100%	103%	107%	109%
	2V	55%	70%	80%	85%	92%	99%	100%	104%	108%	110%

Discharge Current VS. Discharge Voltage

Final Discharge Voltage V/cell	1.75V	1.70V	1.60V
Discharge Current (A)	(A) ≤0.2C	0.2C< (A) <1.0C	(A) ≥1.0C

Charge the batteries at least once every six months, if they are stored at 25°C.

Charging Method:

Constant Voltage	-0.2Cx2h+2.4~2.45V/Cellx24h,Max. Current 0.3CA
Constant Current	-0.2Cx2h+0.1CAx12h
Fast	-0.2Cx2h+0.3CAx4.0h

Maintenance & Cautions

Cycle service
※ Avoid battery over discharge, especially battery sereis connection use.
※ Charged with recommend voltage, ensure battery can be full recharged.
In general, recharge capacity should be 1.1-1.15 times discharge capacity.
※ Effect of temperature on cycle charge voltage: -4mV/℃/Cell.
※ There are a number of factors that will affect the length of cyclic service.
The most significant are depth of discharge, ambient temperature,
discharge rate, and the manner in which the battery is recharged.
Generally specking, the most important factors is depth of discharge.

SHEN ZHEN RITAR POWER CO.,LTD.

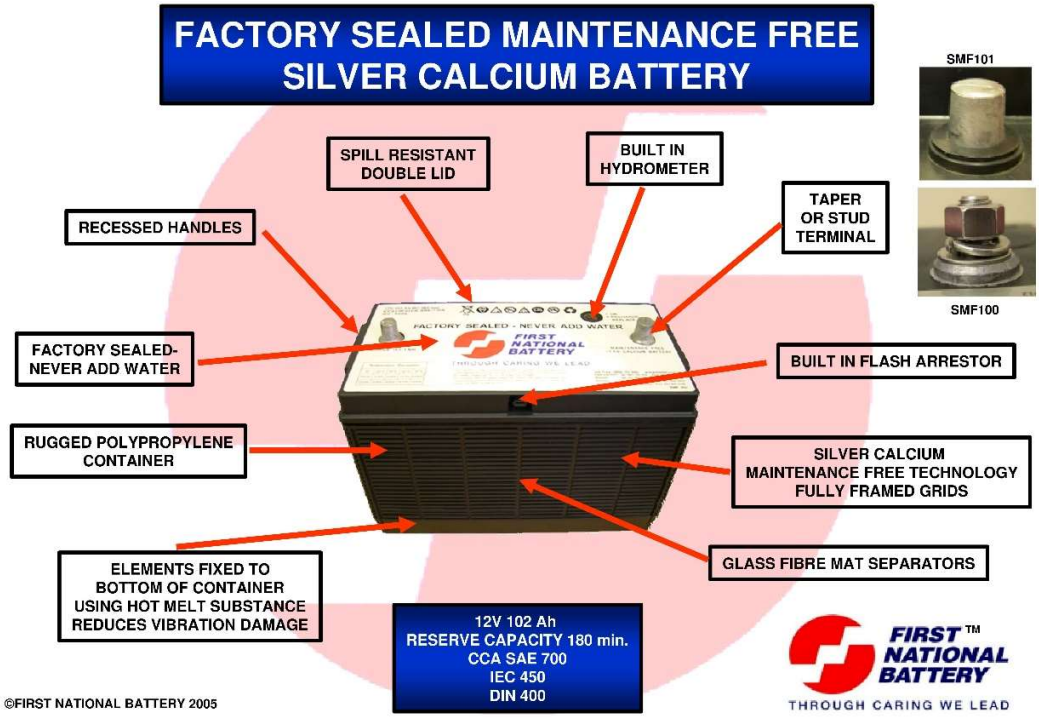
URL:www.ritarpower.com

Address: Rm405,Tower C, Huahan Building,Langshan Rd16, Nanshan District, ShenZhen, 518057, China

Tel:+86-755-33981668 Fax:86-755-8347-5180

2008 - Version I

MIDAS SMF101 12 V 102 Ah SiCa battery information sheet ANNEXURE K



1150K-battery

Features

- Complete protection against reduction of sulfuric acid
- Preventing electrolyte losses by collecting and returning liquid to the reservoir
- Consistent starting performance
- High durability achieved by adoption of special wrought lead calcium grids
- Low resistance envelope separator

1150K-Battery
12V, NUT, 102AH, 240mm (H) 335mm (l), 175mm (w)


SAE post clamp


SAE post & Wing Nut


1150K Nut


1150K to 1111K Converter


J Post

SABMA Code	Item Code	Capacity 20HR Rate	CCA -18°C EN	Dimensions L x W x H mm	Weight Kg	Terminal Layout Type	Terminal Layout
674/Stud	1150K	105A/H	735	331 x 173 x 241	25.9	LHP (Centre)	+ -

LHP: Left hand positive RHP: Right hand positive

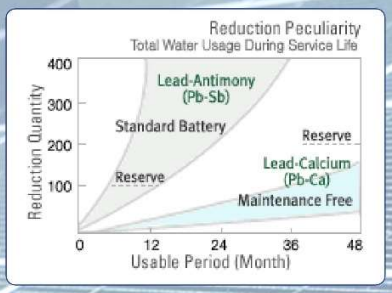
The Royal calcium battery is a general purpose **semi-sealed battery** with a **design life up 3 to 5 years** in standby service.

Royal batteries uses specially **alloyed calcium-lead, which leads to extrememly low levels of "electrolyte decrease"**. Therefore there is no need to supplement distilled water if the charging system remains error-free.

Special liquid-gas separators keeps the electrolyte inside. An electrolyte is any substance containing free ions that behaves as an electrically conductive medium. These separators are also used between the positive and negative plates of a lead acid battery **to prevent a short circuit through physical contact**.

No filler caps are required therefore there is no electrolyte contamination, overwatering or damage in use. Unique wrought **lead-calcium grid design means less internal corrosion and efficient current conductivity for more power and longer life**. It also cuts gassing, resists overcharge,heat and thermal runaway.

Benefits



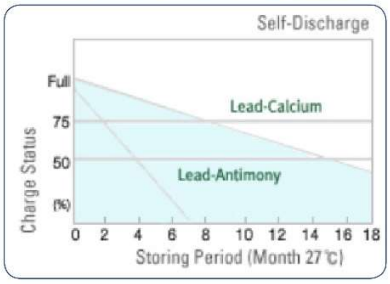
Benefit 1: No need to replenish Distilled Wated

The local action of conventional lead-antimony batteries, due to the effects of the antimony ions during battery use, electrolyzes battery fluid (electrolytes) into oxygen and hydrogen to deplete the battery of fluid. In such conventional batteries, users need to replenish the battery with distilled water or risk the deterioration of battery performance and life Delkor batteries, however, use a special alloy calcium-lead, which leads to extremely low levels of fluid loss. As long as the charging system of the car remains error-free throughout the life of the battery, there is no need to supplement the battery with distilled water.

benefits of calcium LEAD GRID technology

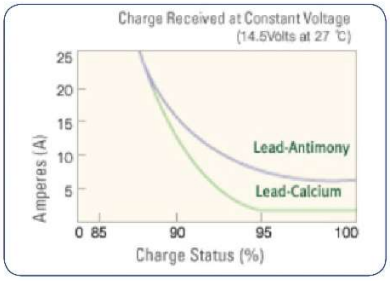
Benefit 2: No Need to Recharge

The phenomenon of self-discharge causes lead-acid batteries to consume charged power, even when the battery is not in use (i.e. during storage). This is due to the impurities contained in the lead alloy, which induces local action and, thus, consumption of electrical energy. Delkor batteries, on the other hand, uses highly-refined, hand-selected lead alloys that render extremely low rates of self-discharge and maintains high battery performance even after long periods of disuse.



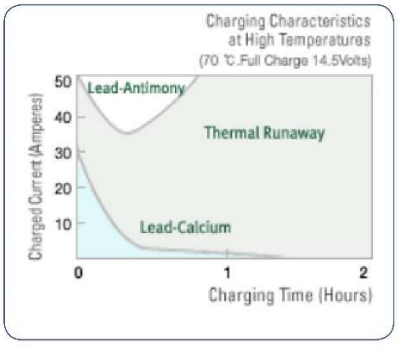
Benefit 3: Prevent Risk of Overcharge

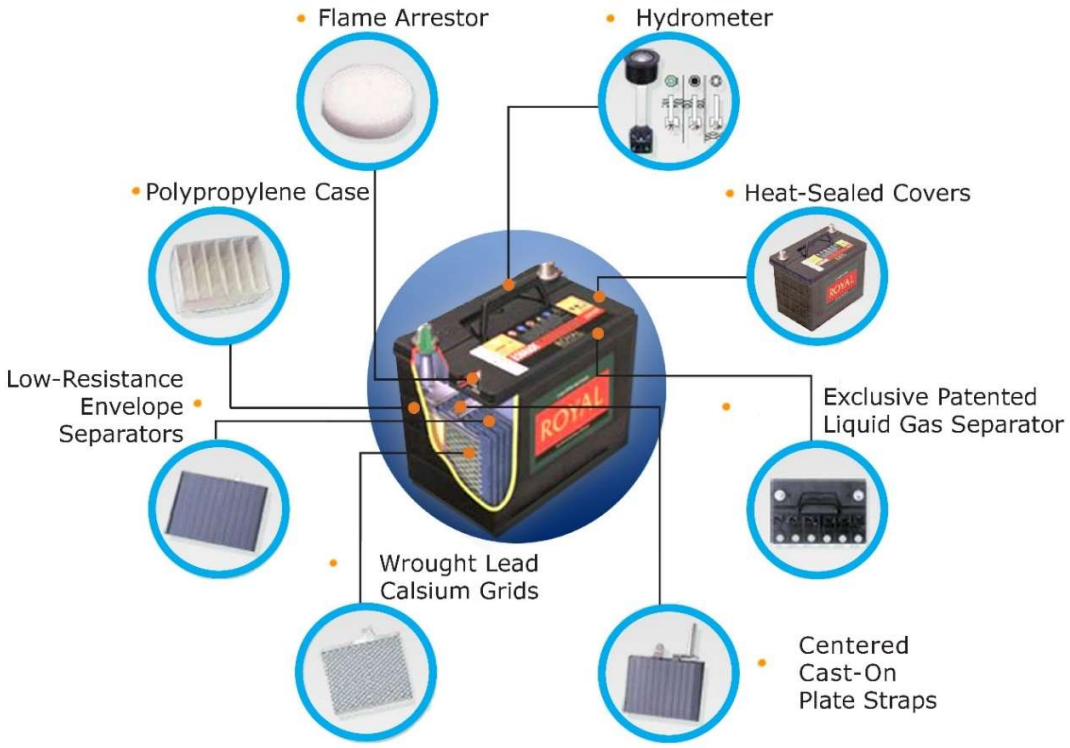
Car batteries can be charged even when the car is in motion. In general, the charged current is adjusted to high or low levels by the voltage regulator. Given the preset voltage in the voltage regulator (14.5V), when a battery is nearly charged to full, the charged current must be reduced to prevent overcharging, which can diminish battery performance. As shown on the graph, the charged current of Delkor calcium batteries are reduced to an extremely low level when the battery is nearly charged to full, thereby minimizing (almost eliminating) the risk of overcharging.



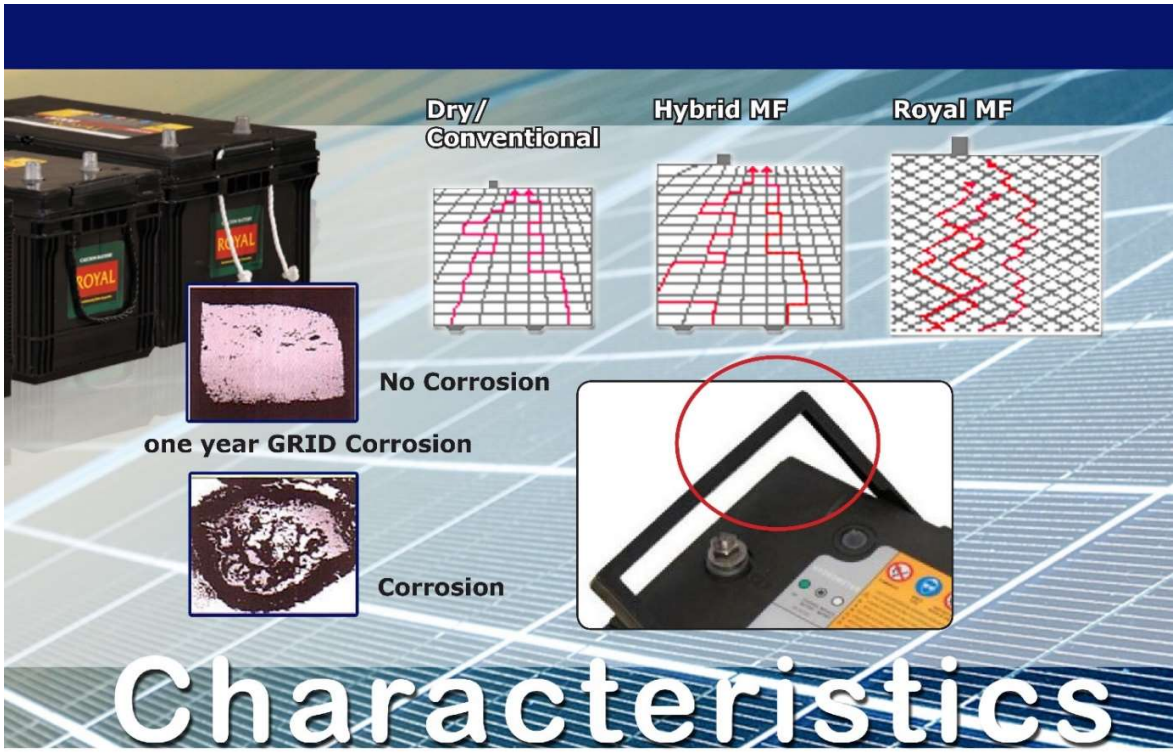
Benefit 4: Thermal Runway

When using the nearly fully charged battery in high temperatures (approximately 70 degrees Celsius), the charged current must be decreased to prevent overcharging and subsequent battery damage. However, in lead-acid batteries, due to the contents of the grid alloy, the charging current decreases during the initial stage, but increases soon thereafter, leading to damages to the gird and deteriorated performance. However, Delkor batteries do not contain such substances and thus, the charged current remains at extremely low levels when the nearly fully charged battery is used in high temperatures to prevent overcharging.





www.rectifier.co.za / www.batterysolutions.co.za



Product Characteristics

No Need for Distilled Water
Delkor batteries use special alloy calcium lead for minimal fluid loss (less than 1/10 of other batteries) meaning that there is no need to replenish distilled water throughout the life of the battery.

Strong Charge
The use of calcium alloy grids and low resistance envelope separators means that Delkor batteries have 20% improved charging ability compared to other batteries, even during intense heat or cold.

Low Rates of Self-Discharge
Calcium alloy grids provide prompt turnover even after long periods of standing.

Mounted Hydrometer
A mounted hydrometer allows you to check the status of the battery.

Long Life
pecial alloy grids prevent corrosion and extend the life of the battery (with) making it the economically practical choice.

Cast Grid Technology		Wrought GRID technology	
Type	**Cat Antimony(Dry/ Conventional)**	**Cast Calsium (Hybrid MF)**	**Wrought Expanded Lead Calsium alloy ROYAL MF**
Technology	• Large Grain Size • Poor Resistance to Deep Corrosion • Poor Resistance to "Buckling" • Loss of physical & Electrical Integrity • Poor High Temperature Performance		• Fine Grain Structure • High Resistance to Corrosion • High Resistance to "Buckling" • Retain physical & electrical integrity • Eliminates Electro chemical effect of Arsenic-Antimony (Gassing, Water loss. Self-Discharge • Improved High Temperature Performance

one year GRID Comparison	
• Deep Penetrating Corrosion • Reduced Electrical Performance • Reduced Physical Strength (broken Grid Wire-Loss of Electrical Contact)	• No deep intergranuiar Corrosion • No loss in performance

DELTEC 12 V 102Ah sealed lead calcium battery datasheet **ANNEXURE L**

WHAT IS UNIQUE ABOUT THE LEAD CRYSTAL BATTERY TECHNOLOGY AS A PRODUCT?

The lead crystal battery technology consists of lead plates, and an acidic solution of SiO_2 as electrolyte. During the initial charge and discharge cycles the electrolyte solidifies and forms a non toxic white crystalline substance. This eventually results in a safe, fluid-less high performance, environmentaly friendly battery.

The lead crystal battery's performance is superior to conventional lead acid batteries. With the following functional advantages:

- **Battery life** – Lead crystal batteries have a float life of 18-20 years at 20°C. Having a battery cycle life of 3 100 (charge discharge) cycles depending on the Depth of Discharge (DOD).
- **Shelf life** – Lead crystal batteries can be stored for 2 years without additional charging. This impacts significantly on rotational charge and logistics.
- **High-rate discharge** – Lead crystal batteries have a discharge rate of up to 10V, without significantly impacting on the battery life.
- **Excellent charge performance** – The lead crystal battery has a charge time, 3-5 times faster than conventional batteries, when charged by conventional means, a generator or solar.
- **Depth of discharge** – The lead crystal battery can be discharged to 0 Volt (100% DOD) and then restored to full rated capacity.
- **Temperature resistance** – Lead crystal batteries operating temperature ranges from -40°C to +65°C. Due to the low internal resistance, the internal temperature remains low when charged and discharged. Tested and cycled at +41°C ambient temperature resulted in only 23% loss of battery life, which is rated between 7 to 10 years. The battery delivers more than 85% of its rated capacity at -40°C.
- **A greener option** – Lead crystal batteries emit no mist or harmful, gaseous emission, as the basic electrolyte is neutral and non-corrosive. Lead crystal batteries will not cause pollution – in line with ever increasing environmental protection requirements (ISO 14001 certification).
- **Safe to transport** – Lead crystal batteries are classified as non-hazardous devices and are safe to transport by land, sea or air.

PRODUCTS

The product range consists of the following:

a. 2 Volt, from 100 Ahr to 3 000 Ahr
b. 6 Volt, from 4 Ahr to 12 Ahr
c. 12 Volt, from 2.3 Ahr to 200 Ahr

BASIC COMPARISON BETWEEN BATTERY TECHNOLOGIES:

ITEM	LEAD ACID	GEL	LEAD CRYSTAL	LITHIUM	SUPERIOR PRODUCT
Range of working temperature	-18°C to +45°C	-18°C to +50°C	-40°C to +65°C	-20°C to +65°C	Lead crystal
Life usage	2-3 years	3-4 years	7-10 years	5-8 years	Lead crystal
Environment	Not friendly	Not friendly	Friendly	Friendly	Lead crystal lithium
Safety transportation	No good	Normal	Good	Good	Lead crystal lithium
Discharge cycle at 80%	450	500	3 100	1 000	Lead crystal lithium
Discharge ability at high current	No good	No good	Good	Normal	Lead crystal
Work ability as a battery pack	OK	OK	Good	Normal	Lead crystal
Cost – value for money	Lower	Low	Slightly more than gel midrange	Much more than gel	Lead crystal

DELTEC LEAD CRYSTAL BATTERIES
LEAD CRYSTAL RANGE

The Deltec lead crystal range has been specifically created for deep cycle, applications resulting in extended battery life and reliability and signals a break through in superior battery solutions.

Because of the ability of the Deltec lead crystal range of batteries to discharge to such a very low level, system designers have more flexibility in their design parameters which results in a far more cost effective system.

Exclusive lead crystal technology optimizes battery life, power capacity and reliability far more than conventional lead acid batteries.

The robust and long lasting design of the Deltec lead crystal range has resulted in a single range that can be used in multiple applications; mobile telecoms, fixed telecoms, ups, solar, power utilities, military communications, network communications, data transmission, television signal transmission, recreational golf carts and wheel chairs.

THE ONE STOP SOLUTION TO VARIED APPLICATIONS

The Deltec lead crystal range is designed and engineered to offer reliable maintenance free back up power for renewable energy applications where frequent deep cycles are required and where remote sites need not be visited or maintained for complete peace of mind.

The Deltec lead crystal range is approved for non-hazardous cargo for ground, sea, and air transport – dot 49 cfr173.159 (D), (i) and (ii).

TECHNICAL FEATURES

PLATES AND GRIDS
- Extra thick plates with grids cast from high purity lead calcium selenium alloy to ensure an extended life.
- The lead crystal battery positive grid alloy contains tin and calcium. This alloy is used to increase the plate resistance to corrosion and improve deep cycle performance
- The lead crystal battery uses a lead alloy combination in the negative grid plates. This alloy improves resistance (lowers internal resistance) and improves the charge acceptance.

SEPARATORS
- Micro porous high absorbent mat (patented)
- Polyethylene envelope separators

CONTAINERS AND LIDS
- Made from thick walled ABS plastic, for unsurpassed strength.
- Lids are heat sealed for added strength, durability and quality. Making every battery 100% leak proof.
- Lead crystal battery cases are made of Polycarbonate/Acrylonitrile Butadiene Styrene (PC/ABS) – A blend of PC and ABS that creates a stronger flame retardant plastic.

TERMINALS
- Threaded post terminals with brass inserts allowing for better conductivity and maximum torque retention. Embedded M8 brass terminals are sealed with double seal O-rings and epoxy resin.

HANDLES
- Handles are integrated in the case, being either rope or plastic for ease of carrying and fold away neatly when not needed.

SAFETY VALVES
- Due to the low gassing of the lead crystal batteries there are only pressure release valves on the battery, with no need for flash back arrestors as the batteries generate marginal amounts of hydrogen.
- According to tests performed by SGS (CE authorized) testing facility, the quantity of gas emitted during the chemical reaction phase (Charging phase – Discharge phase) by the lead crystal batteries is only 1/200 of a normal lead acid battery or AGM batteries. This is a very small amount of gas, making it safe for use. Our batteries pose no risk of explosion. It is very safe. There is no need for a flame arrestor.
- Due to the crystallization process that occurs in the battery during its life, the lead crystal batteries only emit 0.008ml of gas during the charge cycle and not during the discharge or storage cycles. The lead acid and gel batteries emit 0.037ml and 0.034ml of gas during all 3 cycles.

DELTEC LEAD CRYSTAL RANGE IS MANUFACTURED TO THE HIGHEST STANDARDS AND HAS BEEN EXTENSIVELY FIELD TESTED. THIS ENSURES:
- Longer life
- DOD to 100% of stated capacity
- Restores itself to full stated capacity after second charging cycle
- Operating temperatures of -40°C and +65°C
- Double the cycles
- Quicker charge rate

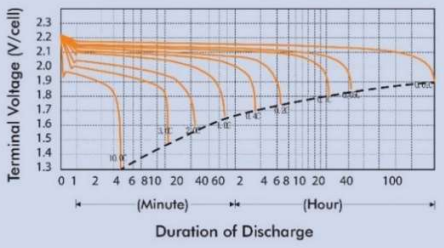
PRODUCT FEATURES

- Longer life
- Versatile use across applications
- Cost effective
- Reliable
- Non-hazardous transport ability
- IEC 60896-21-22 compliant
- Field tested
- Conforms to ISO 9001
- Conforms to ISO 14001
- Can be installed vertically, horizontally or inverse (not that you would want to)
- Electrical characteristics

DELTEC LEAD CRYSTAL RANGE

SPECIFICATION CHARTS

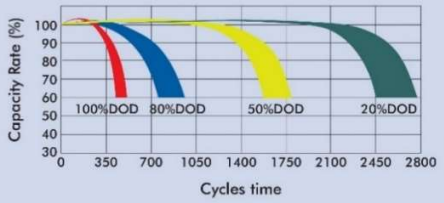
DISCHARGE CHARACTERISTICS 77˚F (25˚C)



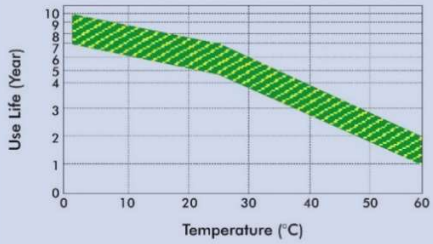
DISCHARGE CURRENT AND FINAL DISCHARGE VOLTAGE

DISCHARGE CURRENT (A)	FINAL DISCHARGE VOLTAGE (V/CELL)
0.05C or below or intermittent discharge	1.9
0.05C of current close to it	1.85
0.1C of current close to it	1.75
From 0.2C to 0.5C	1.7
From 0.5C to 1C	1.6
From 1C to 3C	1.5
Current in excess of 3C	1.3

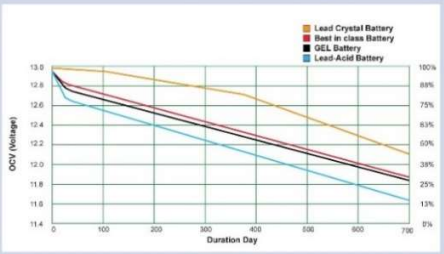
LIFE CYCLE CURVES



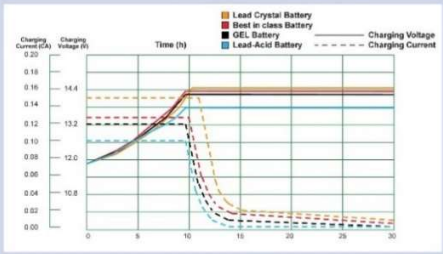
FLOAT SERVICE LIFE



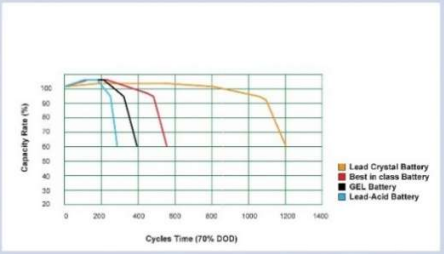
COMPARISON GRAPHS: SELF DISCHARGE CURVE (25˚C)



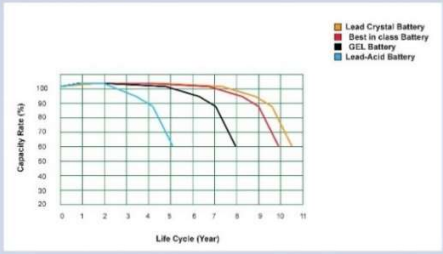
COMPARISON GRAPHS



COMPARISON GRAPHS: CYCLE LIFE CURVES (25˚C)



COMPARISON GRAPHS: CYCLE LIFE CURVES (25˚C)



THE CAPACITY AND SIZES OF LEAD CRYSTAL BATTERIES

			Rated	Rated	Out	Line	Size	(2mm)	Weight for
	No.	Type	Voltage (V)	Capacity (Ah/10hr)	L	W	H	Total H	Reference (kg)
6V DELTEC LEAD CRYSTAL BATTERY	1	3-CNFJ -7.2	6	7.2	151	35	84	100	1.35
	2	3-CNFJ -10	6	10	151	50	94	100	2
	3	3-CNFJ -12	6	12	151	50	94	100	2.1
12V DELTEC LEAD CRYSTAL BATTERY	4	6-CNFJ -2.3	12	2.3	180	35	61	67	0.98
	5	6-CNFJ -7.2	12	7.2	151	65	94	100	2.3
	6	6-CNFJ -10	12	10	151	99	94	100	4
	7	6-CNFJ -12	12	12	151	99	94	100	4.15
	8	6-CNFJ -14	12	14	151	99	98	104	4.35
	9	6-CNFJ -18	12	18	181	76	170	170	6.5
	10	6-CNFJ -22	12	22	181	76	170	170	6.8
	11	6-CNFJ -24	12	24	175	166	125	125	7.8
	12	6-CNFJ -28	12	28	175	166	125	125	8.5
	13	6-CNFJ -28	12	28	185	105	130	135	7.7
	14	6-CNFJ -35	12	35	194	132	172	190	11.4
	15	6-CNFJ -40	12	40	198	166	172	172	14.2
	16	6-CNFJ -55	12	55	229	138	210	220	18.4
	17	6-CNFJ -65	12	65	348	167	175	175	22
	18	6-CNFJ -70	12	70	259	169	206	210	23
	19	6-CNFJ -90	12	90	306	169	206	210	23
	20	6-CNFJ -100	12	100	408	174	211	234	33
	21	6-CNFJ -120	12	120	408	174	211	234	37
	22	6-CNFJ -150	12	150	486	170	241	241	45
	23	6-CNFJ -180	12	180	522	240	219	240	61
	24	6-CNFJ -200	12	200	522	240	219	244	64
2V DELTEC LEAD CRYSTAL BATTERY	25	CNFJ -100	2	100	171	72	205	210	7
	26	CNFJ -200	2	200	176	110	330	365	15
	27	CNFJ -300	2	300	176	154	330	365	22
	28	CNFJ -400	2	400	210	175	330	365	28
	29	CNFJ -500	2	500	244	175	330	365	32.5
	30	CNFJ -600	2	600	301	175	330	366	38.5
	31	CNFJ -800	2	800	410	175	330	366	55.5
	32	CNFJ -1000	2	1000	475	175	330	365	65
	33	CNFJ -1500	2	1500	401	351	342	78	110
	34	CNFJ -2000	2	2000	491	351	344	383	130
	35	CNFJ -3000	2	3000	712	353	341	382	220

DELTEC LEAD CRYSTAL FRONT TERMINAL BATTERY

6-CNFJ-170

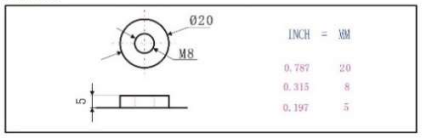
Specifications

Nominal Voltage		12V
Rated Capacity(10 hour rate)		170AH
Dimension	Total Height (with terminals)	320mm(12.6inches)
	Height	320mm(12.6inches)
	Length	560mm(22.05inches)
	Width	125mm(4.92inches)
Weight		Approx. 60kg(132.16Tbs)

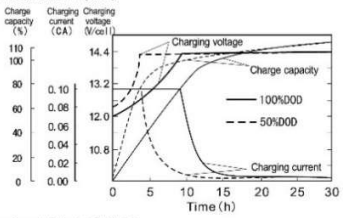
Characteristics

Capacity 77°F(25℃)	120 hour rate (1.8A)	216AH
	20 hour rate (9.5A)	190AH
	10 hour rate (17A)	170AH
Internal Resistance	Full charged Battery 77°F(25℃)	3mΩ
Self-Discharge 77°F(25℃)	Capacity after 3 month storage	95%
	Capacity after 6 month storage	85%
	Capacity after 12 month storage	80%
Max. Discharge Current 77°F(25℃)		1800A(5S)
Terminal	Standard	F4
	Optional	
Charging (Constant Voltage)	Cycle	Initial Charging Current 54A or small 14.4V~14.8V/77°F(25℃)
	Float	13.5V~13.8V/77°F(25℃)

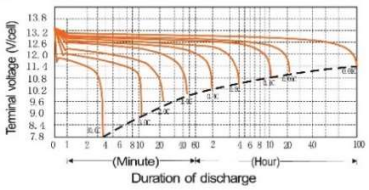
Terminal (F4)



Charge characteristics 77°F(25℃)



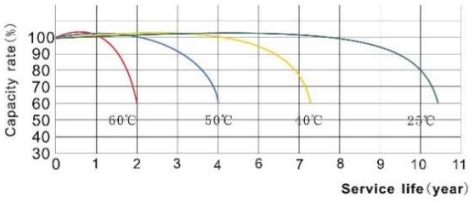
Discharge characteristics 77°F(25℃)



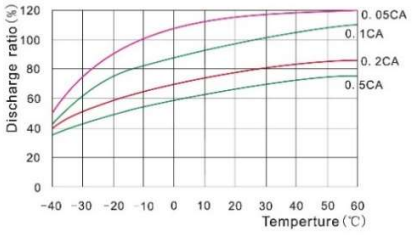
Discharge current and final discharge voltage

Discharge current(A)	Final discharge voltage(V/cell)
0.05C or below or intermittent discharge	11.4
0.05C of current close to it	11.1
0.1C of current close to it	10.8
0.2C of current close to it	10.5
From 0.2C to 0.5C	10.2
From 0.5C to 1C	9.6
From 1C to 3C	9.0
Current in excess of 3C	7.8

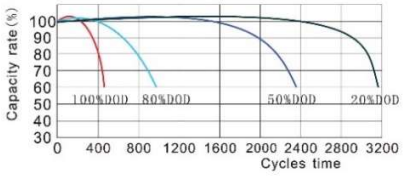
Temperture and float service life



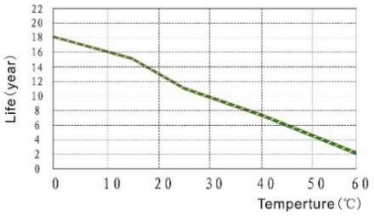
Temperture and discharge capacity



Cycle life curves(25℃)



Float service life



COMPARISON: LEAD CRYSTAL BATTERIES VERSUS OTHER BATTERY TYPES

PARAMETERS	SPECIFICATIONS	LEAD CRYSTAL BATTERIES (YES/NO) - DETAILS
Battery Type	Cyclic Valve Regulated Lead Acid VLRA Gel Type - Gel Tubular OPZV - or other technologies	Yes - New Technology – Valve Regulated Lead Crystal Batteries
Battery nominal volts	48V	Yes - (48V) full charged 2.255 volt per cell 54.13 volt per bank
Battery Capacity	300Ah / 600Ah / 900Ah / 1200Ah	Yes - 300Ah / 600Ah / 900Ah / 1200Ah lead times differ
Application	Cyclic: 2 cycles /day up to 80% DOD	Yes - This has been done in our POC and research site, DOD 100% 2 cycles per day 110 x 2volt/3 000Ah cells in series. 3 Months no signs of deterioration 6 months no deterioration.
Max. foot print	Manufacturer to specify	Yes - Lead crystal batteries conform to standard rack dimensions
Battery container	Poly Propylene Fire retardant -URL 94V	Yes - Standard
Operating Temperature	25 to 35°C	Yes - Lead crystal batteries range is -45°C to +65°C
Compliance	TEC certification/any international standards body certification	Yes - Lead crystal batteries are CE certified and tested according to EN-61000-6-1:2007, EN-61000-6-3:2007, CISPR 16-1-2:2006, CISPR 16-2-1:2005, IEC61000-4-2:2001, IEC61000-4-3:2008
Float Charge / Cell	Manufacturer to specify (Airtel desire 2.27 volts per cell @ 25°C for 48V)	Yes - Lead crystal batteries (2.25 - 2.30 volt per cell @ 25°C for 48V pack)
Boost Charge / Cell	Manufacturer to specify	Yes - Lead crystal batteries (2.40 - 2.48 volt per cell @ 25°C for 48V pack)
End Voltage / Cell	1.75V @ 10 hour rate of discharge at 27°C	Yes - Lead crystal batteries conform (1.75 - 1.80 volt)
Nominal Voltage	2.0V	Yes - (2.0 volt)
Open Circuit Voltage	2.1V	Yes - 2.1 to 2.20 volt per cell
Service Life (As per TEC test method at 80% DOD)	3 000 cycles	Yes - Lead crystal batteries at 20% DOD 3150 Cycles, at 80% DOD 1150 Cycles
Regular depth of discharge feasible	80 - 100%	Yes - Lead crystal batteries can achieve these targets
Charge / Discharge curves and Cyclic life vs depth of discharge at 25 & 35°C temp.	To be provided	(To be provided)
Acceptance Procedure	1. During the test individual cell voltage should not vary more than 0.05V from the Avg. cell voltage 2. Test to be conducted for 0.1°C, 0.5°C as well as 1°C capacity	Yes - Lead crystal batteries conform
Self discharge / month % of c 10 capacity	less than 5 %	Yes - Lead crystal batteries self discharge is less than 2% per month
Recharge	Suitable for recharging at 20% of AH capacity	Yes
Efficiency of gas recombination cycle	Greater than 98%	Yes - Lead crystal batteries conform
Battery Terminals	The battery should be of a sealed maintenance free type with front administered terminals	Yes - Lead crystal batteries conform
Storage	The batteries shall be capable of being stored for up to six months from the date of delivery, without losing more than 30% of its full capacity charge at a maximum of 25°C	Yes - Lead crystal batteries conform less than 30% after 12 months of storage, battery can be discharge 100% in storage and charged back to full capacity with no effect to battery life
Product Markings	The polarity marking of both the negative and positive terminals shall comply with IEC 896-21. Each battery block shall be provided with a bar-coded serial number for asset management purposes.	Yes - Lead crystal batteries conform

COMPARISON: LEAD CRYSTAL BATTERIES VERSUS OTHER BATTERY TYPES (continued)

PARAMETERS	SPECIFICATIONS	LEAD CRYSTAL BATTERIES (YES/NO) - DETAILS
Interconnection	All the necessary inter-cell and inter-row connectors, terminal take-off plates, nuts, bolts and washers shall be supplied with each battery string as per the ordering requirement. All interconnections and cell/ monobloc terminals shall be insulated against accidental short circuits, but shall allow access to the terminals for voltage readings, without the need to remove the insulation.	Yes - Lead crystal batteries conform
Safety	Protection against internal ignition from external spark sources shall comply with IEC 896-21. Suppliers complying with this clause shall supply certification. The valve operation of all products shall comply with EC 896-22. Suppliers complying with this clause shall supply certificate.	Yes - Terminals are designed to have a flash back prevention, lead crystal batteries emits virtually no gas or vapour
Battery Rack - General (Shelter Indoor Usage) – Cost to be quoted separately	Manufacturer to specify	Yes
Battery Rack - Dimensions	Manufacturer to specify	Yes
Battery Rack - Protective Coating	All shelves shall be powder coated, and special care shall be taken to prevent the ingress of electrolyte into any joints and crevices	Yes
Warranty	The batteries shall have a minimum warranty period of at least 3 years from date of delivery	Yes - A 3 year warranty is provided against manufacturing defects that cause or contribute to poor performance; not against performance criteria
State of Charge vs On Voltage Graph at C5 rate of discharge		(To be provided)
Wh Efficiency of Normal Battery @ 100% DOD		96% Efficiency
Wh Efficiency of SRS Profile @ 100% DOD		85% Efficiency
Recharge time to 96% SoC		Fully discharged, with 0.25C initial current and constant voltage 2.4V/cell charging time in 12 hours. This level is reached within 45 minutes during fast charge.
Charge Efficiency		Less than 20% SOC, the charging efficiency is greater than 98%

DELTEC LEAD CRYSTAL RANGE – TYPICAL APPLICATIONS:
UPS, TELECOMS, POWER UTILITIES, RAILWAY SIGNALS, SOLAR, GOLF CARTS, WHEEL CHAIRS, GENERATORS, WIND TURBINES, STREET LIGHTING, SOLAR HOME SYSTEMS, ALARM INSTALLATIONS, TRAFFIC LIGHTS, PUMP SYSTEMS, SURVEY AND MAPPING SYSTEMS, HYDRO SYSTEMS, CCTV SYSTEMS, MARINE INSTALLATIONS, AIRCRAFT SIGNAL SYSTEMS

ZLI012018 12 V 16Ah Zenith lithium-ion phosphate battery datasheet ANNEXURE M

NO.	Items		Caratteristiche / Characteristics	Modalità di test / Testing Methods
1	Tensione nominale / Nominal Voltage		**12V**	《GB/T18287-2013》 Follow GB/T18287-2013》
2	Capacità nominale / Nominal Capacity		**16Ah**	《GB/T18287-2013 》 Follow 《GB/T18287-2013》
3	Minima capacità / Minimum Capacity		**15Ah**	《GB/T18287-2013 》 Follow 《GB/T18287-2013》
4	Impedenza interna della batteria/ Battery internal Impedance		**≤55mOhm**	
5	Valori di tensioni accettati per la spedizione / Shipment Voltage		**12.8～13.6V**	Multimetro / Multi-meter
6	Dimensioni / Dimensions	Larghezza / Length	**166x175x126 hmm**	
		Profondità / Width		
		Altezza / Height		
		Peso /gross weight	**Approx.kg 2,4**	
7	Terminale/Terminal			
8	Temperatura di lavoro Working Temperature	In carica/ Charge	**0~45℃、45~85%RH**	
		In scarica / Discharge	**-20~55℃、45~85%RH**	

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9	Temperatura e umidità di stoccaggio/ Storage Temperature & Humidity Range	Oltre un mese / above one month	**-20~+55℃、45~85%RH**	Termometro e igrometro / Temperature & Humidity Instruments
		Oltre tre mesi / above three months	**0~+45℃、45~85%RH**	
		Oltre un anno / above one year	**+5~+30℃、45~85%RH**	
10	Massima corrente costante di carica / Allowed maximum continuous charge current		**15Amp**	Multimetro / Multi-meter
11	Massima corrent costante di scarica / Allowed maximum continuous discharge current		**30Amp**	
12	Allowed maximum reverse charge voltage		NO Allowed	
13	Massima tensione in carica / Allowed maximum charge voltage		**14.6±0.1Volt**	Multimetro / Multi-meter
14	Tensione minima in scarica / Discharge cut-off voltage		**<10Volt**	Multimetro / Multi-meter
			Ripristino automatico Recovering condition	Scollegare dal carico attendere che il BMS chiuda il circuito e ricaricare Unplug all the load waiting for BMS signal and charging
15	Limitine delle extra correnti Over Current Protection		**65Amp**	Scaricare per 2sec. con un carico da 65Amp. Discharge with **65A** for about 2 sec.
16	Protezione contro extra correnti Over current protection		**10~40ms**	Ritardo intervento Time of delay
			Ripristino automatico Recovering condition	Corrente inferiore al limite ammesso Current lower than protection.
17	Protezione contro I corti circuiti Short circuit protection		Collegare in corto circuito una resistenza da 0.05Ω per un'ora. Use a resistor with less than 0.05Ω to make the battery short circuit for 1 hour.	
			Recupero automatico. Recovering condition	Rimuovere la condizione di corto circuito No short circuit condition

18	Cicli (stimati). Capacità residua >75% Estimated cycles. Remaining capacity >75%	3000	-50% D.O.D. (profondità di scarica) - 25°C - 10A corrente di scarica/discharge current - 4A corrente massima di carica/max charge current
		2500	-80% D.O.D. (profondità di scarica) - 25°C - 20A corrente di scarica/discharge current - 4A corrente massima di carica/max charge current
		2000	-80% D.O.D. (profondità di scarica) - 25°C - 20A corrente di scarica/discharge current - 20A corrente massima di carica/max charge current
		1500	-100% D.O.D. (profondità di scarica) - 25°C - 20A corrente di scarica/discharge current - 4A corrente massima di carica/max charge current
		1000	-100% D.O.D. (profondità di scarica) - 25°C - 20A corrente di scarica/discharge current - 20A corrente massima di carica/max charge current
19	Effetti della temperatura sulla capacità Battery capacity Vs. room temperature	55°C: 95% 25°C: 100% 0°C: 80% -20°C: 60%	Lasciare la batteria per due ore alla temperatura indicate e scaricarla con 4A fino alla tensione minima. Store the battery for 2h at the indicated temperature and discharge with 4A down to the minimum voltage.
20	Capacità residua (batteria a magazzino o non utilizzata) Charge retention (stored or not used batteries)	>90%	Batteria carica, dopo un mese a 25°C. Ricaricare la batteria ogni 3-4 mesi Fully charged battery, after one month at 25°C. Recharge the battery every 3-4 months

Zenith

Modalità di utilizzo / *usage modalities*

- Prima di utilizzare la batteria, leggere le avvertenze riportate e le Informazioni tecniche applicate sulla batteria. Verificare che il carico collegato alla batteria sia compatibile con la batteria stessa
  Before use, please carefully read the handling instructions and the marks on the battery. Check the load is compatible with the battery.
- Tenere lontana la batteria da fonti di calore, ambienti elettrostatici, alta tensione ed evitare che venga utilizzata da bambini. Non colpire la batteria.
  During use, please far away from heat source, electrostatic place, high voltage and avoid children to use. Don't beat battery.
- Ricaricare la batteria con il caricabatteria appropriato e non lasciarla in carica oltre 24ore.
  Please use the special charger to charge the battery, and don't put the battery in the charger more than 24 hours.
- Non collegare in corto circuito I due poli della batteria. Non bagnarla ne danneggiarla.
  Do not make the positive (+) and negative (-) terminals short circuit. And do not wet the battery , or will have dangers.
- Stoccarla adeguatamente se non utilizzata per lunghi periodi, evitando di lascarla scarica. Evitare di lasciarla sotto il sole ed utilizzare luoghi freschi ed asciutti. Evitare di danneggiarla con oggetti metallici.
  Please store the battery well if don't use in a long time. Please keep the battery in half charge , that is to say don't charge fully and don't discharge completely. Please avoid to touch with metal to damage the battery. Please store the battery in shade, cool and dry place.
- Non mettere la batteria nel fuoco o nell'acqua. Maneggiare con sicurezza la batteria vecchia.
  Do not put the battery into a fire or water, and please safely deal with the disuse battery.
- Non caricare la batteria in ambienti con temperature superiori a 50°C.
  Don't charge the battery in environments where the temperature is over 50°C.
- Non generare inversioni di polarità durante l'utilizzo della batteria.
  Don't reverse the two electrodes when use the battery.
- Non perforare la batteria.
  Don't penetrate the battery with sharp things
- Non smontare la batteria
  Do not disassemble the battery.
- Sostituire la batteria una volta che la stessa ha esaurito la sua vita
  Battery has usage cycle life, if its using time is quite little than usual, please change your battery
- Non saldare I poli della batteria
  Don't weld the battery directly .

Zenith

- Non utilizzare la batteria se deformata
  Don't use the battery with seriously scratch and distortion.
- Chiedere a U.B.S. UNION BATTERY SERVICE l'approvazione per eventuali collegamenti in serie/parallelo.
  Ask for U.B.S. UNION BATTERY SERVICE permission is case of use of batteries connected in series or in parallel
- Non utilizzare la batteria se trovata troppo calda, se emana odore, se il contenitore ha cambiato colore o si è deformata.
  Please stop using if you find the battery heat, smell odor, change color, distort or other abnormal states.
- Allontanarsi dalla batteria se si verificano perdite di acido. Manipolarla solo se muniti di idonei strumenti di protezione individuali
  Please far away from the battery if you find leakage. Touch the battery only if properly protected
- In caso di contatto con l'elettrolita uscito dalla batteria, lavarsi con acqua
  Please wash with clean water if the electrolyte leak on your skin or clothes
- Se gli occhi vengono a contatto con l'elettrolita, risciacquarli con acqua e consultare un medico
  If the battery leaks, and the electrolyte get into the eyes. Do not wipe eyes, instead, rinse the eyes with clean water, and immediately see a doctor