Design and Development of a High-Frequency Mosfet Driver

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Declaration

I Arthur James Swart hereby declare that the following research information is solely my own work. This thesis is submitted for the requirements for the Magister Technologiae: Engineering: Electrical to the department of Applied Electronics and Electronic Communication at the Vaal University of Technology, Vanderbijlpark. This dissertation has never before been submitted for evaluation to any educational institute.

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Arthur James Swart

08 November 2004

Acknowledgements

I want to hereby acknowledge Dr. Christo Pienaar for his contribution to the success of this project. His continued encouragement and interest helped me surge ahead, continuing to search for answers to the relevant questions at hand. His advice and experience proved especially valuable when I was designing the Mosfet driver stage, and finally in examining what the expected results should look like.

Dedication

This project is dedicated to my dearly loved wife, Charmain.

Abstract

A high-power Mosfet was incorporated as a switching device into the efficient Class E configuration, where the switching device switches current through itself either completely on or completely off at high frequencies.

The first objective of this project was to demonstrate the effectiveness of a phase-lock loop circuit in generating stable high frequencies when connected in an indirect frequency synthesizer configuration. The indirect frequency synthesizer has established itself as a versatile frequency generator capable of generating high frequencies based on a lower stable reference frequency. The frequency generation stage incorporates a phase-lock loop circuit, a frequency divider and a stable reference frequency section. The phase-lock loop section incorporates the TTL based 74HC 4046 that is based upon the common CMOS 4046 integrated circuit. The frequency divider section is built around the CMOS-based 4526 whilst the reference frequency section incorporates the CMOS-based 4060. The frequency synthesizer produced a range of frequencies from 50 kHz to 8 MHz in 50 kHz steps. The output voltage was constant at 5,5 V.

The second objective was to show that the complementary emitter follower is indeed a worthy Mosfet gate drive circuit at high frequencies. The Mosfet driver stage produced a voltage signal of at least 11 V, being able to source and sink relatively high peaks of current, especially at high frequencies. Voltage amplification occurred through the use of multiple CMOS-based 40106 inverters. The complementary emitter follower, known for its low output impedance and its ability to source and sink large amounts of current, was an important component in the final Mosfet gate section.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ANNEXURES

GLOSSARY OF ABBREVIATIONS AND SYMBOLS

A

A - Amperes

AM - amplitude modulation

B

BV_{PP} - Mosfet breakdown voltage in V

C

C - Coulomb

C_{DG} - capacitance between the Mosfets drain and gate in pF

C_{GS} - capacitance between the Mosfets gate and source in pF

C_{iss} - the input gate capacitance of the Mosfet in pF

CMOS - complementary metal oxide semiconductor

D

d - Mosfet drift region thickness in μm

DDS - Direct digital synthesis

E

E_{gate} - energy expended in the Mosfet gate in J

EXOR - exclusive OR gate

F

f - the input gate frequency in Hz

f_L - the lock range frequency in Hz

FM - Frequency modulation

F_{out} - the VCO output frequency in Hz

F_{ref} - the input reference frequency to the phase comparator in Hz

FSK - frequency shift key

f_T - transit time limited frequency response

G

GND - ground

g_{fs} - Mosfet transconductance

H

Hz - Hertz

I

I - the input Mosfet gate current in A

IC - integrated circuit

IGBT - insulated gate bipolar transistor

I_0 - drain current set by the load impedance

J

J - Joule

J-K - a 5 input flip-flop device

K

K_f - low-pass filter transfer gain

K_n - inverse of the maximum or minimum divider ratio

K_p - phase comparator gain

K_v - VCO gain

kΩ - kilo Ohm being 10^3

kHz - kilo hertz being 10^3

L

L - Mosfet channel length in μm

LF - low-pass filter

M

m - meter

MHz - Mega Hertz being 10^6

N

N - the division factor

O

P

PD - phase detector

PFD - phase frequency detector

P_{gate} - powered consumed in the Mosfet gate in W

pF - pico farad being 10^{-12}

PLL - phase-lock loop

PSU - power supply unit

Q

Q_{gate} - Mosfet gate control charge in C

R

rad - radians

$R_{G(int)}$ - the internal resistance of the Mosfet gate in Ω

R_s - the external resistance to the Mosfet gate in Ω

S

s - seconds

T

t - settling time

t_1 - the positive time period of the frequency in s

TTL - transistor-transistor logic

U

μH - micro Henry being 10^{-6}

V

V - Voltage

VCC - supply voltage V

VCO - voltage controlled oscillator

V_{gs} - the gate to source voltage V

V_T - Mosfet threshold voltage

W

W - Watt

X, Y, Z

Symbols

Ω - Ohms

τ_1 - the time constant set by R3 and C2 (to give the roll off rate) in s

τ_2 - the time constant set by R4 and C2 (to give the roll off rate) in s

ξ - the damping ratio

μ - micro being 10^{-6}

ω_n - natural frequency

Chapter 1 Introduction

1.1 Background

The generation of high frequencies has become part of mankind's history, especially since the advent of the amplitude modulated radio at the beginning of the 20th century. Initially, radio receivers primarily utilized amplitude modulation (AM) to modulate a high carrier frequency with a lower audio frequency. In the latter part of the 20th century, a demand arose for the generation of specific stable frequencies, at specific power levels, thus meeting the needs of an ever-changing technological age. High-frequency generation has now become a primary part of today's radio communication field, featuring prominently in many frequency modulation systems, otherwise referred to as FM systems. Numerous other fields, such as the dielectric heating of materials, have also come to include some or other form of frequency generation. These high-frequency components must contain sufficient energy to be utilized effectively. The appearance of the high-power Mosfet in the latter part of the 20th century made it possible to amplify these high-frequency components to specific levels of usefulness.

1.2 Purpose

The purpose of this research project is to design and develop a high-frequency Mosfet driver capable of driving high-power Mosfets, primarily within Class E configurations. The high-frequency Mosfet driver must exhibit a high degree of frequency stability over the range of 50 kHz to 8 MHz in 50 kHz steps. A selected frequency signal within this range must then be able to successfully drive the gate of a high-power Mosfet that will feed the load.

1.3 Methodology

The design and development of a high-frequency Mosfet driver for use in high-frequency high-power Mosfet applications will be addressed in the following manner. Firstly, an in-

depth literature study will be conducted on various frequency synthesizers. This will then be followed by the design and construction of the high-frequency generator utilizing an indirect frequency synthesizer built around the TTL based 74HC 4046 phase-lock loop, hereafter called PLL. A literature study will then be conducted on Mosfet driver devices. The following step will be to design and construct the Mosfet driver stage by incorporating a complementary emitter follower. A simulated model of the Mosfet driver stage will then be investigated. Finally, the results of the completed high-frequency Mosfet driver will be obtained and analysed. The conclusions and recommendations will then follow, being based upon the analysis of the results.

1.4 Delimitations

The design and development of the Class E high-power Mosfet amplifier does not form part of this research document. The design and construction of the power supply unit (PSU) for the high-frequency Mosfet driver will also not be included in this research.

1.5 Definition of terms

Frequency synthesizer: A device that can produce a large number of output frequencies from a smaller number of fixed-frequency oscillators (Blake 2002:94).

Mosfet driver: An electronic device capable of delivering sufficient charge to the gate of a high-power Mosfet so as to switch it completely on or completely off.

1.6 Importance of the research

High-power Mosfet amplifiers are becoming increasingly widespread, particularly in the use of dielectric heating of materials. The Mosfet devices used in these amplifiers are fairly economical and ideally suited to low-frequency applications. This project will

address the current need for the successful switching of these high-power Mosfets at higher frequencies, particularly within the Class E amplifier environment.

This research project will also address the need for a simplified, economically viable frequency synthesizer to cover the high-frequency spectrum of 50 kHz to 8 MHz in 50 kHz steps. This type of frequency synthesizer can then be utilized as the source signal to various communications equipment in a communications laboratory.

1.7 Overview of the report

The project can be divided into two stages, namely the frequency generation stage and the Mosfet driver stage. Figure 1 illustrates these two stages and their relevant sections by means of a flow diagram.

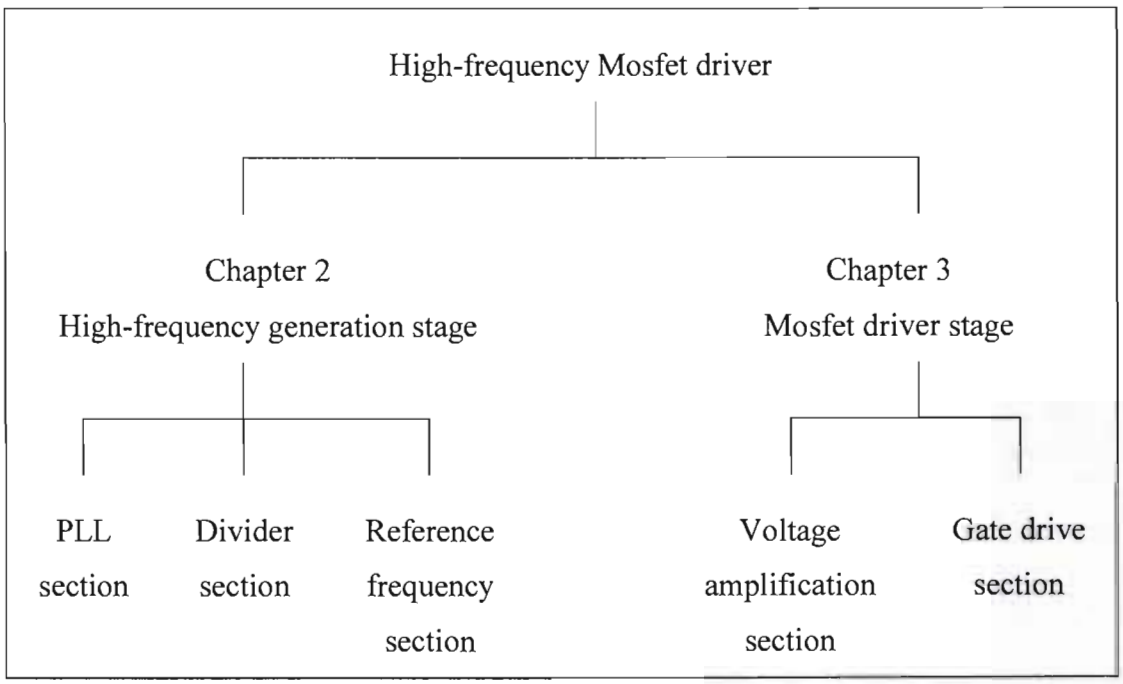

Figure 1 Flow diagram of the design of the high-frequency Mosfet driver.

The design and development of the high-frequency Mosfet driver will start in chapter 2 with a discussion on coherent and incoherent frequency synthesizers. The choice of a coherent indirect frequency synthesizer utilizing a PLL, programmable divider and stable

reference frequency will finally be considered as a possible high-frequency generator. Problems associated with stability and frequency division will be analysed. The design and development of this indirect frequency synthesizer will then be discussed as part of the frequency generation stage.

Chapter 3 will contain an in-depth view of circuits and techniques currently employed to successfully drive high-frequency high-power Mosfets. A voltage amplification section utilizing the HEX inverter 40106 will be investigated to ensure a 12 V input signal to the final gate drive section. The gate drive section incorporating a complementary emitter follower will then be addressed. The final gate drive circuit will also be reviewed by means of a simulation model.

The combination of the frequency generation and gate driver stages will be presented in chapter 4. The results from the final completed high-frequency Mosfet driver will be presented and analysed. The simulated model's result of the gate drive section will also be analysed and discussed.

Chapter 5 will contain the conclusions and recommendations with regard to the high-frequency Mosfet driver.

1.8 Summary

The background to the design and development of the high-frequency Mosfet driver has been given. The methodology has been reviewed as well as the delimitations of the project. Definitions of important terms were presented together with the importance of the research and overview of the entire report. The following chapter will consider frequency synthesis theory, circuitry and design.

Chapter 2 The high-frequency generation stage

2.1 Introduction

According to Blake (2002:6), the low-frequency band extends from 30 kHz to 300 kHz, the medium-frequency band from 300 kHz to 3 MHz and the high-frequency band from 3 MHz to 30 MHz. The high-frequency generation stage must produce a range of frequency from 50 kHz to 8 MHz, and thus incorporates all three of these bands. Chapter 2 will focus on various frequency synthesis techniques that have been employed to generate high frequencies. Various kinds of frequency synthesizers will be presented with attention primarily directed to the indirect frequency synthesizer and its components. The design process of the indirect frequency synthesizer incorporating the TTL based 74HC 4046 PLL, the CMOS based 4526 programmable divider and the CMOS based 4060 14-stage counter will then follow.

2.2 Frequency synthesizer techniques

A frequency synthesizer is a combination of system elements that results in the generation of one or many frequencies from one or a few reference sources. The frequency accuracy and stability of these devices are determined primarily by the accuracy and stability of the crystal and to a lesser extent by the circuit itself. The single crystal-controlled oscillator circuit was superseded by an approach currently referred to as incoherent synthesis. This method utilized a number of crystal-controlled oscillators combined in such a fashion as to generate many frequencies with relatively few crystals. The reference frequency is directly translated using analog techniques such as switching, frequency division, frequency multiplication, filtering and mixing. This approach was eventually improved by the use of just one reference source to produce numerous frequencies and came to be known as coherent synthesis (Manassewitsch 1987:1). Figure 2 represents a typical incoherent frequency synthesizer while figure 3 shows an example of a coherent direct frequency synthesizer.

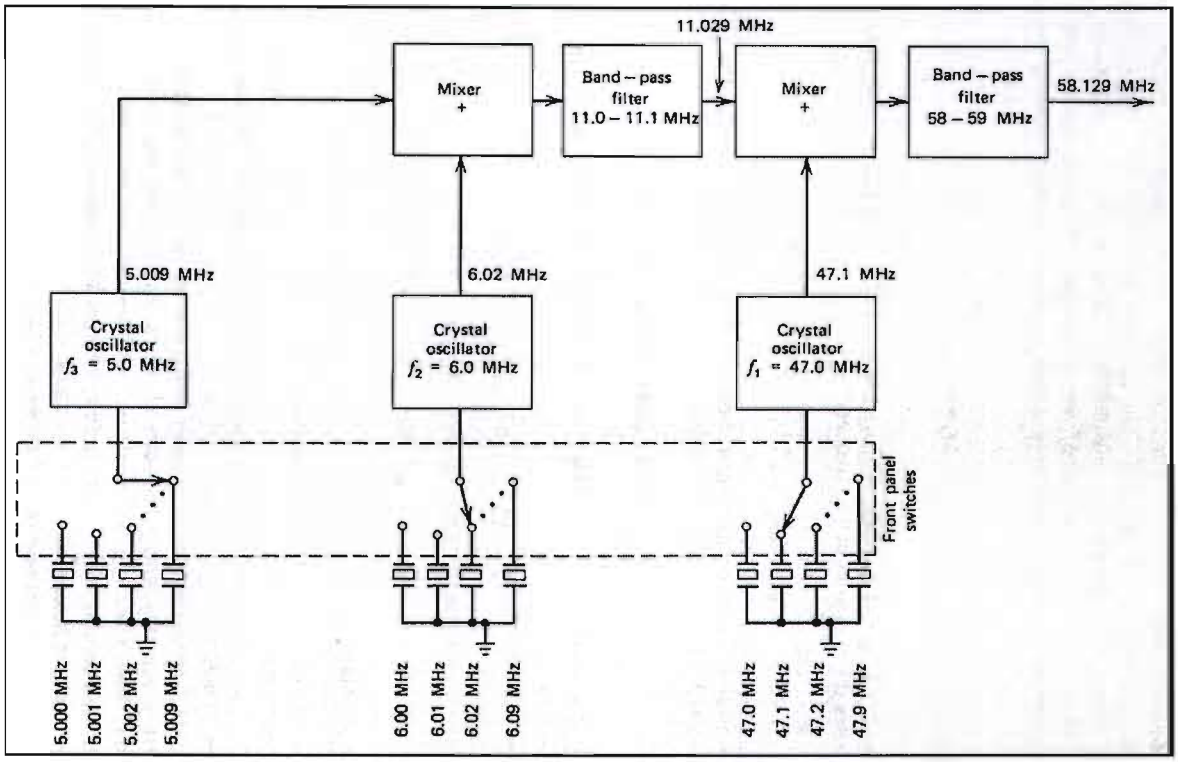

Figure 2 An example of an incoherent frequency synthesizer (Manassewitsch 1987:5).

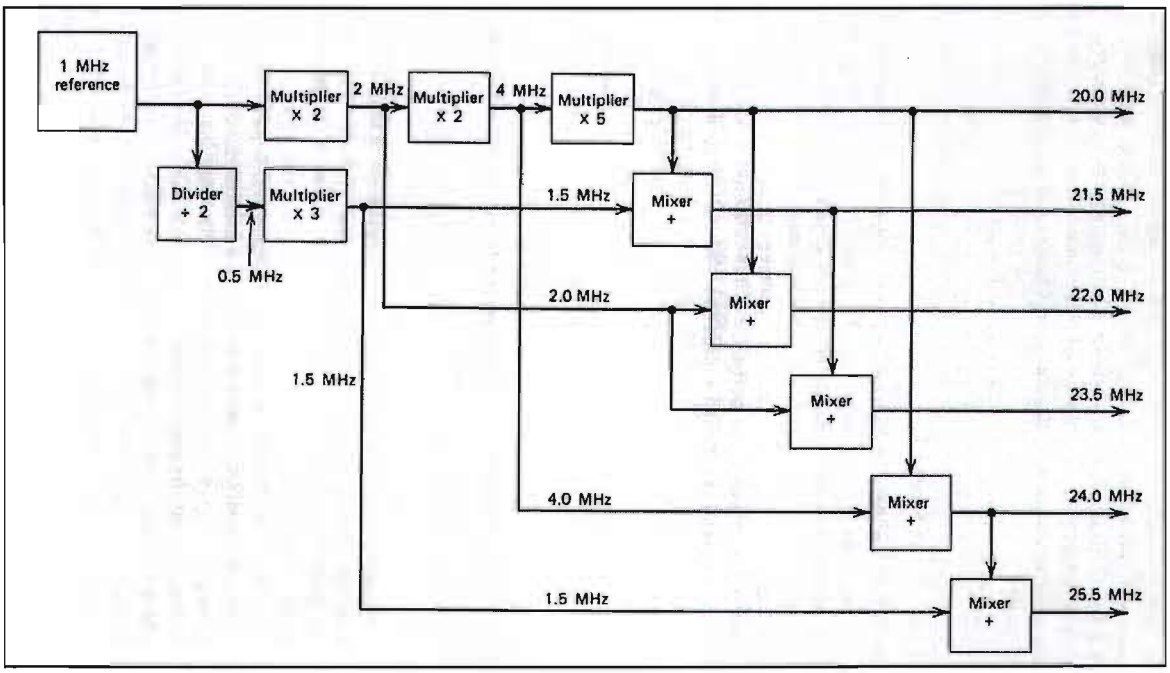

Figure 3 A coherent direct frequency synthesizer example (Manassewitsch 1987:8).

Frequency synthesis may thus be classified into two distinctive groups, namely coherent frequency synthesis and incoherent frequency synthesis. The coherent frequency synthesizers can furthermore be classified into coherent direct frequency synthesizers and coherent indirect frequency synthesizers.

Browne (2003:1) notes that the demand for synthesized sources with a wide range of performance levels is growing, as tuning in high-frequency systems is now dominated by digital approaches - tuning frequencies in discrete steps - rather than earlier analog methods, which utilized continuous tuning. Various techniques are currently utilized in modern frequency synthesizers, such as the "integer-N" synthesizer, the "fractional-N" synthesizer and the direct-digital synthesizer. These latter ones rely on the principle of conversion of 32-to-48-bit phase/frequency/amplitude digital data into analog output signals through use of precision accumulators and digital to analog converters. Direct digital synthesis (DDS) is an example of a coherent direct frequency synthesizer, where the output signal is created as a one-to-one function of an input digital word. This allows high-speed frequency switching and execution of such functions as frequency hopping and generation of complex chirp signals. Direct frequency synthesis may also be achieved via analog circuitry, where a comb of frequencies are generated and then filtered out to produce the required frequency components. The amount of filtering needed for high-frequency and broadband coverage leads to a design that is complex and expensive. The "integer-N" synthesizers use a multiplication factor, N, to determine the output frequency as a multiple of the reference source frequency. The "fractional-N" synthesizer is similar to an "integer-N" synthesizer but makes use of non-integer values for N. The "integer-N" synthesizer may be designed with a single loop for optimal frequency switching speed, or with multiple loops when lower noise performance is required. The "integer-N" synthesizer can achieve phase-noise levels that are close to the reference source, although they tend to be limited in bandwidth. This "integer-N" synthesizer forms part of the coherent indirect frequency synthesis group (Browne 2003:1). An example of an indirect frequency synthesizer is shown in figure 4. Table 1 contains a summary of the advantages and disadvantages of incoherent and coherent frequency synthesizers.

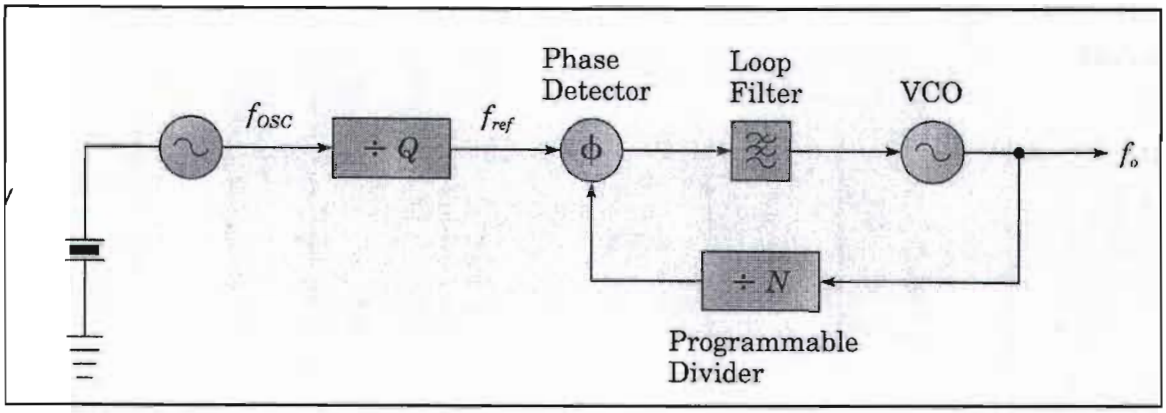

Figure 4 A coherent indirect frequency synthesizer (Blake 2002:86).

Table 1. Comparison of incoherent, coherent direct and coherent indirect frequency synthesizers.

	Advantage	**Disadvantage**
Incoherent frequency synthesizer	Very high output purity	Very high complexity Many components Many crystals
Coherent direct frequency synthesizer	Low spurious tone levels Low phase jitter One Crystal	Very high complexity Many components
Coherent indirect frequency synthesizer	Very easy to implement Easily integrated Few components One crystal	

The above table indicates that coherent indirect frequency synthesizers are much easier to design and implement. Having fewer components than their counterparts leads to a reduction in both cost and size. Finally, the wide availability of both PLL and divider circuits makes them the ideal choice for use in high-frequency generation, and will thus be utilized in this research project.

2.3 A theoretical overview of the indirect frequency synthesizer

Lythall (2002:1) presents the indirect frequency synthesizer as an arrangement whereby the reference frequency is multiplied by a programmable amount to achieve just about any frequency within a selected output frequency range. Best (1984:vii) describes the PLL circuit as an exotic device, found within specific electronic devices present in practically every home worldwide today. Indeed, the PLL is one of the most versatile sought after designs when it comes to stable frequency generation (Best 1997:1). Van Roon (2001:1) mentions a French scientist, H. de Bellescize, who in 1932 already published findings on PLL's called "La Réception Synchrone", published in Onde Electrique, volume 11. Van Roon (2001:1) further relates that the initial cost of the PLL circuit outweighed its counterparts and thus prohibited the widespread use of this technology. The PLL circuit did though become very popular when monolithic integrated circuits were developed, with complete PLL circuits being housed in these low-cost IC packages. From the 1940's on, the applications of the PLL circuit included synchronization of the horizontal and vertical sweep oscillators in television receivers to the transmitted sync pulses. AM and FM demodulators, frequency shift key (FSK) decoders, motor speed controls, touch-tone decoders, light-coupled analog isolators and frequency synthesized transmitters and receivers all make use of PLL circuitry today.

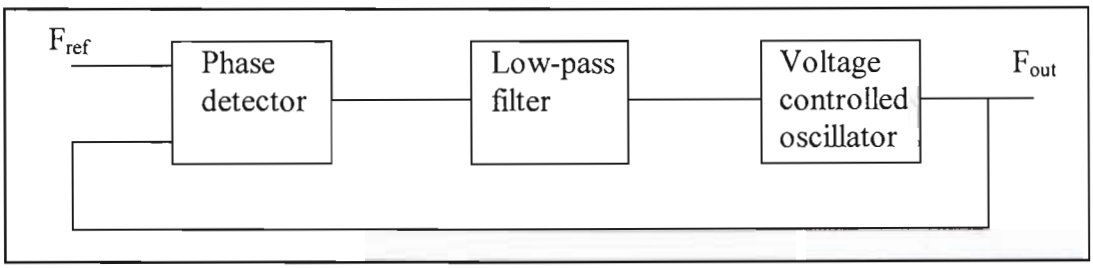

Figure 5 The block diagram of the common PLL circuit.

Best (1997:2) defines the PLL as a circuit synchronizing an output signal, generated by an oscillator, with a reference or input signal in frequency as well as in phase. Once synchronized or locked, the phase error state between the output and input frequency is virtually zero. He sketches the block diagram of the PLL circuit as containing three

distinct and separate sections, namely the phase detector (PD), low-pass filter (LF) and voltage controlled oscillator, hereafter called VCO. Berlin (1982:5-17) furthermore describes the PLL as a circuit incorporating an electronic feedback loop system consisting of a phase detector, low-pass filter and VCO. The block diagram of the PLL is sketched in figure 5.

Brennan (1996:26) describes the VCO as an electronically tuneable oscillator in which the output frequency is dependent on the value of an applied tuning voltage. VCO's are realised in many forms from RC multivibrators at low frequencies to varactor oscillators at higher frequencies. The most important property of a VCO is their tuning characteristic that is also referred to as the VCO's transfer function. This non-linear transfer function of input voltage to output frequency is shown in figure 6.

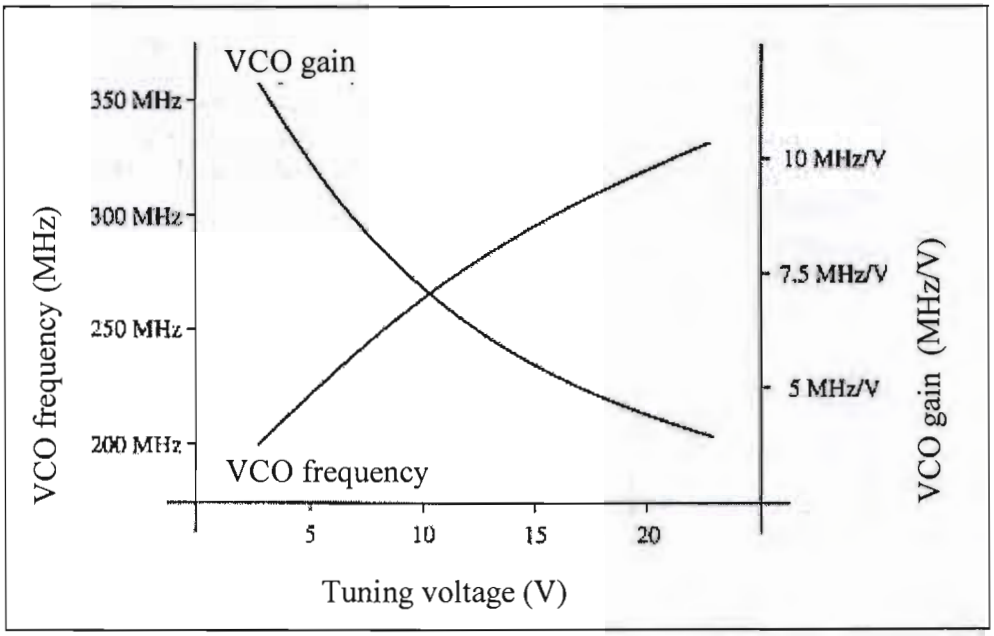

Figure 6 The transfer function of a VCO (Brennan 1996:27).

Best (1997:2) illustrates the transfer function of the phase detector as a function of the average value of the phase detector output signal to the phase error. This difference in phase value then generates a phase error as a DC voltage that is passed by the low-pass filter to the VCO. This DC voltage then serves to move the output frequency of the VCO either up or down, depending on its initial point of rest. The transfer function of the phase

detector is sketched in figure 7, where the optimum points of operation are between $+\pi$ and $-\pi$.

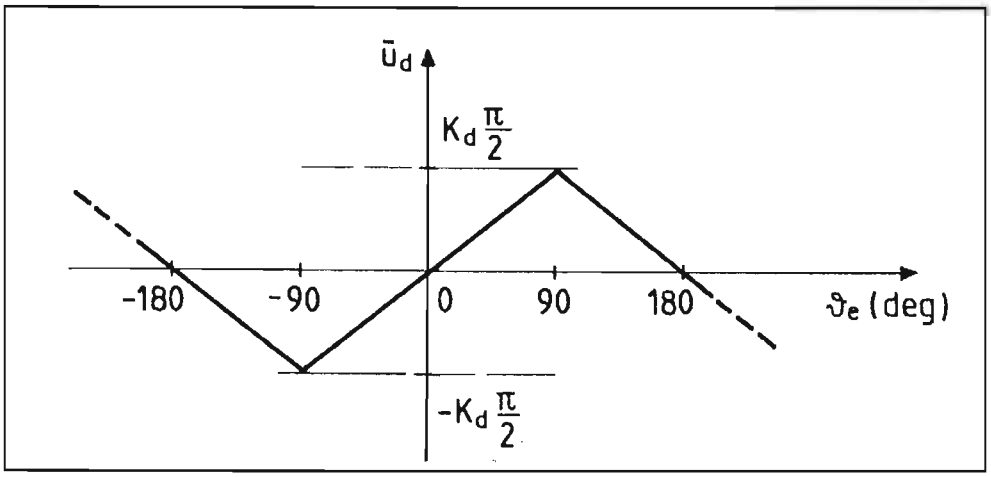

Figure 7 The phase detectors transfer function (Best 1997:95).

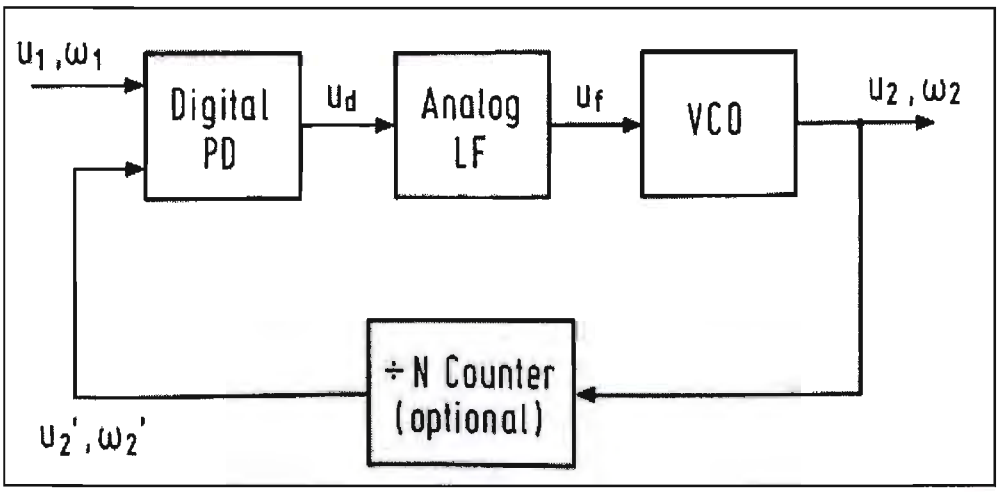

Figure 8 The block diagram of the digital phase-lock loop otherwise known as a frequency synthesizer (Best 1997:91).

From the 1970's on, the digital phase-lock loop, or DPLL, made its appearance. The DPLL included a divide-by-N counter in its configuration. The phase detector was constructed from EXOR gates or JK flip-flops, although the rest of the components were still analog. An improved phase detector later emerged that made use of 2 D-Type flip-flops connected to a NAND gate and comparator. This type of detector makes use of

positive edge triggering, being influenced only by the initial positive going edge of the incoming pulse signal. Best calls this improved phase detector a "Phase Frequency Detector", or PFD. He also accredits the PFD as the main workhouse of the DPLL circuit, incorporating no passive components. The classical DPLL block diagram is shown in figure 8, which is also termed the frequency synthesizer circuit (Best 1997:92). Voltage u_1 at frequency ω_1 is the reference frequency obtained from a stable reference source, such as a single quartz crystal. The VCO's output frequency is represented by u_2, ω_2 while u_2',ω_1' is the divided frequency obtained from the divide-by-N counter. The PLL circuit comprising the VCO and phase detector have become widely available in integrated circuit packages such as the CMOS-based 4046. The divide-by-N counter is also housed in a separate integrated package, or IC, external from the PLL section. The low-pass filter is the only section that features externally with passive components. The simplest loop filter configuration, being that of passive lag, is easily implemented with the 4046 (Best 1997:152). Figure 9 illustrates the bode diagram of a passive lag filter.

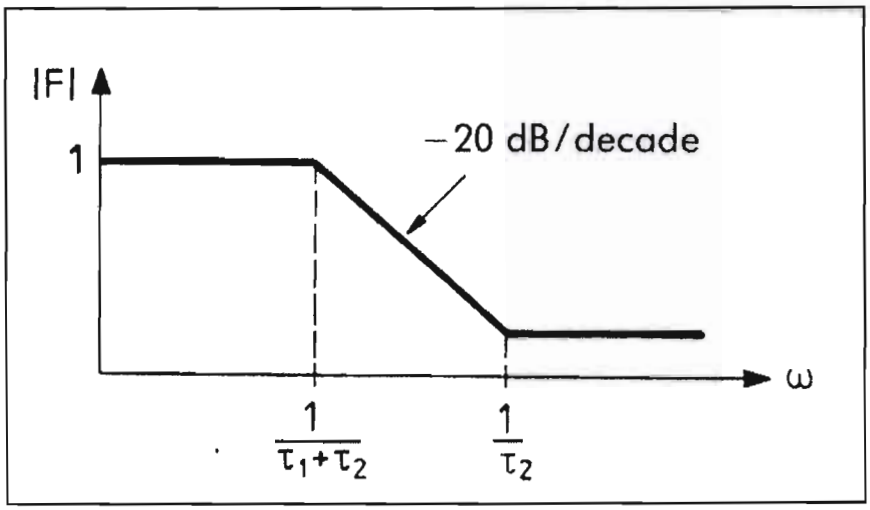

Figure 9 The bode diagram of a passive lag filter (Best 1997:9).

Best (1997:152) did a case study on frequency synthesizers, in which he considered the 74HC 4046. He noted the usefulness of the 74HC 4046 in generating high frequencies. This is verified in the datasheet specifications of the 74HC 4046 (Annexure A). The 74HC 4046 PLL circuit contains three different phase detectors, namely an EXOR gate, a PFD and a JK flip-flop. Table 2 provides a summary of the individual advantages and

disadvantages of the three phase detectors/comparators that are utilized in the 74HC 4046.

Table 2. Comparison of the three phase comparators used in the 74HC 4046.

	Phase comparator 1 EXOR flip flop	**Phase comparator 2 D-type flip flop**	**Phase comparator 3 JK flip flop**
Capture range dependant on the low-pass filter	Yes	No	Yes
Noise rejection at signal input	High	Low	Low
PLL locks onto harmonics of the VCO centre frequency	Yes	No	Yes
Phase difference between input and output locked signals	90°	0°	180°
Input signals duty cycle	Must be 50%	Not important	Not important

Best (1997:152) also plotted the VCO's characteristic as illustrated in figure 10. The linear operational range of the VCO was found to be between 1,1 and 3,9 V, when the output frequency changed from 1 to 2 MHz. The results obtained from the case study done by Best as well as the datasheet specifications highlights the following advantages of 74HC 4046:

- High-frequency generation up to 20 MHz.
- Constant 5 V peak output signal over the 20 MHz range.
- A choice of three different comparators or detectors.
- Linear input to output range of the VCO.

The 74HC 4046 will be used in this research project due to the advantages mentioned above. Phase comparator 2 will be chosen due to its advantages highlighted in table 2.

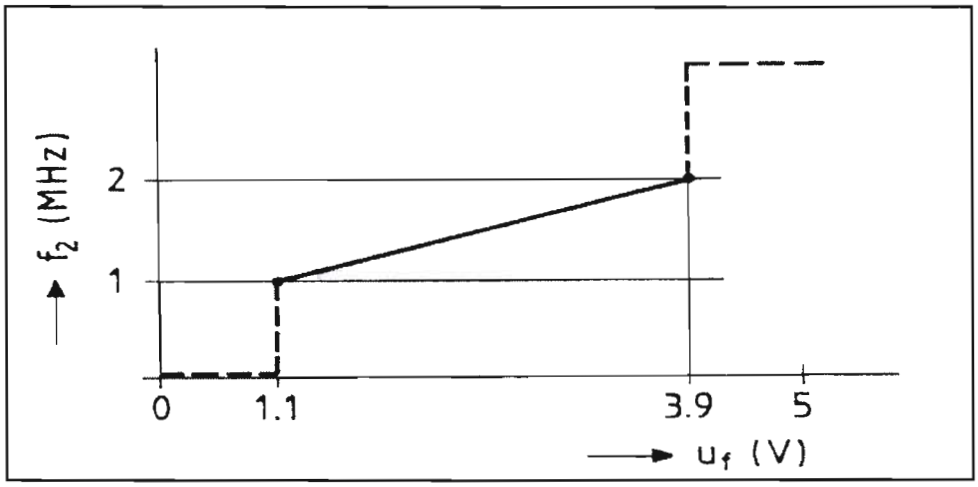

Figure 10 The 74HC 4046 VCO's characteristic (Best 1997:153).

The division of frequencies plays an important role in the function of any frequency synthesizer circuit. When a counter is used between the output of the VCO and the one input to the phase detector, the VCO then generates a frequency that is N times the reference frequency resulting in (Best 1997:92),

$$F_{out} = F_{ref} \times N \text{ Hz} \quad \ldots. (2.1)$$

Where F_{out} ≡ the VCO output frequency in Hz

F_{ref} ≡ the input reference frequency to the phase comparator in Hz

N ≡ the division factor

Berlin (1982:5-17) states that the divide-by-N counter is a logic circuit that produces a single output pulse for every N input pulses, where N is an integer. Often referred to as the modulus of the counter, the value of N can easily be changed to a different value and thus also affect the output value of the VCO. The CMOS-based 4526 is one of the best-known programmable cascaded down counters according to Marston (1996:196). A single counter has a maximum count of 16. The greatest advantage of the 4526 is the ease at which multiple counters may be cascaded together to obtain higher N counts. The reference frequency may then be made smaller resulting in the output frequency being adjustable in smaller frequency steps. The 4526 has the following advantages:

- High-frequency operation up to 10 MHz when fed with a 6 V power supply.
- Numerous counters may be cascaded together for higher divide-by-N counts.

The 4526 will be incorporated into this research project to function as the divide-by-N counter.

Lastly, a reference frequency must be obtained from a stable source. Berlin (1982:5-13) notes that the PLL synthesizer can only work correctly if based on a stable reference frequency. The frequency must be held constant over a period of time and under varying temperature conditions, otherwise the output VCO frequency will drift according to the input reference frequency, which is unacceptable. This is avoided by using a very stable oscillator, such as a quartz crystal oscillator that has the advantages of greater accuracy and stability (Blake 2003:72).

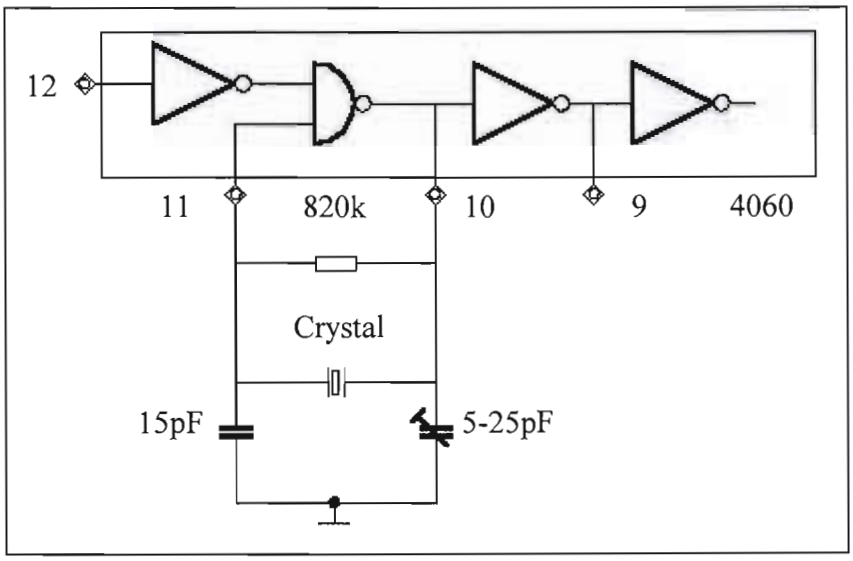

Figure 11 Crystal oscillator configuration on the 4060.

Marston (1996:267) explains that a crystal oscillator can be used to provide precision submultiples of the crystal frequency by feeding the crystal's output through a suitable number of digital divider stages, or a divide-by-Q counter. The CMOS-based 4060 is a 14-stage ripple carry binary counter, which can directly accept any crystal value up to 10 MHz. Figure 11 illustrates the capability of the 4060 to accept a quartz crystal in a Pierce oscillator configuration. Multiple cascaded stages within the 4060 offers the possibility of

dividing the crystal frequency by a factor of 2^n, where n represents the number of selected stages. The following two advantages of the 4060 can be noted:

- It directly accepts crystals up to a value of 10 MHz.
- It can divide the original input frequency by a factor of 2^n, and can thus function as a divide-by-Q counter.

The 4060 together with a quartz crystal will thus be included in this research project to function as the reference frequency section.

2.4 The indirect frequency synthesizer components

Today's technology has evolved at such a rate that many PLL circuits are available on the market in IC package form. One package of special interest is the TTL package, the 74HC 4046. The 74HC 4046 PLL functional diagram is shown in figure 12.

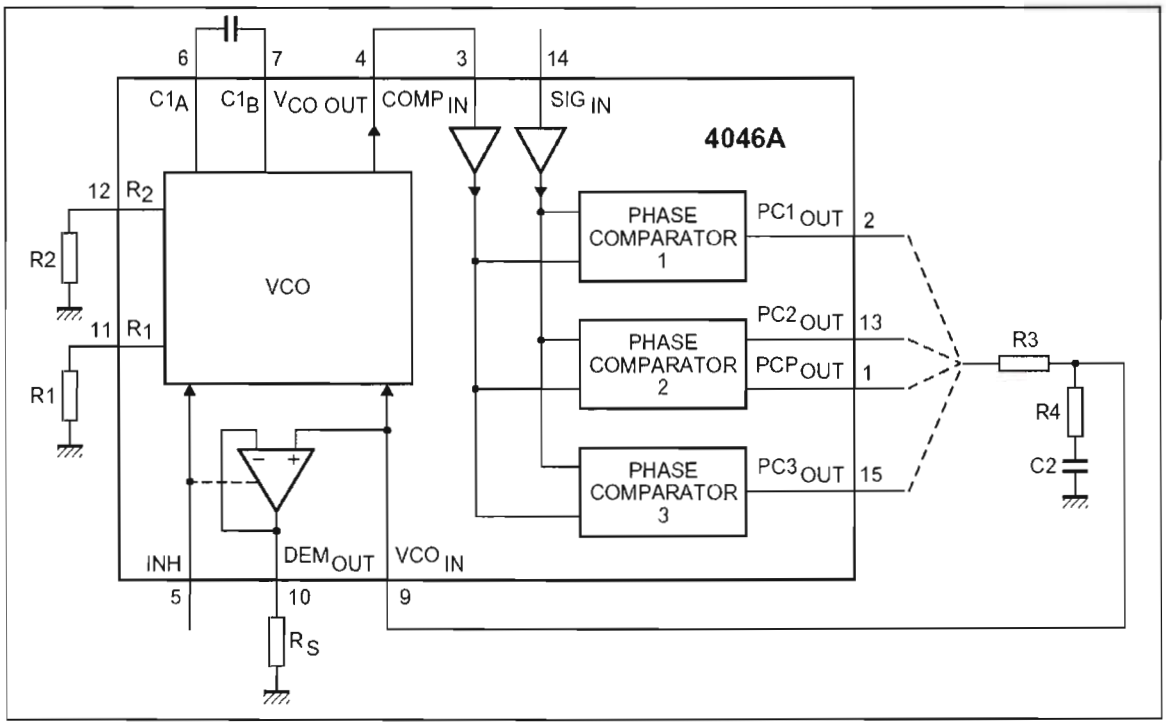

Figure 12 The 74HC 4046 functional diagram (Philips Semiconductors 2004).

The 74HC 4046 will be utilized as the PLL circuit in the frequency synthesizer to obtain the frequency range of 50 kHz to 8 MHz. The advantages of using the 74HC 4046 have

been presented in the theoretical overview. The 3 different phase comparators and VCO are housed inside the IC as shown in figure 12. The low-pass filter is the only external part, connected between the phase comparator's output and the VCO's input.

The divider circuit will be based upon the 4526, a programmable 4-bit down counter. Multiple connections of this device in series create higher division orders, with the highest input frequency being 10 MHz at a supply voltage of 6 V, according to the datasheet. The division factor can be set by means of 4-pole dipswitches. See annexure B. The functional diagram of the 4526 is shown in figure 13.

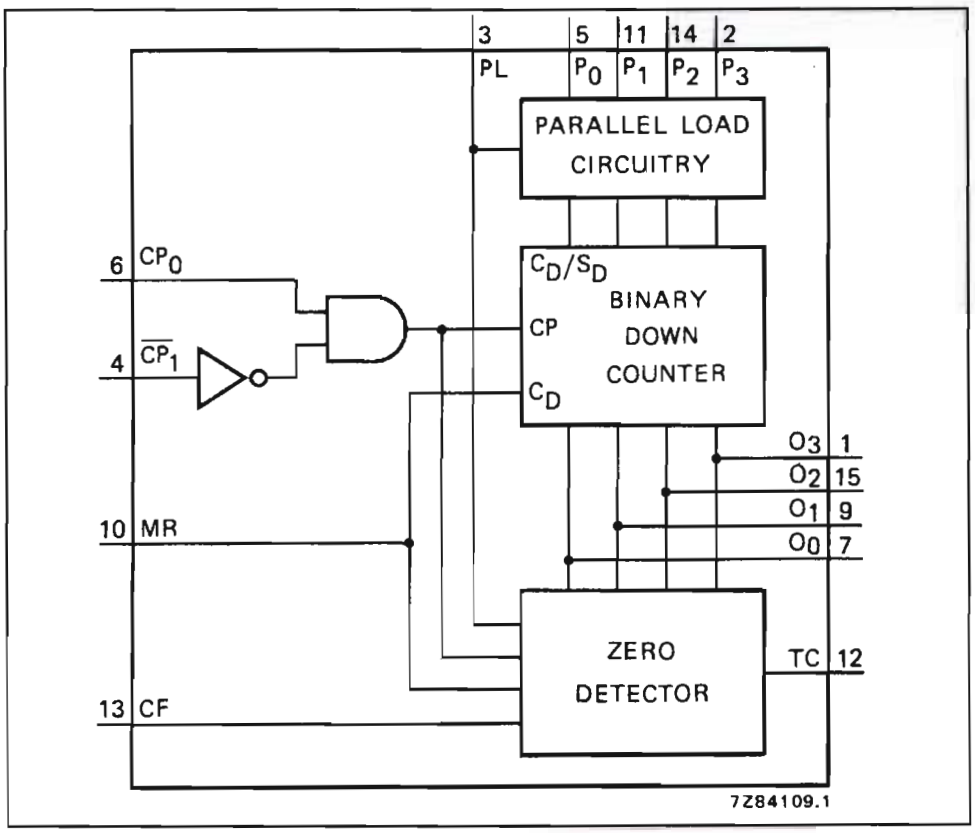

Figure 13 The 4526 functional diagram (Philips Semiconductors 2004).

The reference frequency that will be utilized in controlling the output frequency of the VCO must be very stable, so as to prevent the output VCO's frequency from drifting uncontrollably. A 4060 will be utilized in conjunction with a quartz crystal so as to obtain

a variety of reference frequencies. The functional diagram of the 4060 is illustrated in figure 14, where Q4 through Q14 represent the respective output divided frequencies.

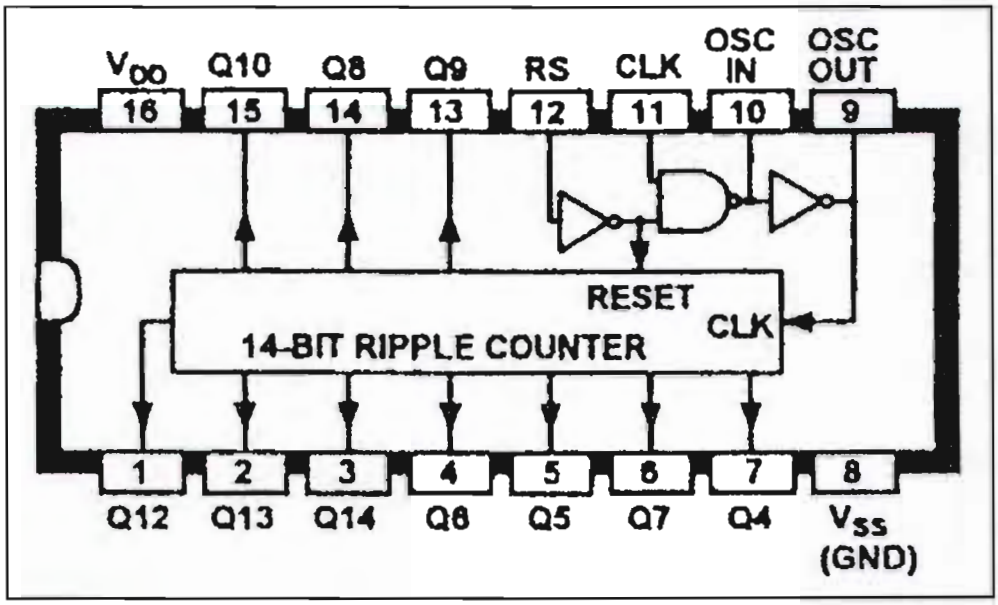

Figure 14 The functional diagram of the 4060 (Marston 1996:161).

2.5 The design process of the high-frequency generation stage

The first step is to implement the design criteria for the 74HC 4046 to achieve a free-running frequency with a desired lock range from 50 kHz to 8 MHz. Secondly, the inclusion of the 4526 as the frequency divider will be reviewed, as the output frequency must be changed in steps of 50 kHz. Finally, the generation of the 50 kHz reference frequency via the 4060 and quartz crystal will be considered.

The 74HC 4046's free-running frequency together with its capture and lock range are set via an external capacitor, C1, connected between pins 6 and 7, and by a resistor R1 connected between pin 11 and ground. Figure 18 shows the position of C1 and R1. For a free-running frequency of 2 MHz and a maximum lock frequency of 8 MHz, values for C1 and R1 can be selected by utilizing figure 15. The values for R1 would be 3 kΩ and for C1 around 300 pF. It was found that R1's value is correct around 3,3 kΩ, but C1 was not confirmed. Instead, a value of 33 pF was utilized that achieved the desired results.

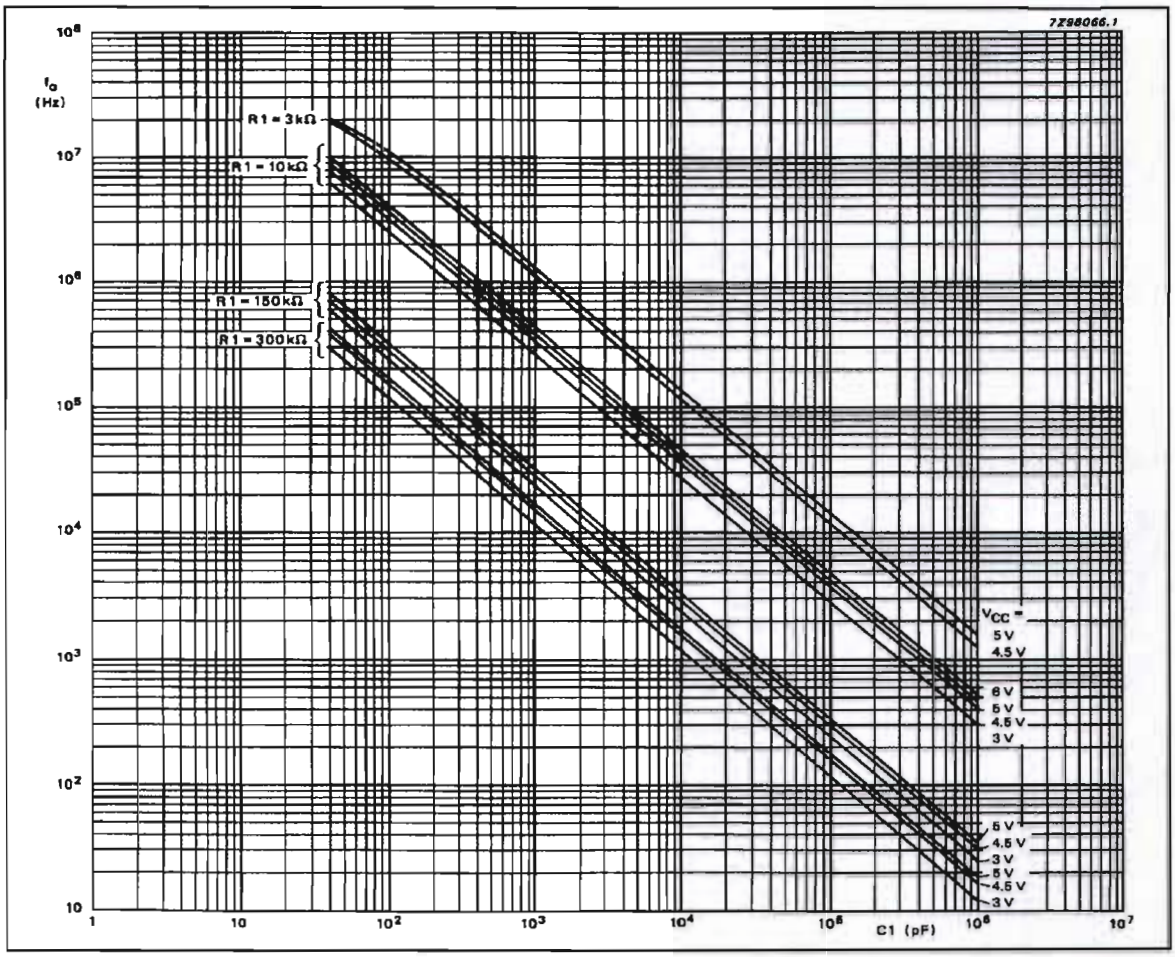

Figure 15 C1 and R1 from a predetermined VCO frequency (Philips Semiconductors 2004).

The inclusion of R2 creates a DC offset for the free-running frequency. This DC offset is handy when working at lower frequencies below 4 MHz, especially when utilizing the standard 4046 PLL. The introduction of R2 in the 4046 enables a higher stability and a decrease in the overshoot and ringing of the final VCO output frequency. Its application is though not warranted in the 74HC 4046, as it was found that it introduces instability and an oscillation at frequencies above 4 MHz. It will thus be ignored in this design and be considered as an infinitely high resistance to ground. The low-pass filter's values can be determined for a desired lock range of 7,950 MHz, a settling time of 1 ms and a supply voltage of 5,5 V at the maximum frequency point. The following equations for the calculation of the low-pass filter are taken from the datasheet in annexure A.

The VCO gain (K_v) is given by,

$$K_v = \frac{2 \times f_L \times 2 \times \pi}{0,9 - (\text{VCC} - 0,9)} \quad \ldots. (2.2)$$

Where f_L ≡ the lock range frequency in Hz

VCC ≡ the supply voltage V

Thus calculating the VCO gain of the 74HC 4046 results in,

$$K_v = \frac{2 \times 7950 \times 10^3 \times 2 \times \pi}{0,9 - (5,5 - 0,9)}$$

$$K_v = 26,8 \times 10^6 \text{ rads}^{-1}\text{V}^{-1}$$

Phase comparator gain (K_p) is calculated by,

$$K_p = \frac{\text{VCC}}{4 \times \pi} \quad \ldots. (2.3)$$

$$K_p = \frac{5,5}{4 \times \pi}$$

$$K_p = 0,437 \text{ Vrad}^{-1}$$

The transfer gain of the low-pass filter (K_f) is determined by,

$$K_f = \frac{1 + \tau_2}{1 + (\tau_1 + \tau_2)} \quad \ldots. (2.4)$$

Where τ_1 ≡ the time constant set by R3 and C2 (to give the roll off rate) in s

τ_2 ≡ the time constant set by R4 and C2 (to give the roll off rate) in s

Refer to figure 18 for the position of R3, R4 and C2.

The natural frequency (ω_n) is defined by,

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}} \text{ s}^{-1} \quad \text{.... (2.5)}$$

Where K_n is the inverse of the maximum or minimum divider ratio being,

$$N_{min} = \frac{F_{out(min)}}{F_{ref}} \quad \text{.... (2.6)}$$

$$N_{min} = \frac{50 \text{ kHz}}{50 \text{ kHz}}$$

$$N_{min} = 1$$

$$N_{max} = \frac{F_{out(max)}}{F_{ref}} \quad \text{.... (2.7)}$$

$$N_{max} = \frac{8 \text{ MHz}}{50 \text{ kHz}}$$

$$N_{max} = 160$$

A damping ratio (ξ) of 1 will cause an overshoot of less than 15% and will settle to within 2% at $\omega_n t$ = 5, according to the datasheet. See annexure A. The settling time (t) has already been given as 1 ms. Thus, ω_n is calculated as,

$$\omega_n = \frac{5}{t} \quad \text{.... (2.8)}$$

$$\omega_n = 5000 \text{ s}^{-1}$$

Now rewriting equation 2.5 results in,

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2} \quad \text{.... (2.9)}$$

The maximum overshoot will occur at the maximum natural frequency of equation 2.8, thus,

$$(\tau_1 + \tau_2) = \frac{0,437 \times 26,8 \times 10^6}{5000^2 \times 160}$$

$$(\tau_1 + \tau_2) = 2,928 \text{ ms}$$

Thus if C2 equals 100 nF then R4 equals,

$$\text{R4} = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \xi - 1}{K_p \times K_v \times K_n \times \text{C2}} \quad \ldots. (2.10)$$

Where $\xi \equiv$ the damping ratio

$$\text{R4} = \frac{[2,928 \times 10^{-3} \times 2 \times 5000 \times 1 - 1] \times 160}{0,437 \times 26,8 \times 10^6 \times 100 \times 10^{-9}}$$

$$\text{R4} = 3,8 \text{ k}\Omega$$

R3 is then calculated as follows,

$$\text{R3} = \frac{\tau_1}{\text{C2}} - \text{R4} \quad \ldots. (2.11)$$

$$\text{R3} = \frac{2,528 \times 10^{-3}}{100 \times 10^{-9}} - 3800$$

$$\text{R3} = 21,5 \text{ k}\Omega$$

$$\text{R3} = 22 \text{ k}\Omega$$

The low-pass filter, including component values, is sketched in figure 16. R3 is connected between the VCO's input and phase comparator 2's output. Lythall (2002:1), in his improved frequency synthesizer design, includes a 470 nF capacitor in parallel with R4. This serves to decrease the wide "skirt" found at the bottom of the fundamental frequency, thus improving the overall spectral purity. It also significantly improves the lock range and increases the stability of the output VCO frequency. The output frequency of the VCO tends to oscillate uncontrollably on the outskirts of the lock range. The improved low-pass filter design, depicted in figure 17, inhibits this uncontrolled

oscillation to a degree, thus ensuring an excellent lock range from 50 kHz to 8 MHz. The phase noise of the system is also significantly reduced.

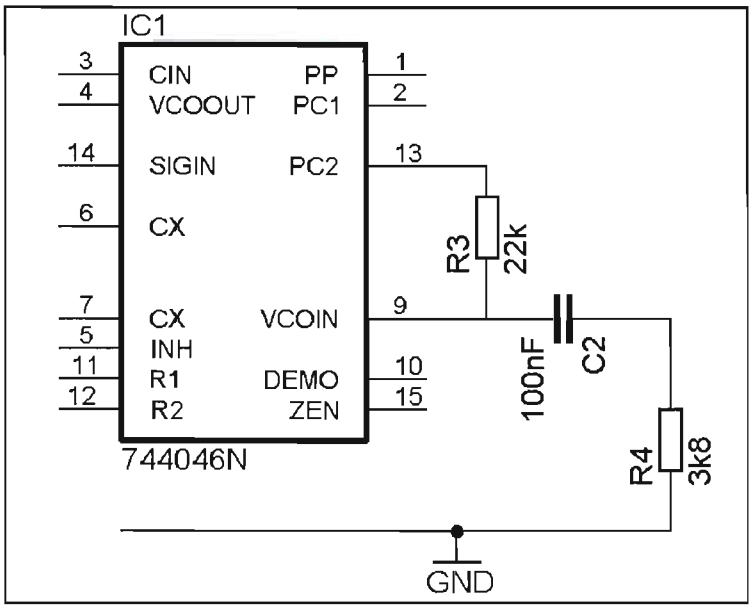

Figure 16 The low-pass filter network connected between pins 9,13 and ground.

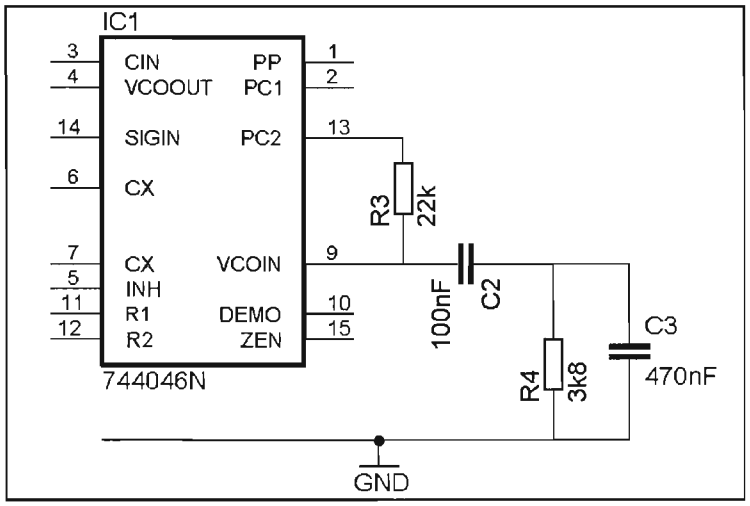

Figure 17 The improved low-pass filter incorporating the parallel capacitor across R4.

The PLL circuit incorporating all component values is illustrated in figure 18. The timing capacitor, C1, together with R1 are responsible for setting the free-running frequency of the PLL and has been chosen to be 33 pF. Capacitors C4 and C5 serve to DC de-couple

the VCO's input from the divider's output and the VCO's output from the divide-by-N input respectively. The input reference frequency to pin 14 on the PLL is also DC de-coupled via C6. R5 and R6 form a resistive network to ensure correct impedance matching between the reference frequency section and the PLL. The supply voltage is set to 5,5 V.

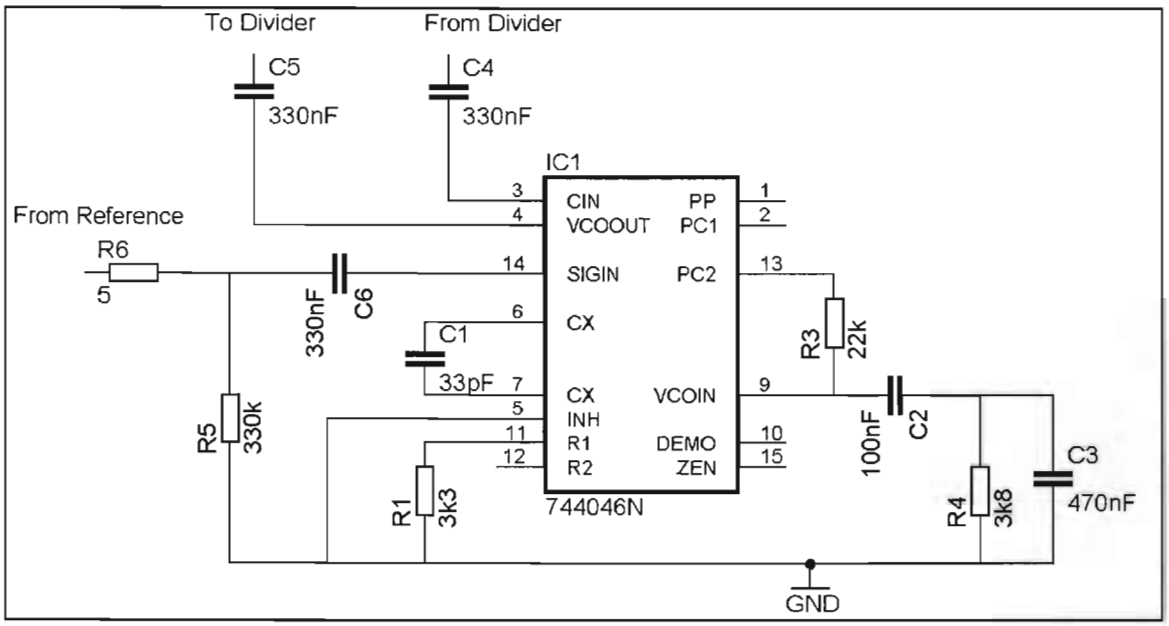

Figure 18 The complete circuit diagram of the TTL 74HC 4046 PLL.

The operating frequency range of the VCO is set between 50 kHz and 8 MHz. This must be adjustable in 50 kHz steps, which thus necessitates the use of a divider circuit. The minimum required division factor is 1, as calculated earlier in equation 2.6. The maximum value was found to be 160 from equation 2.7. To achieve a maximum division factor of 160 will require two counters to be cascaded, as one 4526 can only provide a maximum count of $2^4 = 16$. Using two 4526's results in a maximum division factor of $2^8 = 256$. The configuration of the two counters, the 4526's, is portrayed in figure 19. Connecting multiple 4526's together is made possible by means of CF (Carried forward function). Pins DP0 to DP3 serve as the input pins to set the division value to a predetermined amount. These pins should never be left floating, as this will cause the 4526 to operate incorrectly. They must either be connected to ground via a 1,8 kΩ

resistor to represent a "zero", or they must be connected to VCC to represent a "one". The master reset, MR or RES pin, needs to be grounded for the divider circuit to function correctly. All parallel load inputs, PL or PE inputs, must be connected together to ensure that the 4526 divider circuit operates in a cascade configuration. The clock input of successive counters is also connected to the maximum output pin of the forgoing counter. From the datasheet of the 4526 it is noted that the output frequencies from these circuits do not have a duty cycle of 50 %, but rather of around 10 % (Annexure B). Supplying the 4526 with a supply voltage of 5 V should result in successful frequency division upwards of 12 MHz according to the datasheet (Annexure B). This did not hold true in practice as the divider circuit only functioned correctly up to 2 MHz when fed with 5,5 V. A prescaler was thus included to divide the maximum frequency of 8 MHz by 4, so that it fell within the 2 MHz operating range of the 4526. It was only later discovered that increasing the supply voltage by 0,5 V to 6 V resulted in the 4526 correctly operating for an input frequency range of 0 - 12 MHz. The prescaler was thus discarded, leaving the twin pair of 4526's as the only necessary IC components of the divider section. The 74HC 4046 PLL's maximum supply voltage is 5,5 V (Annexure A). A series diode was however included in the supply rail of the 74HC 4046 to ensure that a maximum supply voltage of 5,5 V was never exceeded.

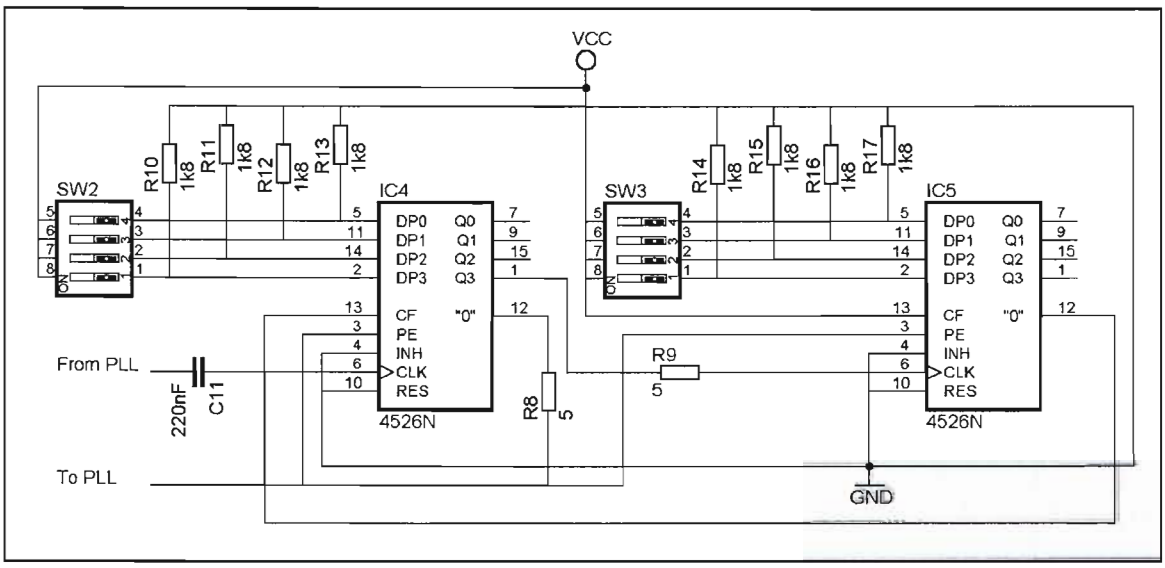

Figure 19 4526's connected in series to act as a maximum divide by 256.

The reference frequency must change the output frequency of the VCO in steps of 50 kHz. As already noted, a quartz crystal will satisfy the requirements for a stable reference source. Moreover, the ability of the 4060 to supply a variety of reference frequencies based upon a single quartz crystal frequency eliminates the impractical requirement of changing the crystal every time the reference frequency needs to be adjusted. The 4060 has the capability of directly accepting a quartz crystal across pins 10 and 11, with a few associated components. This configuration enables the crystal then to begin oscillating, as it is connected across a nand gate inverter. The initial quartz crystal frequency is thus accepted by the 4060, and then halved by the first divider stage. Every successive stage then divides its input frequency by 2 until a maximum division factor of 2^{14} is achieved. The first available output frequency occurs at pin 7, which is a division factor of 2^4, as 4 division stages are employed. A 6,4 MHz quartz crystal results in the first available output frequency of 400 kHz at pin 7. Then, by simply including a further 3 stages within the 4060, a 50 kHz reference frequency will be available at pin 6. Therefore, the following steps are necessary to set up the 4060 so as to provide a required reference frequency:

- Select a reference frequency.
- Multiply this reference frequency by 2^n, where n represents the number of stages in the 4060. This calculated frequency then becomes the value of the quartz crystal oscillator.
- If this quartz crystal is not commercially available, repeat the above step by either increasing or decreasing the power value, until a value for the quartz crystal is obtained that is freely available.

Selecting a reference frequency that is either double or half the initial reference frequency is now very easy to accomplish. The components surrounding the 4060 are shown in figure 20. The output frequency of the 4060 may be taken from any connection on J1, depending upon what value is required for the reference frequency. Using a 6,4 MHz crystal across pins 10 and 11 will result in a 50 kHz reference frequency being available at pin 6.

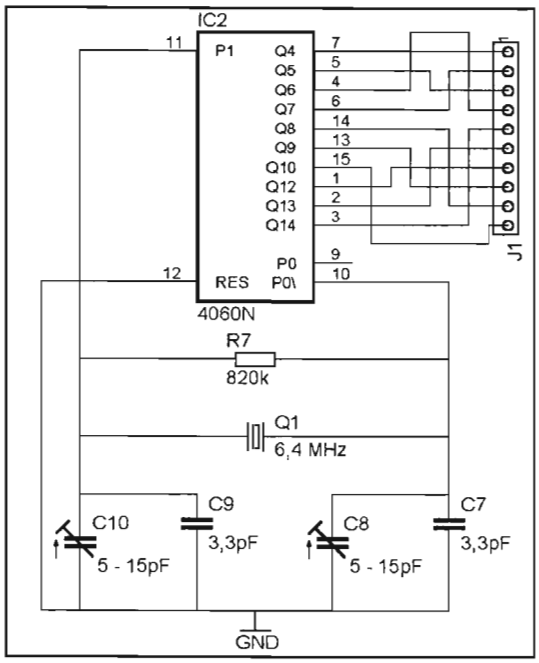

Figure 20 The reference frequency section built around the 4060.

2.6 Summary

The different kinds of frequency synthesizer circuits have been discussed as well as their individual advantages and disadvantages. Focus was directed at the indirect frequency synthesizer and in particular the 74HC 4046 PLL IC. Passive component selections were addressed to enable the 74HC 4046 to function correctly in the frequency range from 50 kHz to 8 MHz. These component selections also included the design of the low-pass filter that exists externally to the 74HC 4046, as well as the timing capacitor to set the free-running frequency. The maximum voltage supply to the 74HC 4046 is limited to 5,5 V and thus the maximum output voltage will be slightly less than 5,5 V.

The incorporation of the divide-by-N circuit, the 4526, was discussed. Cascading two of these counters will result in a maximum possible count of 256, although only 160 counts are required. The supply voltage to the divider section must be 6 V so as to ensure successful operation.

Finally, the generation of the reference frequency signal via the 4060 was considered. It was decided to make use of a 6,4 MHz crystal in conjunction with a 4060 for the generation of the stable reference frequency, being 50 kHz.

Chapter 3 will consider the design and implementation of the Mosfet driver stage. Attention will be given to the frequency limitation aspects of high-power Mosfets, as well as to the amplification of the output frequency of the 74HC 4046.

Chapter 3 The Mosfet driver stage

3.1 Introduction

The ability of high-power Mosfets to act as a switch makes it the ideal switching device according to Doyle (1976:3,4). This technique of switching between maximum and zero voltage across the high-power Mosfet is readily achieved at frequencies below 1 MHz. Raising the frequency to within the radio frequency range has often proved a problem since high-power Mosfets tend to have a frequency cut-out point. Chapter 3 will thus consider various techniques and methods currently employed to supply suitable charge to the gate of high-power Mosfets at high frequencies. The voltage amplification and gate drive sections will then be addressed. The minimum gate voltage required to successfully switch the Mosfet is around 10 V, according to Brown (1990:51). This chapter will thus also focus on voltage amplification techniques that will ensure an input gate voltage of around 12 V. This voltage amplification section is necessary as the output voltage from the frequency generation stage is limited to 5,5 V. The complementary emitter follower will eventually be considered to fulfil the role of the gate drive section.

3.2 Theoretical overview of Mosfet switching techniques

The advent of the power Mosfet ranks as one of the most significant developments in power electronics in recent years according to Grant and Gowar (1989: v). This statement is largely attributed to the numerous advantages that the power Mosfet holds over other semiconductor devices. Some noteworthy advantages are (Grant & Gowar 1989:17):

- Higher switching speeds.
- Their ability to maintain gain up to much higher frequencies.
- A very high input resistance.

A further significant advantage of the power Mosfet is its use as a switch in high-power applications. An ideal switch must either be completely closed or completely open. In the closed state the voltage across the Mosfet should ideally be zero, independent of the

current. In the open state the opposite must hold true, with zero current independent of the voltage (Doyle 1976:3,4). Although not an ideal switch, it is the device of choice when switching applications are considered (Grant & Gowar 1989:215). Figure 21 depicts the operation of the Mosfet as a switching device. Brown (1990:50,51) also notes the popularity of high-power Mosfets as fast power switches within the power electronics field. Mosfets are voltage driven devices, which in turn means that much less average current is needed to successfully drive the gate of high-power Mosfets.

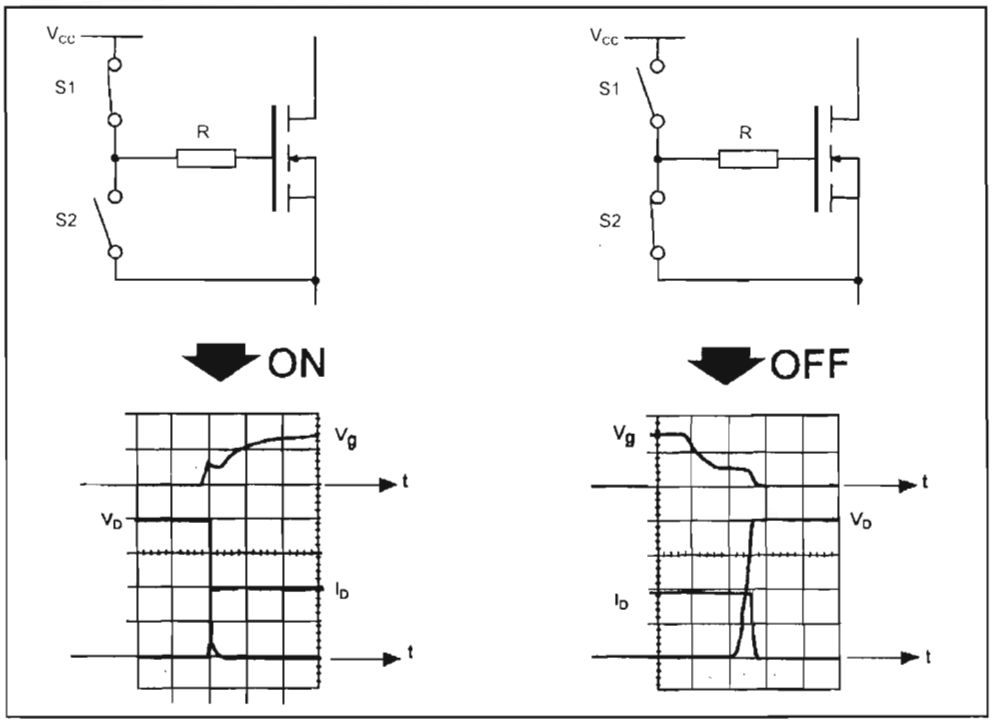

Figure 21 Driving the Mosfet/IGBT gates (Maurice and Wuidart 1994).

The switching of the Mosfet occurs through a voltage applied to the gate of the semiconductor device. Rapid voltage transients applied to the gate contact have to charge and discharge the gate capacitance. The charging and discharging currents have to flow through the significant sheet resistance of the polycrystalline silicon layer. They are thus subject to propagation delays and degradation as they travel to the more remote regions of the gate. This means that some care has to be taken over the layout of the gate connections, in order to ensure that no part of the gate is more than some minimum distance from the nearest connection. The gate charge needed to turn the Mosfet on and

off is insensitive to the current being switched and to the precise waveforms. A layout of the gate connections that minimizes the polysilicon path lengths is crucial if the Mosfet is to be activated in high-frequency operations. For efficient operation above 50 MHz, the gate connections must be less than 1 mm apart (Grant & Gowar 1989:139-143).

The speed limitations of MOS circuits are due entirely to stray circuit capacitance and the inability of the Mosfet to charge and discharge this capacitance (Crawford 1967:3-10). Balogh (2001:4) also makes the statement that the practical switching times of Mosfets are at least two to three orders of magnitude longer than the theoretical switching time. In high-speed applications then, the most important parameters are the parasitic capacitances of the Mosfet device (Balogh 2001:4). Intrinsic cut-off frequencies of MOS devices themselves are in the order of 1 GHz. It could thus be said that Mosfets are not really inherently bound to frequency limitations within the high-frequency range, because of the absence of minority carrier transport. Two limits to high-frequency operation are set by (Baliga 1987:300):

- The transient time across the drift region.
- The rate of charging of the input gate capacitance.

The transit time limited frequency response (f_T) is a function of breakdown voltage (Baliga 1987:300),

$$f_T = \frac{6{,}11\times10^{11}}{(1+\frac{L}{d})\times(BV_{PP})^{\frac{7}{6}}}\ \text{Hz} \qquad \ldots. (3.1)$$

Where $L \equiv$ Mosfet channel length in μm

$d \equiv$ Mosfet drift region thickness in μm

$BV_{PP} \equiv$ Mosfet breakdown voltage in V

Taylor (1993:3) examines the gate control charge of a Mosfet when switched on. The gate control charge (Q_{gate}) may be expressed as (Taylor 1993:3),

$$Q_{gate} = C_{iss} \times V_{gs} \text{ C} \quad \text{.... (3.2)}$$

Where C_{iss} ≡ the input gate capacitance of the Mosfet in pF

V_{gs} ≡ the gate to source voltage V

C_{iss} is the sum of the real capacitance between the gate and source, C_{GS}, and the voltage dependant capacitance between the drain and the gate called C_{DG}. The value of V_{gs} is a function of the device and the voltage required to achieve full enhancement. The energy expended in accumulating this gate charge (E_{gate}) can best be expressed as (Taylor 1993:3),

$$E_{gate} = 0,5 \times C_{iss} \times V_{gs}^{\ 2} \text{ J} \quad \text{.... (3.3)}$$

To show the overall drive efficiency then, the power consumed in the gate (P_{gate}) must be considered via the equation (Taylor 1993:4),

$$P_{gate} = 0,5 \times C_{iss} \times V_{gs}^{\ 2} \times f \text{ W} \quad \text{.... (3.4)}$$

Where f ≡ the input gate frequency in Hz

This power in the gate will only be dissipated within the gate structure if the gate structure's resistance happens to be significantly higher than the drive circuit impedance. The amount of power that will be dissipated in the gate of an IRF 140 (see annexure C for the datasheet specifications of the IRF 140) when the gate to source voltage is 10 V and the frequency of operation is 1 kHz is,

$$P_{gate} = 0,5 \times C_{iss} \times V_{gs}^{\ 2} \times f$$

$$P_{gate} = 0,5 \times 1660 \times 10^{-12} \times 10^{2} \times 1000$$

$$P_{gate} = 83 \ \mu\text{W}$$

Therefore, driving high-power Mosfets at low frequencies requires only a small amount of power, and thus a small amount of gate current. The gate charge may also be expressed as an equation with regard to current and time (Taylor 1993:24),

$$Q_{gate} = I \times t_1 \text{ C} \qquad \ldots. (3.5)$$

Where $I \equiv$ the input gate current in A

$t_1 \equiv$ the positive time period of the frequency in s

The ramifications of this simplified equation are extremely profound. If the circuit designer knows the gate charge which is required by the power device and can design the circuit in such a way as to utilize and exploit these charging characteristics, by judicious control of the current flowing into or out of the gate terminal, it will then follow that time being the ratio of the charge to the current, the switching times can be accurately predicted (Taylor 1993:24). The variation of the gate voltage with gate charge time when considering the drain-source voltage is shown in figure 22. Applying a positive gate voltage greater than the threshold voltage (V_T) gives rise to a conducting channel between the source and the drain. I_0 represents the current that will flow through the drain for certain load impedances and g_{fs} is the transconductance that determines the current-carrying capacity of the device (Grant & Gowar 1989:36, 68, 102)

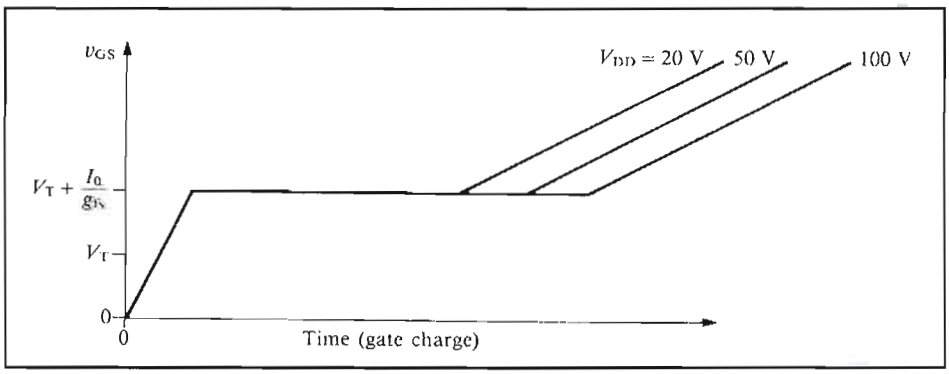

Figure 22 Gate voltage to gate charge time with varying drain-source voltages (Grant & Gowar 1989:138).

A portion of the gate drive power will be dissipated in the internal resistance of the gate. At frequencies around 100 kHz these losses are negligible, but at higher frequencies they become significant, especially when considering frequencies in the 10 MHz range. The internal gate losses ($P_{g(int)}$) are given by (Grant & Gowar 1989:165),

$$P_{g(\text{int})} = V_{gs} \times Q_{gate} \times f \times \frac{R_{G(\text{int})}}{R_s + R_{G(\text{int})}} \text{ W} \qquad \ldots. (3.6)$$

Where $R_{G(int)}$ ≡ the internal resistance of the Mosfet gate in Ω

R_s ≡ the external resistance to the Mosfet gate in Ω

To switch the Mosfet from the non-conducting to the conducting state, the gate-source voltage must be raised from below to above the threshold voltage by a transfer of charge into the gate. Turn-off is achieved by reversing the process. The manner in which the transition takes place determines the switching performance of the device. A gate drive circuit may generally be represented by a voltage source in series with a resistance. A resistance may be inserted intentionally between the gate of the Mosfet and the voltage source so as to modify the switching speed or represent the impedance of the voltage source (Grant & Gowar 1989:191). Different turn-on and turn-off times may be achieved by utilizing a diode in parallel with this series resistance as shown in figure 23 and figure 24.

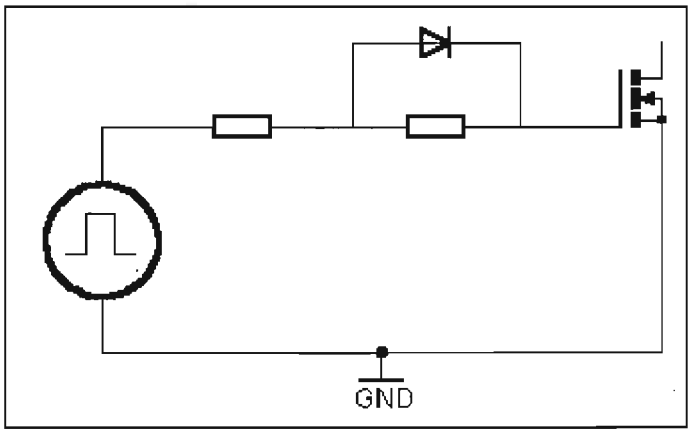

Figure 23 Asymmetric gate drives featuring a fast turn-on technique.

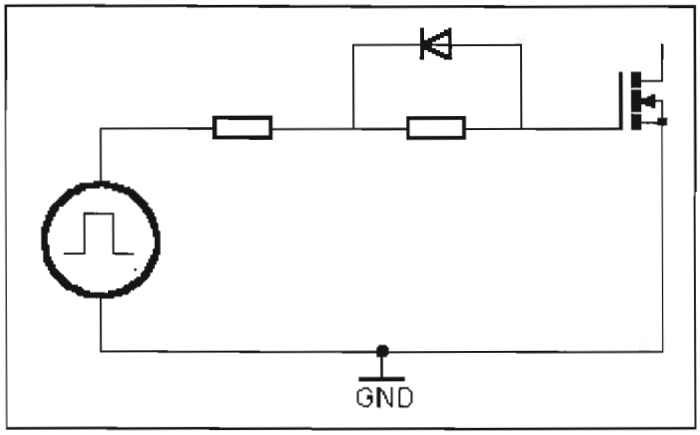

Figure 24 Asymmetric gate drives featuring a slow turn-on technique.

However, asymmetry may be inherent in gate drive circuits, for example when a gate driver has an active pull down action but a passive pull up action or visa versa. Figure 25 illustrates gate drive circuits with inherent asymmetry.

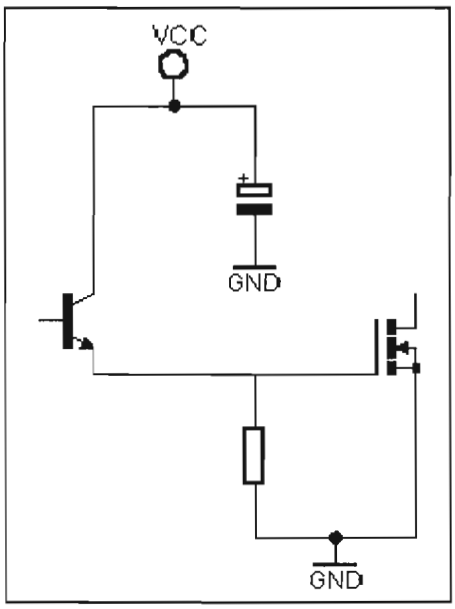

Figure 25 Gate drive circuits with inherent asymmetry.

To archive switching speeds of the order of 100 ns or less requires a gate drive circuit with a low output impedance and the ability to source and sink relatively large currents. For example, an IRF 140 will require a gate control charge of 16 nC to raise the gate voltage from 0 to 10 V. This is calculated for an input gate capacitance of 1600 pF and a

gate voltage of 10 V when used in equation 3.2 (see annexure C for the IRF 140 datasheet specifications). If the turn-on is completed within 50 ns, then the average gate current is 320 mA from equation 3.5. A NPN and PNP transistor connected in a totem-pole configuration as shown in figure 26, is capable of sourcing and sinking this amount of current. It provides low output impedance, which is required by the gate of the Mosfet, regardless of the direction of the load current (Grant & Gowar 1989:195-196).

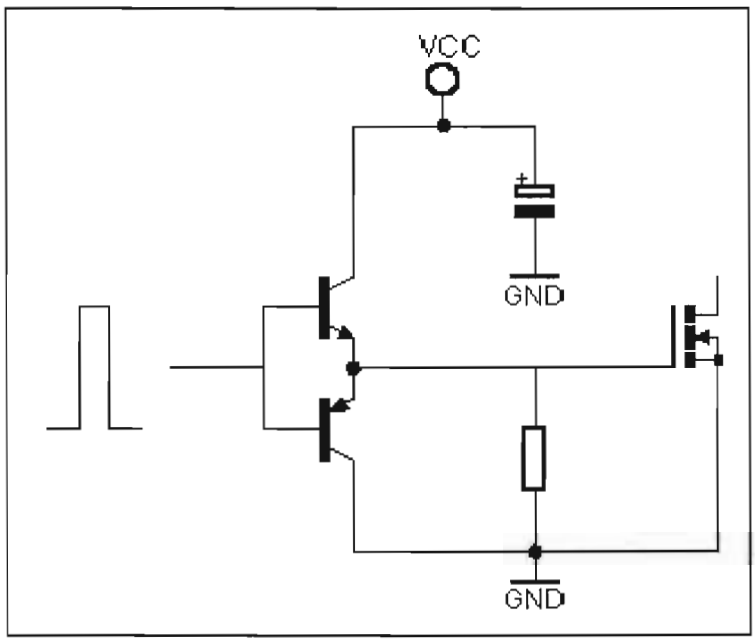

Figure 26 Complementary emitter follower, low impedance gate drive circuit.

According to Brown (1990:51), the attainment of a saturated drain to source voltage requires a gate voltage of at least 10 V. However, switching the Mosfet quickly on and off may require an ampere or more of peak current. This means that the driver should be a low-impedance active pull-up/pull-down type driver, such as the totem-pole driver comprising a complementary emitter follower. This totem-pole driver should have a solid, well-bypassed voltage supply in order to sink and source relatively high peak currents. Attaining switching speeds around 30 to 50 ns should not be too difficult with this type of driver (Brown 1990:52). However, Grant and Gowar (1989:194) warn about raising the gate voltage too high and thus make a recommendation to keep the gate voltage to a maximum of 15 V, so as to maintain the reliability of the power Mosfet.

High-power Mosfets may also be directly driven from CMOS IC's. The output characteristics of CMOS are approximately the same whether sourcing or sinking current. The main advantage is that the supply voltage may be set at 15 V, which is just what is needed to switch the power Mosfets on and off. Lower output impedance can be achieved by connecting a number of CMOS gates in parallel as shown in figure 27. Higher switching times can also be achieved by the incorporation of a buffer made up of a complementary emitter follower (Grant & Gowar 1989:203-204).

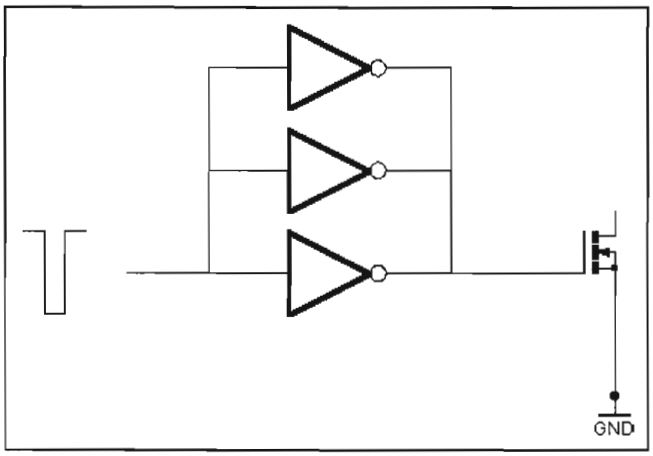

Figure 27 CMOS output paralled to increase drive capability.

Switching a high-power Mosfet may also be achieved by using a photovoltaic isolator as shown in figure 28. Output voltage may be 10 V while the output current will be around 50 µA maximum. It follows then that the switching frequency will be limited to around 2 kHz or less (Taylor 1993:34).

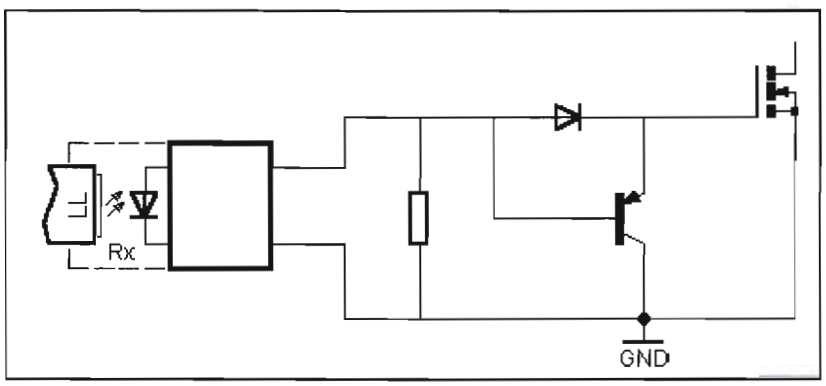

Figure 28 A photovoltaic isolator used as a simple gate drive circuit.

If it is desirable to include some type of protection, Taylor (1993:35) suggests using one of the many Micropower or CMOS linear integrated circuits. The only additional required component will be a moderately low impedance turn-off circuit, to prevent accidental turn-on by applied dv/dt. In the circuit layout of Mosfet gate drives, it is good to keep the following three points in mind (Taylor 1993:60):

- Maintain all conductor lengths as short as is physically possible in order to reduce the levels of stray capacitance.
- Currents in all conductors should be maintained as continuous, if possible, with a small ripple component.
- Gate circuit return leads should connect directly to the source terminal of the Mosfet package in order to eliminate the effects of feed-back from the source inductor.

3.3 The voltage amplification and gate drive sections

Amplification of high-frequency signals has always posed a challenge to researchers the world over. Common methods include among others Class A and Class C amplifiers. These circuits are not ideal as they operate over a relatively narrow bandwidth. The bandwidth required in this case is 7,950 MHz, being from 50 kHz up to 8 MHz. The ideal waveform required in the successful gate drive of high-power Mosfets is a square waveform, switching the Mosfet either on or off. A circuit that would thus operate successfully across this 8 MHz bandwidth and provide a very close replica of a square waveform is the CMOS based 40106, a HEX inverting Schmitt trigger containing 6 separate invertors. The logic diagram of one of the 6 invertors contained in the 40106 package is shown in figure 29.

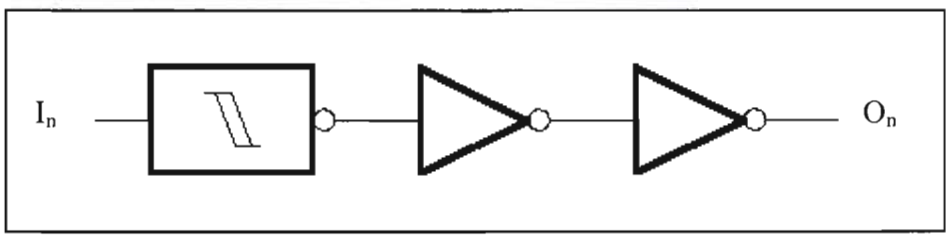

Figure 29 Logic diagram of a single inverter within the 40106.

From the datasheet specifications (Annexure D), it can be seen that the 40106 output transition time from low to high is typically around 60 ns when fed from a 5 V source. High to low transition time is typically also 60 ns. As the supply voltage increases, these transition times decrease, thus increasing the maximum allowable clock frequency that can be handled by the 40106. A 5 V supply will cause the 40106 to successfully accommodate a frequency of around 8 MHz that is a 120 ns time period, which then accords to the sum of the low-to-high and high-to-low transition times of 60 ns each. The Schmitt trigger action is mainly responsible for this transition time as well as for relatively high input noise immunity. The 40106 will also thus provide a close replica of the required square waveform as it switches between VCC and ground continually. The output peak-to-peak voltage is thus a function of the supply voltage to the chip, which can be anything between 5 and 15 V.

A buffer circuit comprising a complementary pair of NPN and PNP transistors has been presented in chapter 2 as an ideal circuit to connect Mosfet gates to frequency generation circuits. Due to their very low output impedance and excellent current sourcing, they provide the necessary switching conditions for the gate of high-power Mosfets.

3.4 The design process of the Mosfet driver stage

Connecting multiple 40106 circuits together in series, each operating at different supply voltages, will result in voltage amplification from 5,5 V to 12 V. This will then be incorporated into the design to provide the necessary 12 V peak-to-peak voltage signal needed to successfully drive the gate of a high-power Mosfet. Signal conditioning between the 40106 voltage amplification section and the gate of the Mosfet will take place via the use of a complementary emitter follower. Both a simulated and experimental model will be employed in the design process of the gate drive section.

From the datasheet specifications of the 40106 (Annexure D), the hysteresis voltage is found to be 0,5 V for a voltage supply of 5 V. The minimum input voltage level required

to switch the output of the 40106 low is typically 2 V. To switch the output high will thus require an input voltage of 0,5 V less than the 2 V, which equates to 1,5 V. Figure 30 shows the input switching waveform required by the 40106, where V_p represents the positive going input threshold voltage, V_N the negative going input threshold voltage and V_H the hysteresis voltage. The output from the frequency synthesizer is 5,5 V, which should mean theoretically that only one 40106 supplied with 15 V would be necessary as the minimum input switching levels, according to the datasheet specification, are set at 4 and 4,9 V. However, this was not found to be the case. The typical values have to be considered, especially when operating at 8 MHz. Thus a typical value of 4,5 V is necessary to switch the output high, and a value of 5,8 V to switch the output low when operating at a 10 V supply. This is just out of reach from the frequency synthesizers 5,5 V maximum voltage. So by making the supply voltage to the first 40106 8 V, it is possible to switch successfully between ground and VCC when supplied with an input voltage of either ground or 5,5 V.

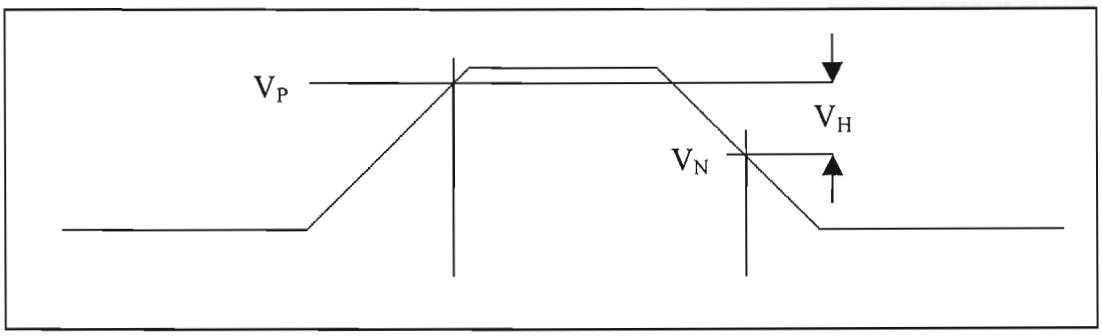

Figure 30 Switching input characteristics of the 40106.

Using just one inverter on the 40106 does not provide sufficient drive to the following inverter in the circuit. It was found that by paralleling 3 inverters on the chip resulted in a lower output impedance, thus providing sufficient energy for the next set of inverters, exactly as foretold by Grant and Gowar (1989:204). The supply voltage cannot yet be set to 15 V, as the required switching input voltages are 6,5 V and 8,3 V, and the maximum output from the first set of inverters is not quite VCC, but rather 7,425 V. Thus a second set of inverters on a second 40106 is fed from a 9 V supply and this improves the output switching voltage range between Ground and 9,015 V. This range between ground and 9

V was found though to be insufficient to drive the next stage of inverters when placed at a 15 V supply. A 11,4 V supply was thus utilized, which accepted the 9 V maximum input voltage signal and increased it to 11,43 V. This signal level of 11,4 V could now be passed to the fourth and final set of inverters operating at 12 V. The 3 inverters on each 40106 thus provide voltage amplification to the next set of inverters. Four identical inverter sets were thus used to increase the frequency synthesizer's voltage from 5,5 V to 7,425 V, then to 9,015 V, then to 11,43 V and then finally to 12,04 V. Figure 31 illustrates the four identical inverter sets on individual HEX inverter Schmitt triggers which serve as the voltage amplification section.

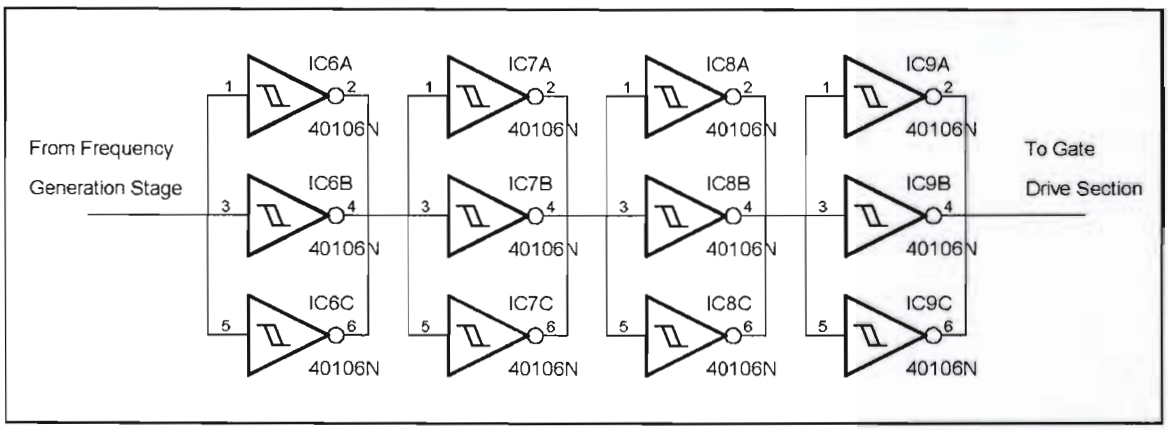

Figure 31 Four 40106's connected in series which provide the voltage amplification of a square wave.

The output from the final 40106 is passed to a complementary emitter follower via a small value resistor and DC de-coupling capacitor. The main reason for this complementary emitter follower is to accommodate the high-frequency signal between the voltage amplification section and the Mosfets gate. The 40106 will not be able to supply sufficient drive to the gate of the Mosfet to switch it either completely on or off. By utilizing the complementary emitter follower, the gate of the Mosfet is shorted either to VCC or to ground, which are the two ideal switching conditions for successful high-power Mosfet operations. The supply voltage to the complementary emitter follower is set at 15 V. Two complementary emitter followers are utilized. One incorporates small signal transistors capable of sourcing 0,5 A, and the other one uses large signal transistors

capable of sourcing 1,5 A. The aim of this design was firstly to provide further isolation between the Mosfet gate and the voltage amplification section and secondly to ensure that the peak currents through the gate of the Mosfet does not destroy the small signal transistors that are incapable of sourcing these high currents. Figure 32 shows the two complementary emitter followers connected in series. The inclusion of the series inductor is to damp oscillations that occur in the output of the Mosfet as it passes through the linear regions. It must also be remembered to couple suitable bypass capacitors onto the supply rails of both complementary emitter followers. These bypass capacitors must be situated as close as possible to the individual buffers, so as to source and sink relatively high peaks of current that will pass through the complementary emitter section. Allowing the gate of the high-power Mosfet to float when the device is connected across the supply rails proves detrimental. It is for this reason that R18 is included in the circuit design.

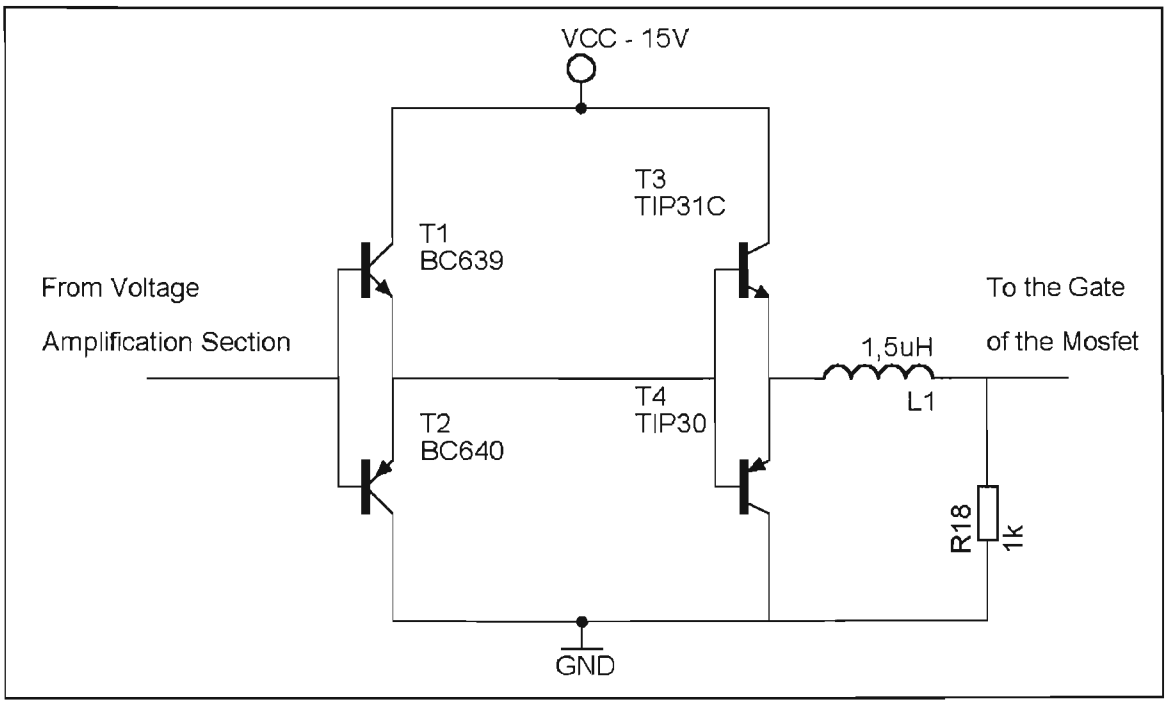

Figure 32 The complementary emitter followers connected in series.

The complementary emitter follower was also simulated via the SIMETRIX simulation software package. Figure 33 shows the simulated package's circuit diagram. The first complementary emitter follower uses a BC 639 and BC 640. The second complementary

emitter follower incorporates a TIP 31C and TIP 32C. The BC 639 and BC 640 have an f_T of 130 MHz and 50 MHz respectively while being able to dissipate 800 mW of power (D.A.T.A. BOOK 1988:191,220). Utilizing equation 3.4 and an IRF 610 high-power Mosfet with a C_{iss} of 140 pF, a V_{gs} of 12 V and a 7 MHz frequency results in,

$$P_{Gate} = 0,5 \times 140 \times 10^{-12} \times 12^2 \times 7 \times 10^6$$

$$P_{Gate} = 70 \text{ mW}$$

The value of C_{iss} is taken from the datasheet specifications for the IRF 610 (Annexure E). However, incorporating an IRF 140 Mosfet into the design would increase the required gate power to 837 mW, as its respective C_{iss} is 1660 pF (Annexure C). It is for this reason then that the second complementary emitter stage was included to handle this amount of power dissipation. The f_T of both the TIP 31C and TIP 32C are set at a minimum of 3 MHz according to the datasheet specifications (D.A.T.A. BOOK 1998:315,350).

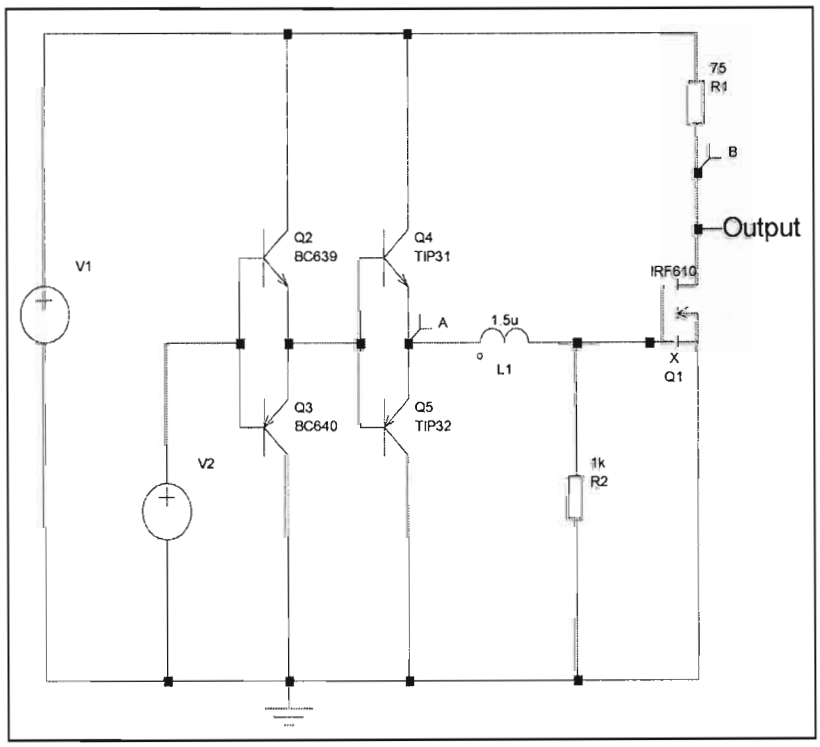

Figure 33 The circuit diagram of the complementary emitter followers, as present in the simulated package.

The supply voltage was initially set to 15 V. The input signal to the first complementary emitter stage was a 7 MHz 12 V peak square wave. A 50 % duty cycle was utilized with the total time period being 143 ns.

3.5 Summary

This chapter has focused on the amplification of the 5,5 V output signal of the frequency synthesizer in chapter 2. The voltage amplification section consists of 4 series connected HEX Schmitt triggers in package type 40106. Each set of inverters increases the voltage level by about 1,2 V so that the final output voltage swing is from ground to 12 V, at the maximum operating frequency of 8 MHz.

The final section, before connecting to the gate of the high-power Mosfet, consists of two complementary emitter followers connected in series. These two buffers provide the necessary impedance and current sourcing required by the gate of the Mosfet.

Chapter 4 will present the results obtained from the frequency generation stage as well as the results measured from the voltage amplification section and complementary emitter followers that serves as the Mosfet driver stage. Measured waveforms obtained at specific points on the final circuit board will be presented. The final circuit layout as well as the final printed circuit board will also be considered.

Chapter 4 The results

4.1 Introduction

Chapter 4 considers the measured results, in both time and frequency domain, of the completed high-frequency Mosfet driver. The simulated and experimental results of the complementary emitter circuit utilized in the high-frequency Mosfet driver section will also be presented. The measurements were obtained via the PICO-SCOPE ADC 200/100 spectrum analyser and the TEKTRONIX 100 MHz Digital Storage Oscilloscope.

4.2 The results of the high-frequency generation stage

The frequency generation stage comprises the PLL, programmable divider and frequency reference sections. These sections are present in figure 35 where the final circuit diagram with all relevant test points are shown. Figure 34 is obtained from test point A and illustrates a 7 MHz PLL output frequency.

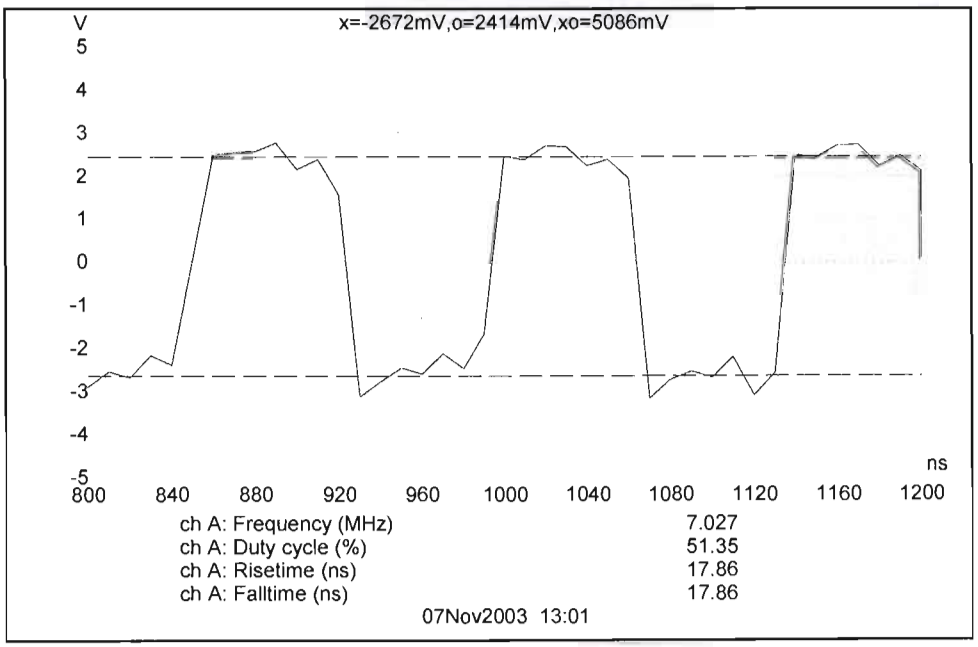

Figure 34 The 7 MHz output frequency signal taken from test point A.

Note the rise and fall time is around 18 ns while the duty cycle remains at roughly 50 %. The maximum output voltage of the PLL is consistent with the supply voltage of 5,5 V. The programmable divider, the 4526, has been set to 140. The frequency spectrum of the 7 MHz signal taken from test point A is shown in figure 36. Note the 2nd and 3rd harmonics at 14 and 21 MHz respectively.

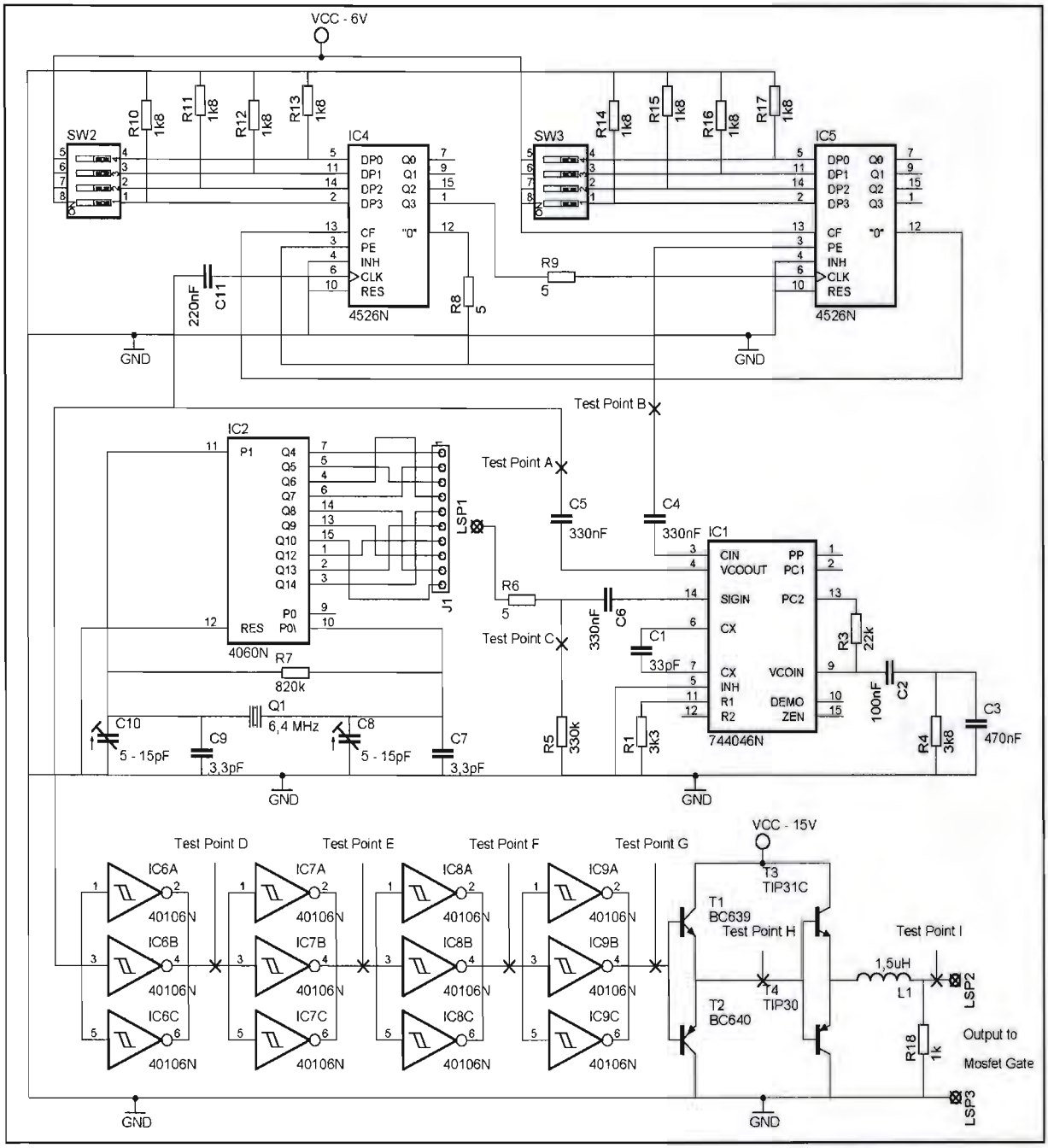

Figure 35 The complete circuit/block diagram of the high-frequency Mosfet driver.

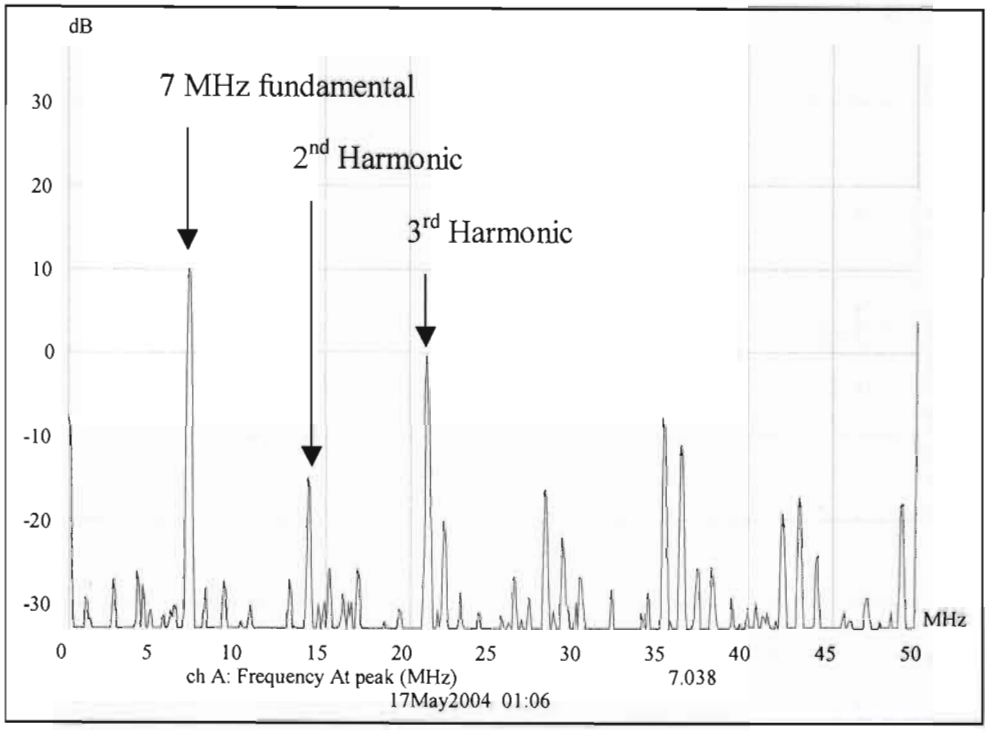

Figure 36 Frequency spectrum showing a 7 MHz frequency signal.

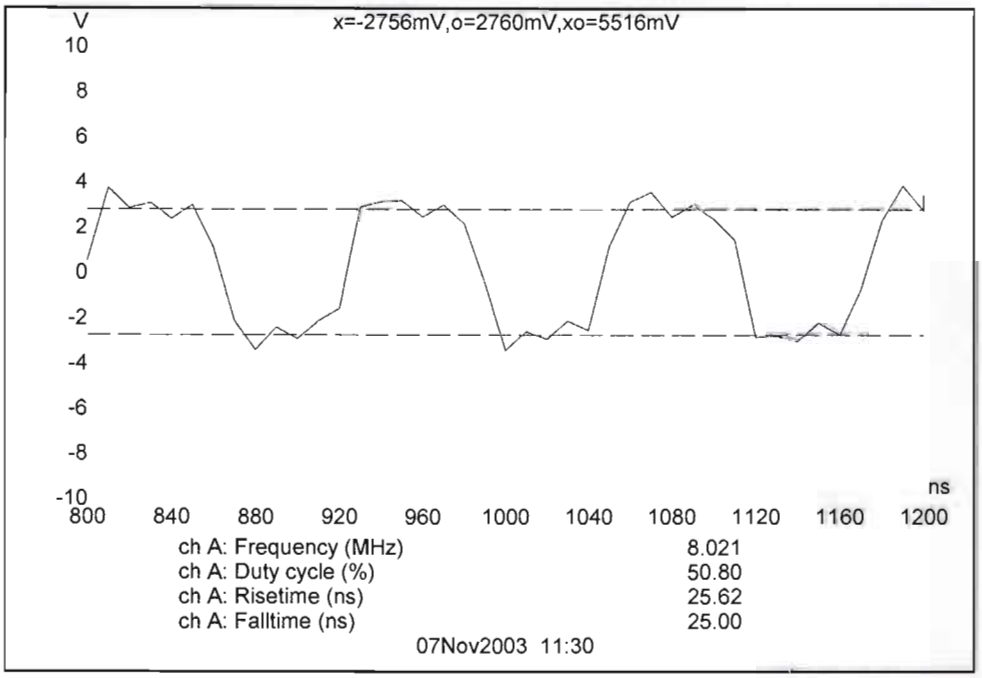

Figure 37 Maximum possible output frequency of 8 MHz obtained at test point A.

The maximum possible output frequency of the frequency generation stage measured via the digital oscilloscope at test point A is shown in figure 37. This 8 MHz output

frequency is accomplished by setting the dip switches on the divider circuit (the CMOS 4526) to divide by 160. Note that the output voltage remains around 5,5 V peak-to-peak while the rise and fall times are roughly 25 ns each. The duty cycle remains at 50 %. These values for rise and fall time as well as for duty cycle and peak-to-peak voltage remain more or less constant across the entire frequency range from 8 MHz down to 50 kHz. Figure 38 illustrates the 50 kHz output frequency measured at pin 9 of the 74HC 4046. The division factor on the dip switches connected to the divider section, the two 4526's, is set at 1, since both the reference frequency and output frequency are 50 kHz.

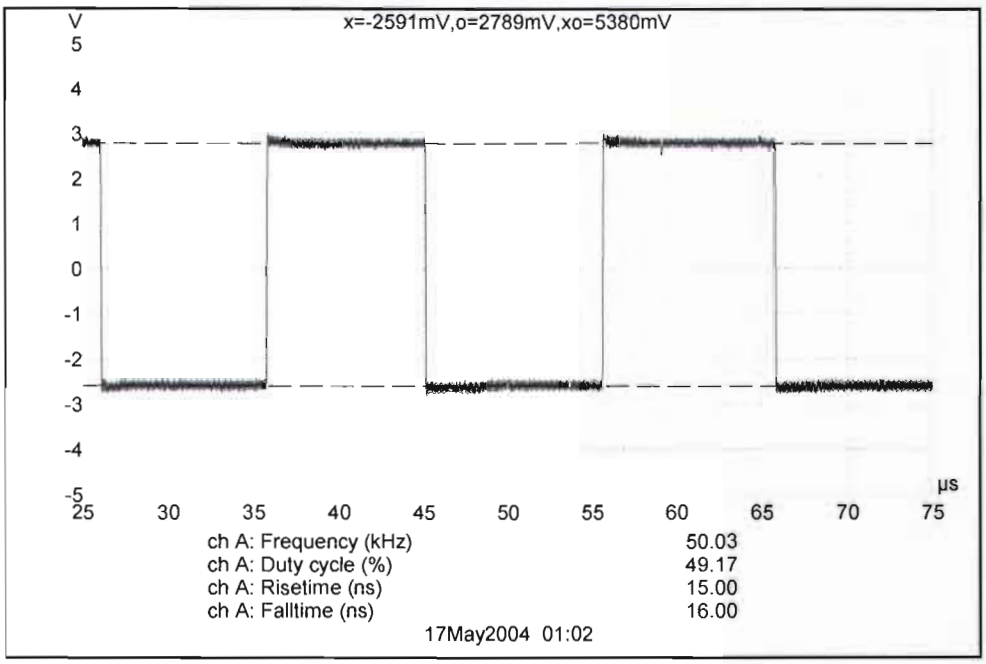

Figure 38 Minimum possible output frequency of 50 kHz obtained at test point A.

Figures 39 and 40 show the output frequency spectrum of the 74HC 4046 as seen via the digital spectrum analyser. The odd harmonics of the 8 MHz signal are evident in figure 39 while figure 40 highlights the harmonics of the 50 kHz minimum output frequency. A significant observation is that the amplitude level of both the 50 kHz and 8 MHz signals are roughly constant at 10 dB. This was also verified by the digital oscilloscope readouts as shown in figure 37 and figure 38, where the average peak-to-peak voltage remained at around 5,5 V, independent of frequency change.

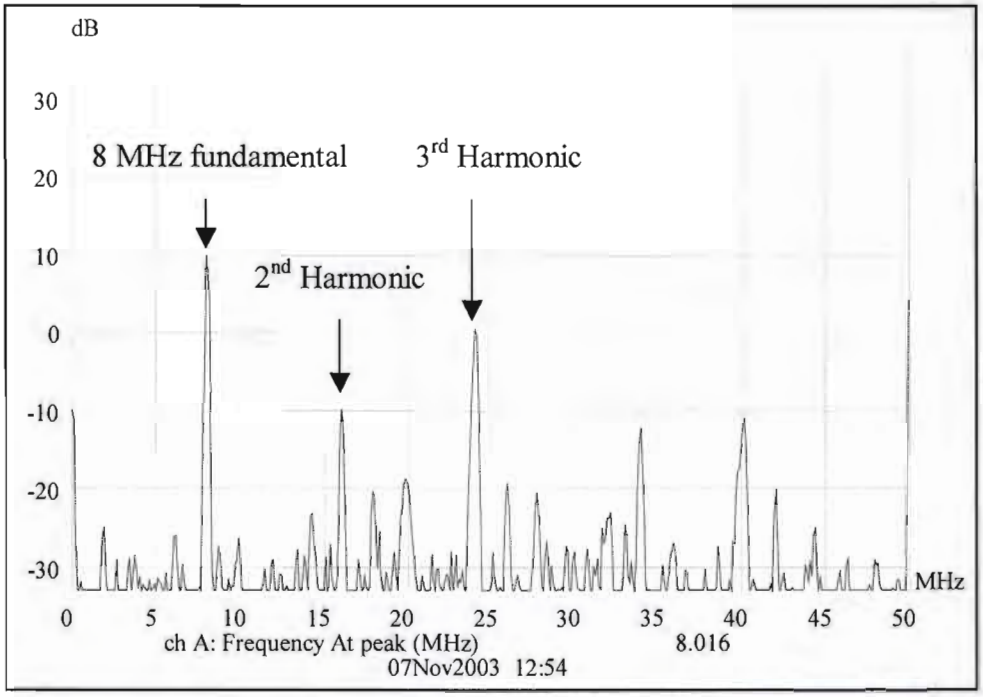

Figure 39 Maximum output frequency of 8 MHz displayed by a spectrum analyser.

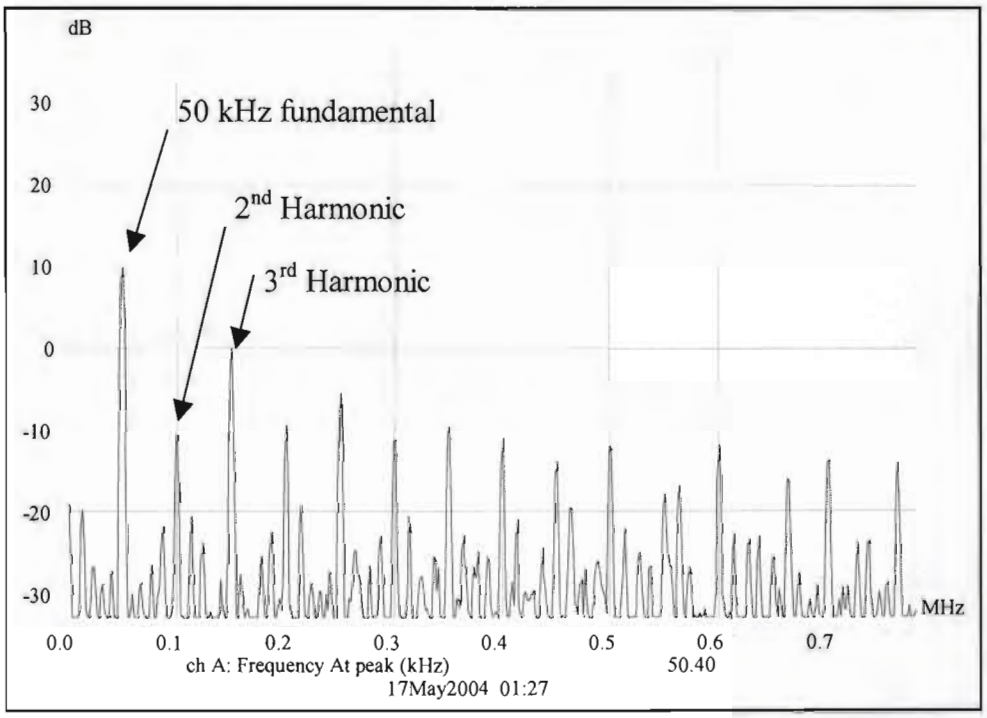

Figure 40 Minimum output frequency of 50 kHz displayed by a spectrum analyser.

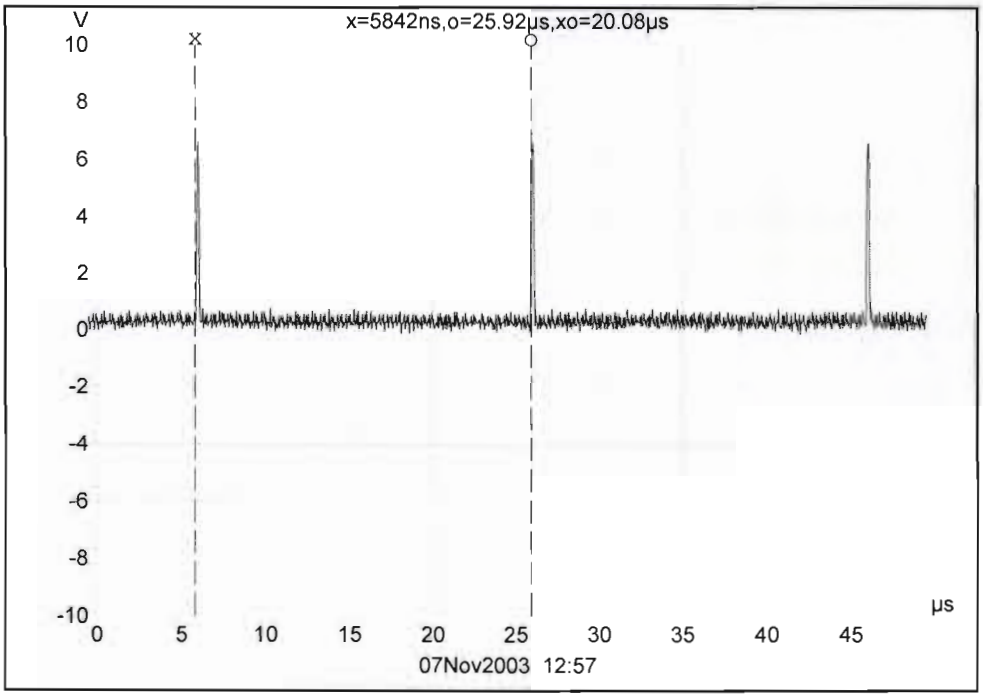

Figure 41 Divider section's output frequency obtained from test point B.

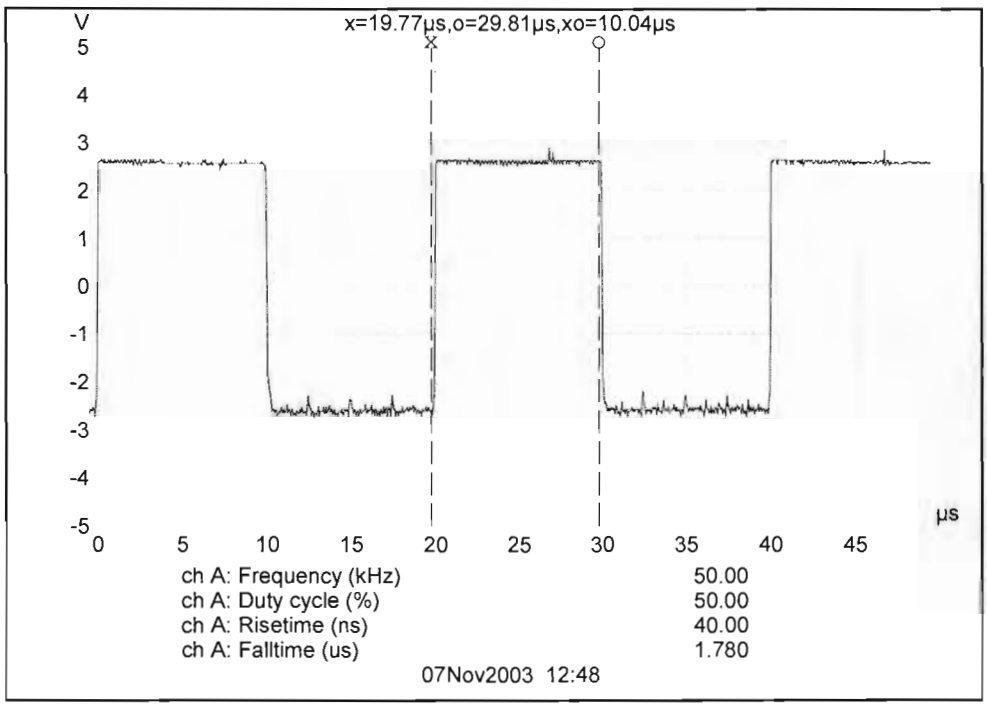

Figure 42 50 kHz output from the reference frequency section.

Figure 41 illustrates the output frequency of the divider section taken from test point B. Note that the duty cycle is around 5 %, which is acceptable for the input of the 2nd phase

comparator circuit in the 74HC 4046. This is because it makes use of D-type flip-flops that are positive-edge triggered devices. Other circuits will not be as lenient, and thus some type of signal conditioning will have to be performed. For instance, the reference single input circuitry of the 74HC 4046 will not function correctly if supplied with such a 5 % duty cycle signal. It is thus for this reason that the reference frequency is taken from pin 6 of the 4060, which provides a exact 50 % duty cycle as shown in figure 42. Figure 42 is the resulting signal from test point C. This is derived from a 6,4 MHz quartz crystal connected across pins 10 and 11. This 6,4 MHz frequency signal is then divided by a factor of 2^7 to give 50 kHz.

4.3 The results of the Mosfet driver stage

The Mosfet driver stage comprises a voltage amplification and gate drive section. The voltage amplification section consists of 4 CMOS HEX inverters, where 3 inverters on each IC are paralled. The outputs of each of the 4 CMOS HEX inverters, obtained from test points D through G (see figure 35), are shown in figures 43 through 46 respectively.

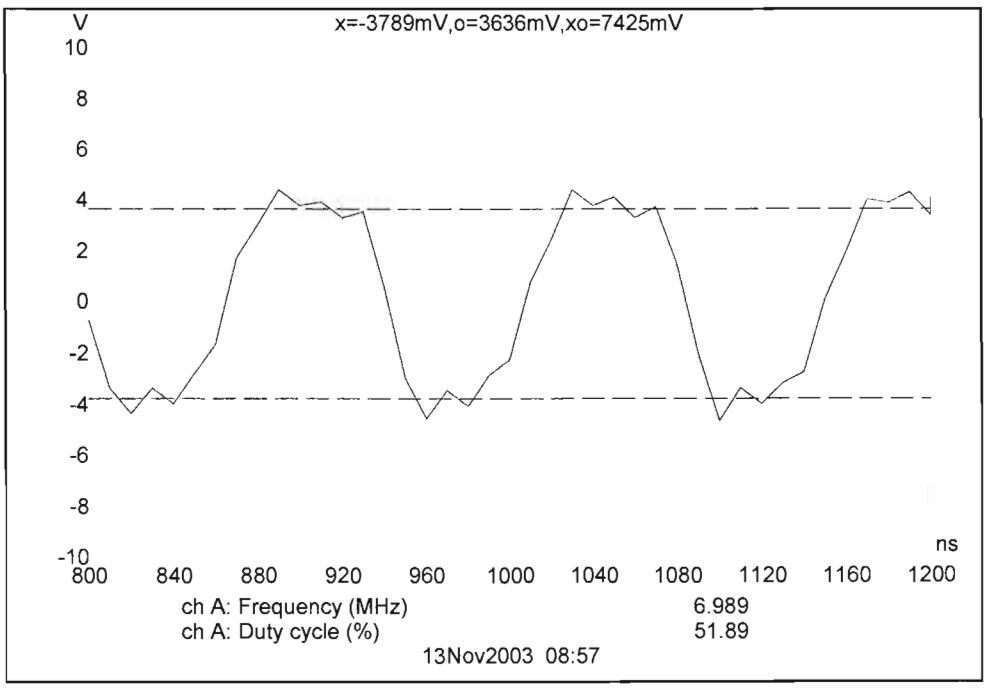

Figure 43 The first 40106's output within the voltage amplification section.

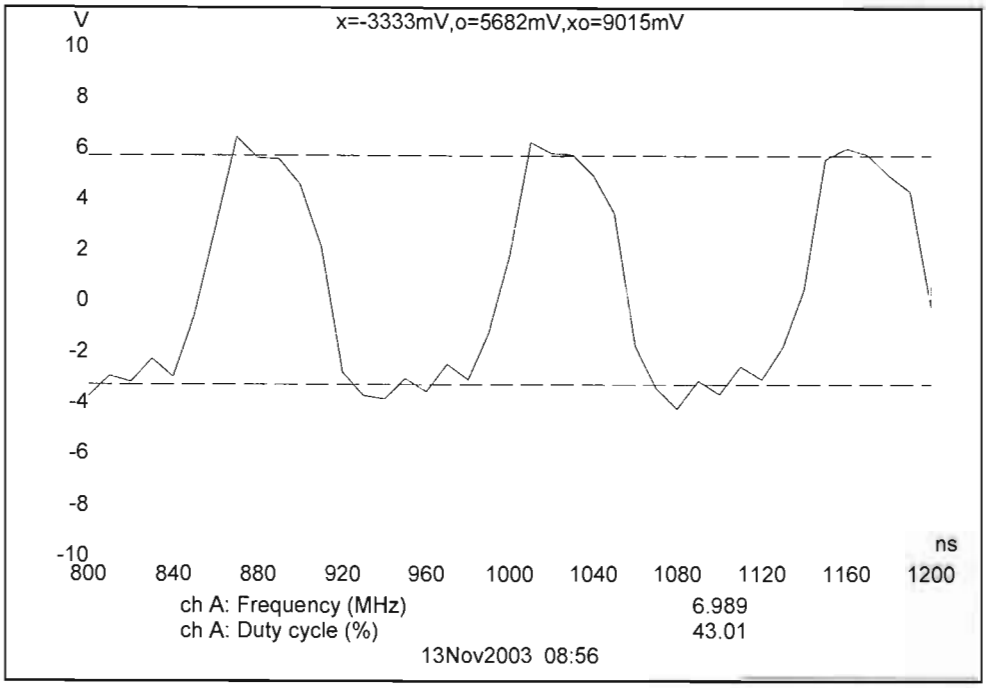

Figure 44 The second 40106's output within the voltage amplification section.

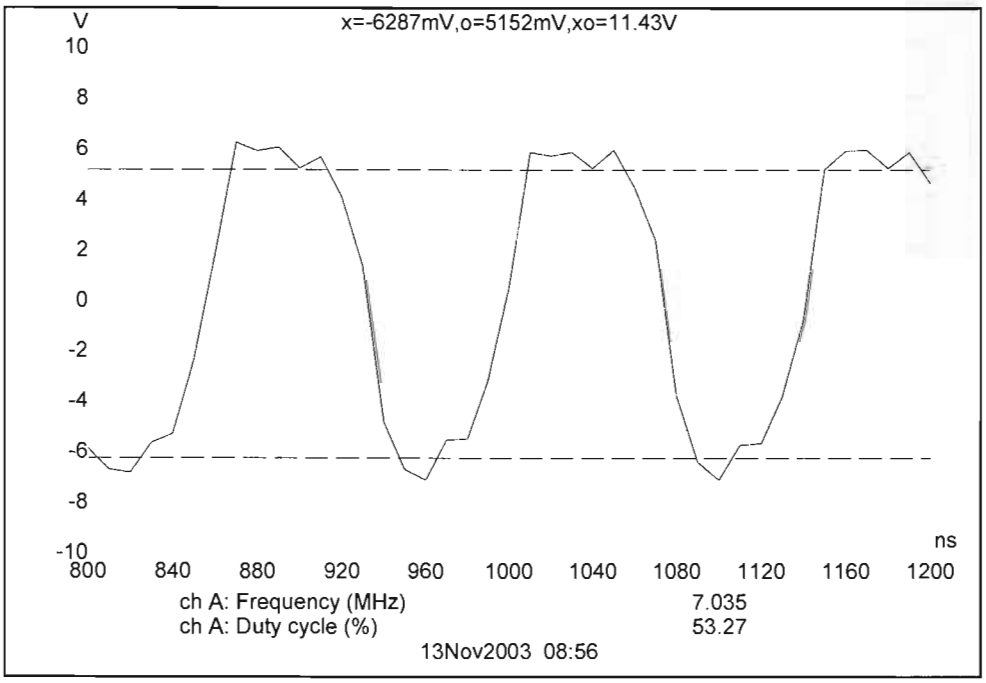

Figure 45 The output of the third 40106 within the voltage amplification section.

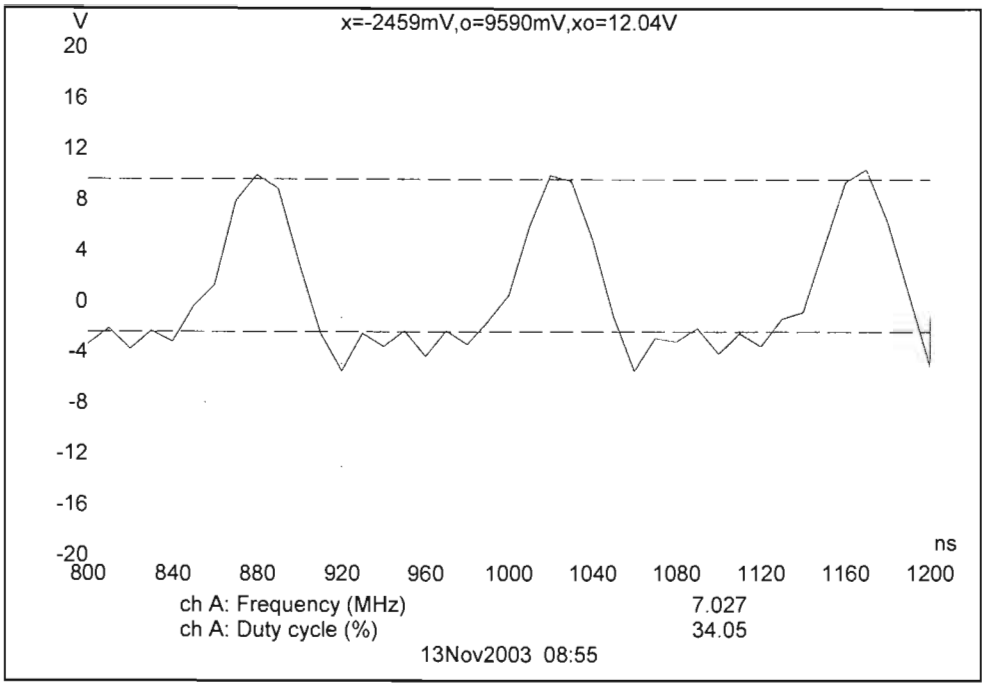

Figure 46 The output of the fourth 40106 within the voltage amplification section.

The above results show that the voltage amplification section is working correctly. Each HEX inverter does indeed provide a voltage increase of around 1,2 V. This then serves to increase the output from the frequency generation stage from 5,5 V to the required 12 V to successfully drive the gate of the high-power Mosfet. The output frequency spectrum from the last inverter IC, the 40106, of the amplification section is shown in figure 47. The 2^{nd} harmonic component is very evident at 14 MHz, while the third harmonic component has fallen somewhat. Recall from figure 36 that the output from the PLL for a frequency of 7 MHz contained a higher third harmonic component than the second harmonic component. The amplification section utilizing the four 40106 HEX inverters seem to reverse this phenomena and provide more amplification to the second harmonic component than to the third, as seen in figure 47. This frequency signal is now passed to the complementary emitter follower. Figure 48, taken from test point H in figure 35, portrays the output of the first complementary emitter follower that functions as the first buffer. The output voltage of the complementary emitter follower remains at 12,04 V, although the duty cycle is significantly less than 50 %. The output from the second buffer (figure 49) was obtained at test point I, when connected to the gate of the high-power

Mosfet comprising an IRF 610. The output duty cycle of 32 % does not significantly influence the switching characteristics of the high-power Mosfet.

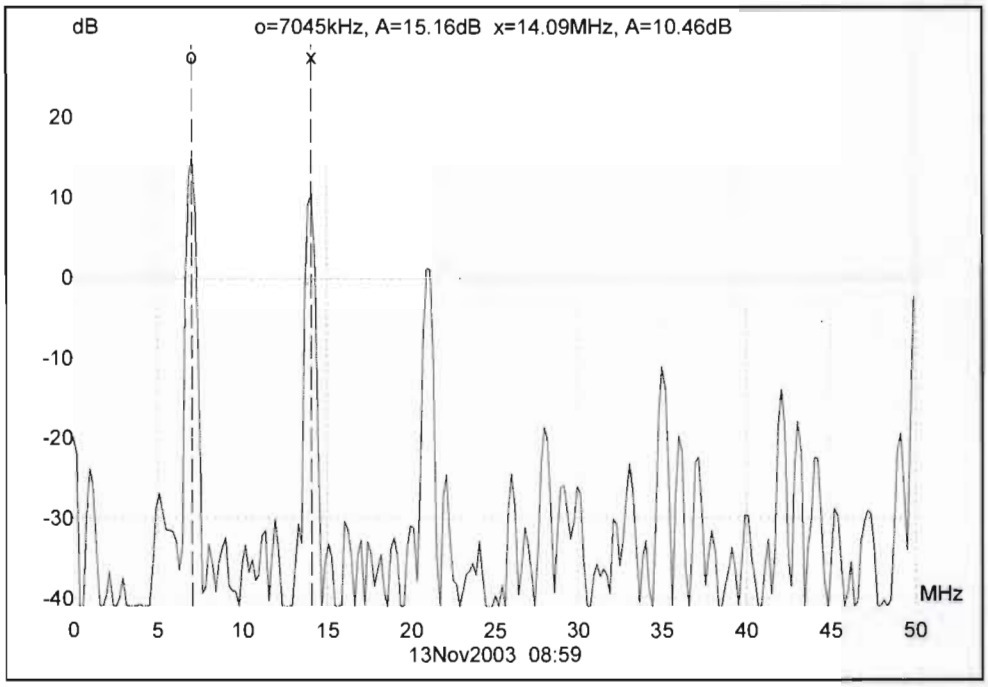

Figure 47 Output frequency spectrum of the voltage amplification section.

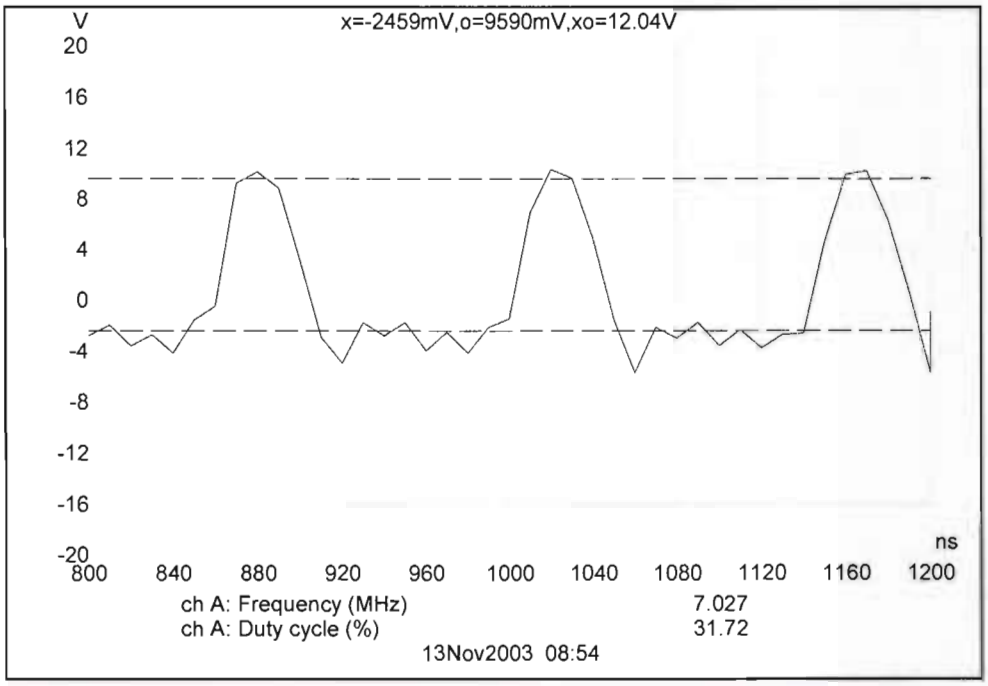

Figure 48 Output waveform of the first complementary emitter follower.

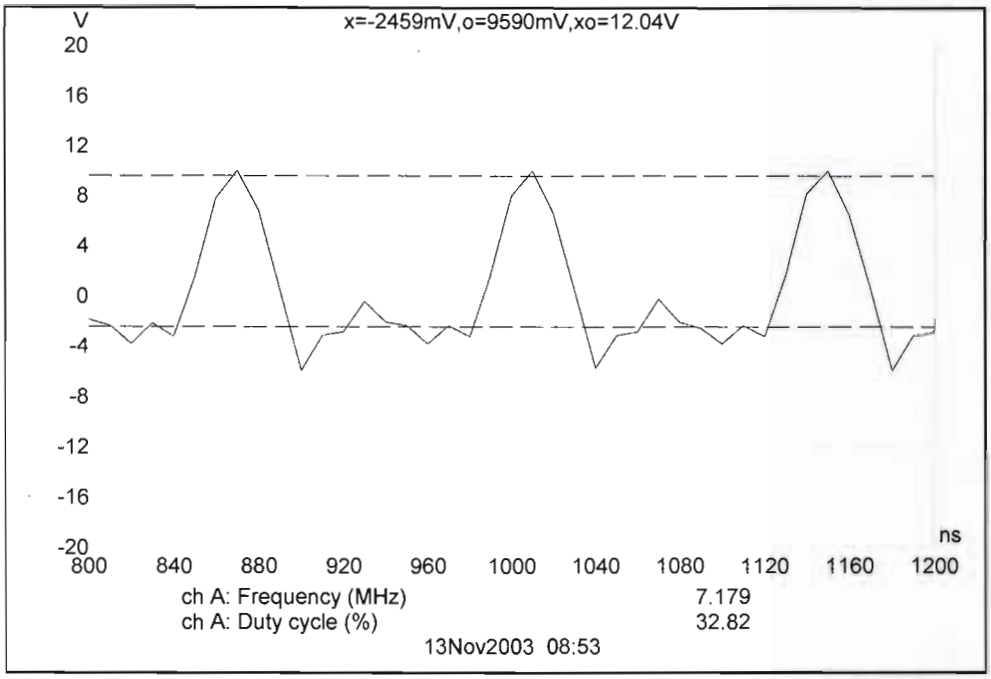

Figure 49 Output waveform of the second complementary emitter follower.

The effect of the complementary emitter follower on the gate of a high-power Mosfet was also investigated by means of a simulated model. Figure 50 shows the simulated model's result. Signal A represents the input signal to the Mosfet gate while signal B represents the output of the high-power Mosfet. The input voltage signal of 12 V, supplied by the complementary emitter follower, successfully switches the 15 V supply that is across the Mosfet. The frequency of operation was also calculated as 7 MHz, from the resulting time period. The simulated model's result for input signal to output signal for the Mosfet was then compared to the experimental models result. The experimental model's result is shown in figure 51, where the gate input signal and drain output signal are shown. Refer to figure 33 for this test point's location in the circuit. Comparing figures 50 to 51 yields no real significant differences except for the waveform shapes. Signal voltages and switching times are similar for both the simulated and experimental models. A comparison was also made between the outputs of the complementary emitter follower when connected to and when isolated from the gate of the high-power Mosfet. Figure 52 illustrates this comparison.

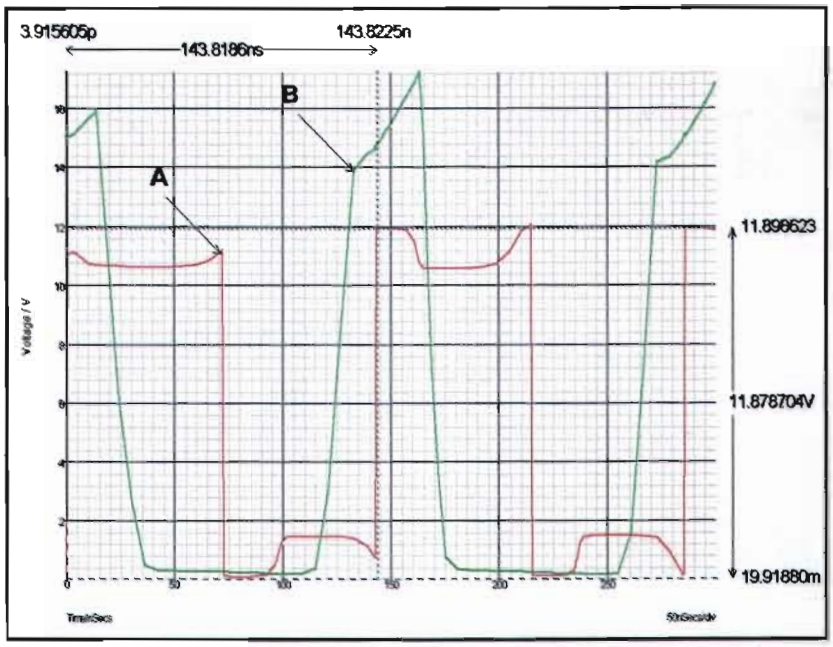

Figure 50 The simulated models result of the high-power Mosfet where; A – is the input to the Mosfet gate and; B – is the output from the Mosfet drain.

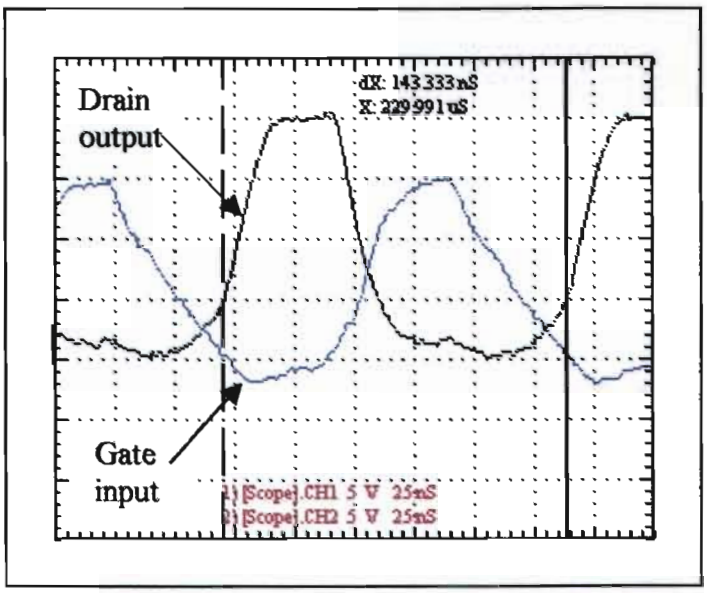

Figure 51 The input and output of the high-power Mosfet according to the experimental model.

No significant differences exist except for the zero voltage of the isolated gate being smoother than that of the connected gate. This is due to the influence of the gate

capacitances on the input voltage signal from the complementary emitter follower. The differences between the output voltage signals of the experimental and simulated models were investigated and are depicted in figure 53. Once again no significant differences exist, except for the experimental models flatter top voltage response.

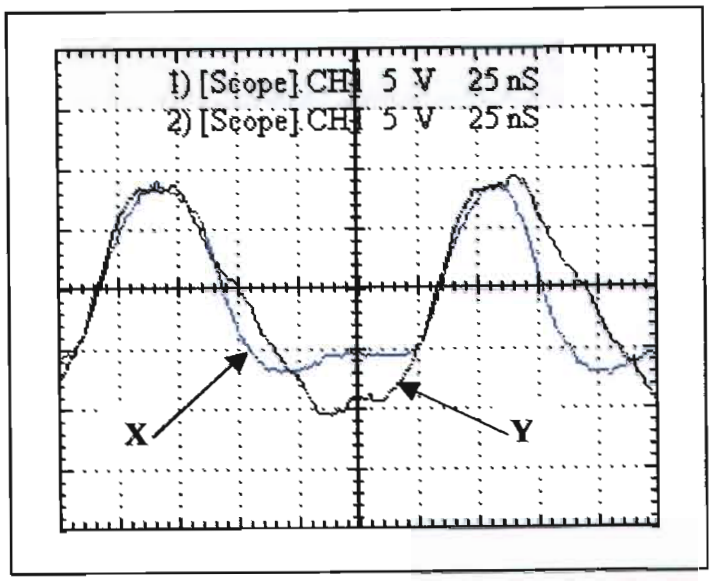

Figure 52 The output of the complementary emitter follower when; X – isolated from the Mosfet's gate and; Y – connected to the gate of the high-power Mosfet.

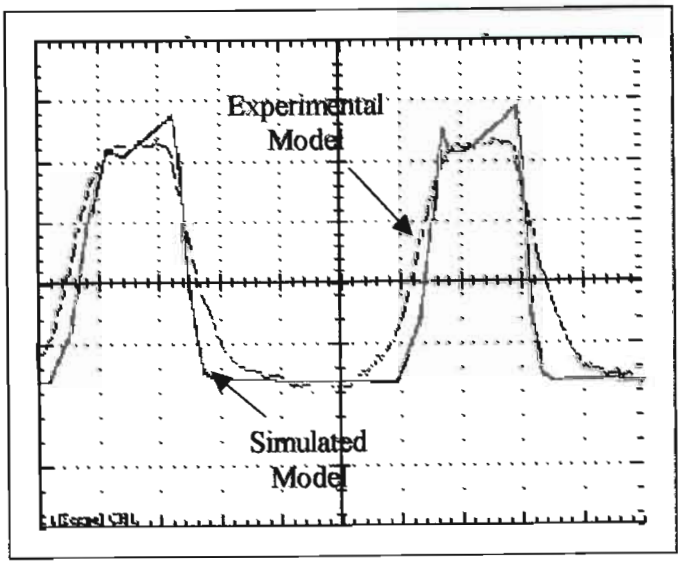

Figure 53 The simulated and experimental models result.

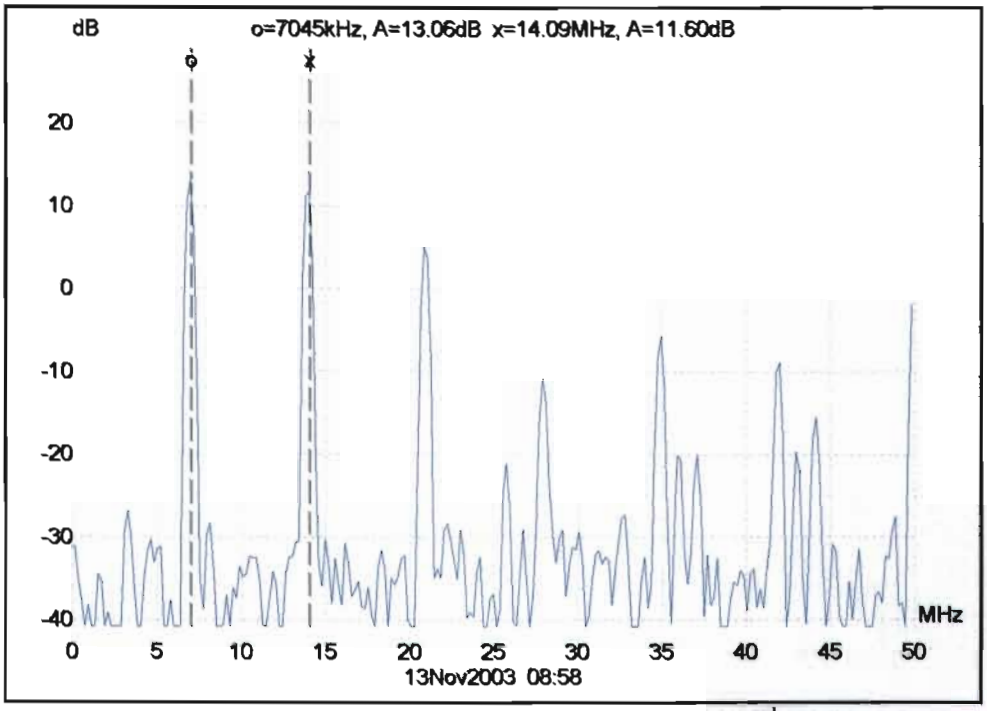

Figure 54 Frequency spectrum portraying the output of the 2nd buffer stage when connected to the gate of an IRF 610 high-power Mosfet utilized in a Class E amplifier.

The output frequency spectrum of the final buffer stage when connected to the gate of the high-power Mosfet is illustrated in figure 54. Note that the fundamental harmonic and the second harmonic are almost equal in power.

The complete circuit diagram of the high-frequency Mosfet driver is included as annexure F. The individual power supplies that feed the 4 separate inverters in the voltage amplification section are evident on the left side of the circuit diagram (Annexure F). The printed circuit board appears in annexure G while annexure H contains a photo of the completed high-frequency Mosfet driver.

4.4 Summary

The measurements and results of the high-frequency Mosfet driver have been comprehensibly covered in this particular chapter. The output waveforms from the

frequency generation stage incorporating the 74HC 4046 PLL, 4526 divider and 4060 ripple counter have been presented. The results of the voltage amplification section and complementary emitter follower have also been discussed. The final waveforms from across the IRF 610 Mosfet indicates the successful switching of the Mosfet at 7 MHz. This has been confirmed by both the experimental and simulated models results. Swart and Pienaar (2004) presented the experimental results at the SAUPEC 2004 conference held at the University of Stellenbosch, South Africa. Swart, Pienaar and Case (2004) furthermore presented the simulated results of the gate drive circuit at the AFRICON 2004 conference held in Gaborone, Botswana.

The final chapter of this research project, chapter 5, will consider the conclusions reached with regard to the design and development of the high-frequency Mosfet driver. Recommendations as to future research on high-frequency Mosfet drivers will also be put forward.

Chapter 5 Conclusions and recommendations

5.1 Introduction

The final chapter of this research document presents the conclusions reached with regard to the design and development of a high-frequency Mosfet driver. The original purpose will be reviewed together with the final results of the high-frequency Mosfet driver. Recommendations for future research will conclude this chapter.

5.2 Conclusions

One of the most notable conclusions that can be made from this project is the flexibility, efficiency and reliability of the PLL circuit. A number of prototypes were manufactured in the design and development of the frequency generation stage. Each of the prototypes, while not functioning according to expectation, produced a stable output frequency based on an equally stable input frequency. The lock range, of the first prototype, was found to exist between 98 kHz and 1,144 MHz, when utilizing a timing capacitor, C1, of 180 pF. See figure 35 for C1's position. At this time only a single capacitor, C2, was being utilized in the low-pass filter configuration. It was found that a smaller loop filter capacitance of 15 pF used in conjunction with phase comparator 1 would result in a smaller amount of VCO output frequency variations. A wiring error had though occurred between the PLL and divider section that was rectified in the second prototype.

The second prototype would though only operate between 200 kHz and 800 kHz. The value of C1 had remained constant but the value of the loop filter's capacitor had changed to 100 nF. The reason for making the loop filter's capacitor larger was that, although variations within the output frequency range where being combated with lower values of C2, the lock range was being lowered and high output frequencies were not being produced. Phase comparator 1 was still being utilized, as it was desired to have the free-running frequency at the middle of the lock range when no input signal was available. Now with the low-pass filter set at 100 nF, oscillation in the order of 3 kHz

readily occurred at higher frequencies of 500 kHz and above. This is where Lythall's (2002:1) design was utilized incorporating a paralleled resistance and capacitance in series with a single capacitor to ground. A 470 nF capacitor was paralled with a 3,3 kΩ resistor and a 100 nF capacitor in series to ground. All oscillations stopped and a perfect square wave originated at the output with no visible distortions. Frequency lock was achieved much quicker, with no excess drifting of the locked frequency. Thus, it can be concluded that an existing PLL circuit can be improved utilizing the improved low-pass filter technique from Lythall (2002:1). It was further decided to move to phase comparator 2, as this would make the capture and lock range equal. It would also eliminate the possibility of the output frequency locking onto the harmonics of the reference input signal. The CMOS-based 4059 was utilized as the divider section. It is a divide-by-N counter capable of a maximum count of 15000, but being restricted to an input clock frequency of 2 MHz.

With the PLL circuit operating correctly, attention was then directed to a new divider section comprising the 4526. A third prototype was developed using the specifications of the second prototype for the PLL, but incorporating the 4526 as the divider section so as to attain frequencies higher than 2 MHz. The third prototype was completed and tested. It was found that the divider section was not operating correctly at frequencies above 2 MHz. A divide-by-4 prescaler was thus included into the 4th prototype. The idea was to divide the maximum output frequency by 4, which would then result in a frequency below 2 MHz, a frequency that the divider IC, the 4526, could accommodate. This proved successful and the frequency synthesizer was operating correctly between 50 kHz and 8 MHz in 50 kHz steps. Then, instead of utilizing a 5 V regulator to feed the frequency synthesizer section, a 6 V regulator was used to feed the divider and reference section, while a diode was added in line to the PLL circuit, so that its voltage remained at below 5,5 V. This then enabled frequency operation upwards of 10 MHz by the divider section, the 4526. A noteworthy deduction here is that just a half a volt increase on the supply voltage to the 4526 makes it operate at frequencies above 2 MHz. The prescaler could now be discarded and the final and fifth prototype could be constructed.

Subsequent measurements confirmed the successful operation of the frequency generation stage. Attention was now directed at the Mosfet driver stage.

Focus was directed to the amplification of the 5,5 V signal received from the 74HC 4046. It was initially assumed that the use of 4 HEX inverter IC's would increase the voltage level of the maximum output frequency of the PLL to an acceptable level to drive the gate of a high-power Mosfet. This was implemented and worked immediately. However, the 40106 could not provide sufficient drive to the Mosfets gate as it cannot source and sink large amounts of peak current. Therefore, 2 complementary emitter followers were included to source and sink the peak currents that flowed into and out off the Mosfets gate. Results were immediately forthcoming and successful. The most notable conclusion is that complementary emitter followers proved to be very successful in driving the gate of the high-power Mosfets, even at high frequencies.

The original purpose to design and develop a high-frequency Mosfet driver was achieved. The generation of frequencies between 50 kHz and 8 MHz in 50 kHz steps was accomplished by the frequency generation stage utilizing a coherent, indirect, frequency synthesizer. This frequency synthesizer incorporated a PLL, divider circuit and reference frequency section. Supplying sufficient drive to the gate of a high-power Mosfet was addressed by the use of 4 HEX inverters and 2 complementary emitter followers. The effectiveness of the complementary emitter followers was proven both in the simulated and experimental models.

5.3 Recommendations

A number of IC's have been developed that include both the divider and the reference frequency section. Investigation into the possible use of these circuits in place of the three separate sections currently used could lead to the simplification of the overall board construction. Smaller board designs could thus be forthcoming. Utilizing the IRF 610 Mosfet accomplished the desired on and off switching time of less than 70 ns, which equates to a frequency of around 8 MHz. However, it does not have the capability of

handling large amounts of power. Connecting 2 or more IRF 610's in parallel could solve the problem of delivering larger amounts of power to the load. This aspect remains to be investigated with regard to high-frequency Mosfet drivers.

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List of Annexures

INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4046A
Phase-locked-loop with VCO

Product specification 1997 Nov 25
Supersedes data of September 1993
File under Integrated Circuits, IC06

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI.

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is: $V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi}$ (V/r).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig.6. The average of V_{DEMOUT} is equal to $\frac{1}{2}V_{CC}$ when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig.7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range.
This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig.5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed,

$$\text{is: } V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

$$\text{The phase comparator gain is: } K_p = \frac{V_{CC}}{4\pi}\,(V/r)\,.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig.8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig.9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed,

$$\text{is: } V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

$$\text{The phase comparator gain is: } K_p = \frac{V_{CC}}{2\pi}\,(V/r)\,.$$

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig.10. Typical waveforms for the PC3 loop locked at f_o are shown in Fig.11.

The phase-to-output response characteristic of PC3 (Fig.10) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC3, to its lowest frequency.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF; R1 = 3 kΩ; V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in V.

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

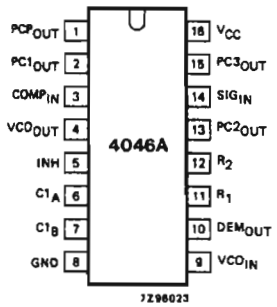


Fig.1 Pin configuration.

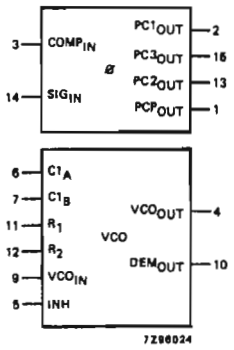


Fig.2 Logic symbol.

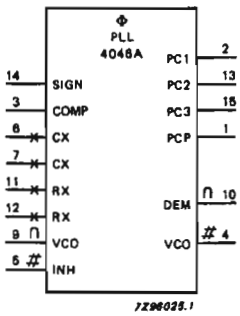


Fig.3 IEC logic symbol.

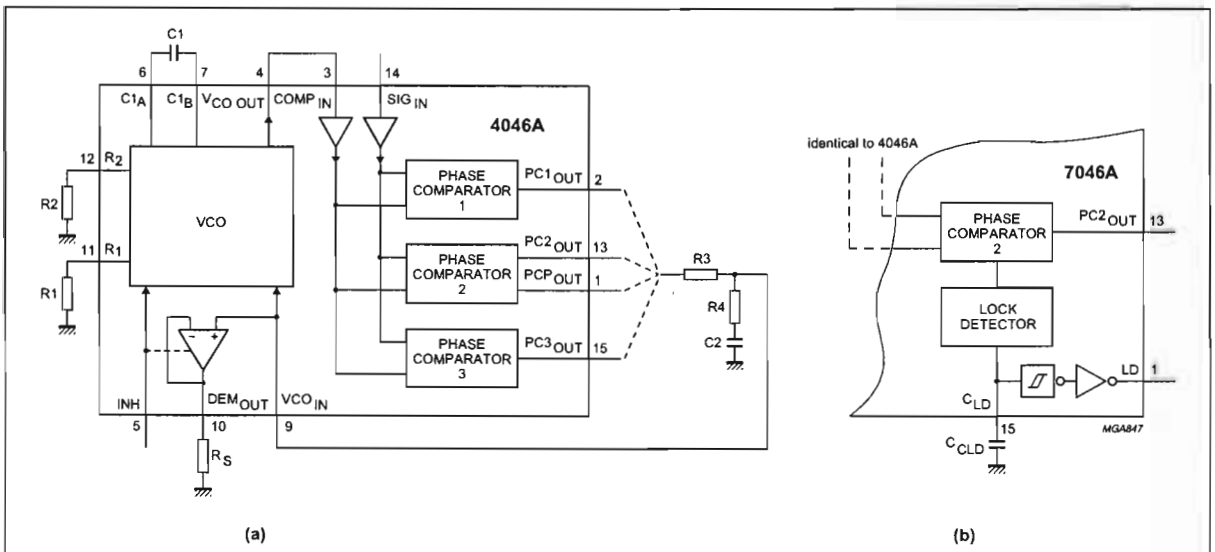


Fig.4 Functional diagram.

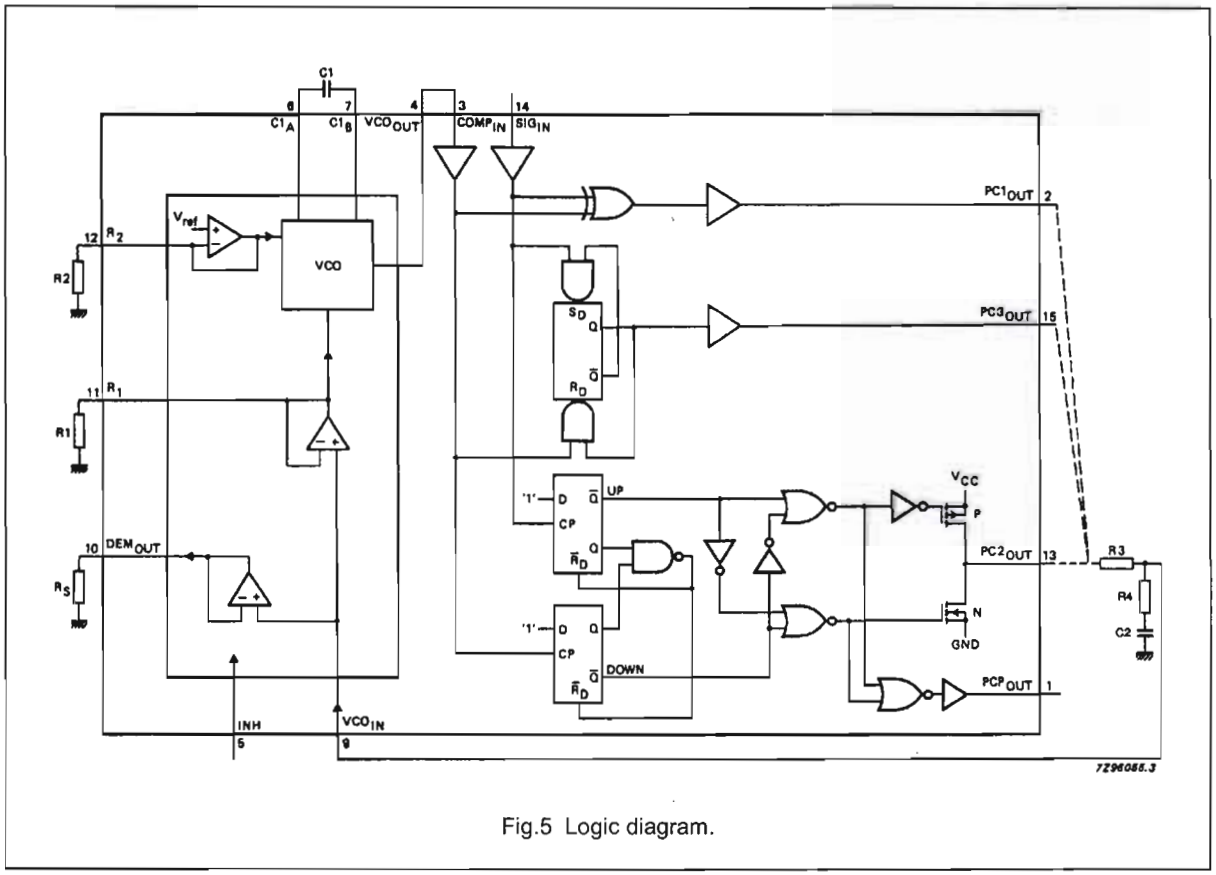
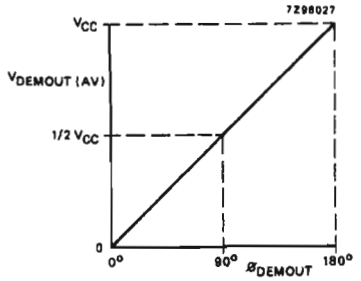


Fig.5 Logic diagram.



$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

Fig.6 Phase comparator 1: average output voltage versus input phase difference.

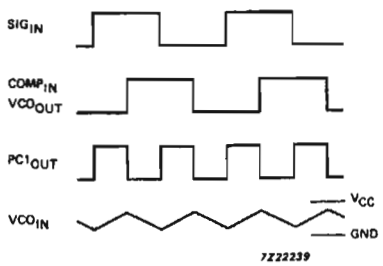
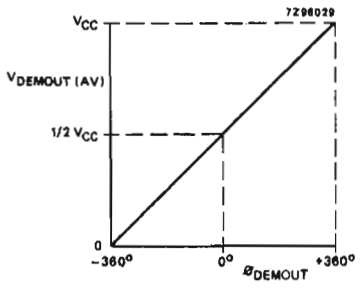


Fig.7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.



$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi C_{OMPIN})$.

Fig.8 Phase comparator 2: average output voltage versus input phase difference.

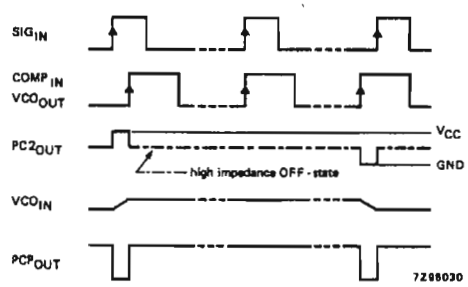
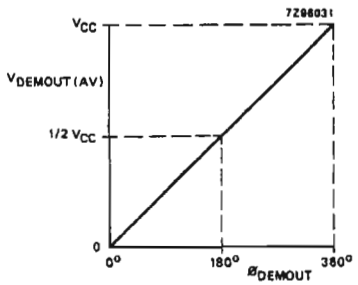


Fig.9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.



$$V_{DEMOUT} = V_{PC3OUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN}).$$

Fig.10 Phase comparator 3: average output voltage versus input phase difference:

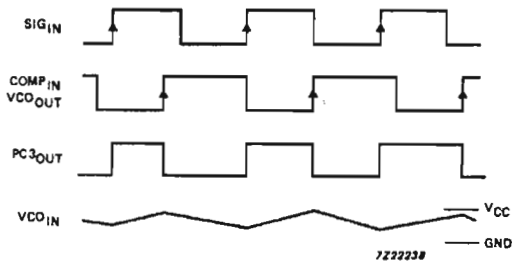


Fig.11 Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	–40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	–40		+125	–40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000		6.0	500	ns	V_{CC} = 2.0 V
			6.0	500		6.0	500	ns	V_{CC} = 4.5 V
			6.0	400		6.0	500	ns	V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: – 40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above + 70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above + 70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	V_O = V_{CC} or GND

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ kΩ kΩ	3.0 4.5 6.0	V_I at self-bias operating point; ΔV_I = 0.5 V; see Figs 12, 13 and 14	

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R_2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 4.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to+85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at R_S > 300 kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; values taken over R_S range; see Fig.15
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	V_{DEMOUT} = 1/2 V_{CC}

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.16
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig.16
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.16
t_{PZH}/ t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig.17
t_{PHZ}/ t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig.17
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.16
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig.18
f_o	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig.19
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	µA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	µA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min	typ.	max	min	max	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
R_I	input resistance SIG_{IN}, $COMP_{in}$		250						kΩ	4.5	V_I at self-bias operating point; ΔV_I = 0.5 V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min	typ.	max	min	max	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R_2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at R_S > 300 kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; values taken over R_S range; see Fig.15
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	V_{DEMOUT} = 1/2 V_{CC}

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		23	40		50		60	ns	4.5	Fig.16
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		35	68		85		102	ns	4.5	Fig.16
t_{PHL}/ t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		28	54		68		81	ns	4.5	Fig.16
t_{PZH}/ t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		30	56		70		84	ns	4.5	Fig.17

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHZ}/ t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		36	65		81		98	ns	4.5	Fig.17
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.16
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max	min.	max	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig.18b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig.19
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

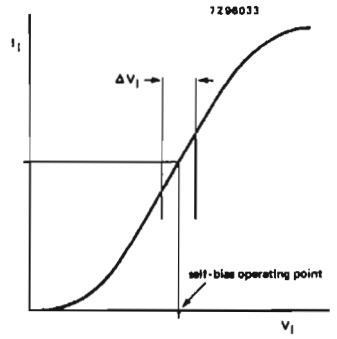


Fig.12 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

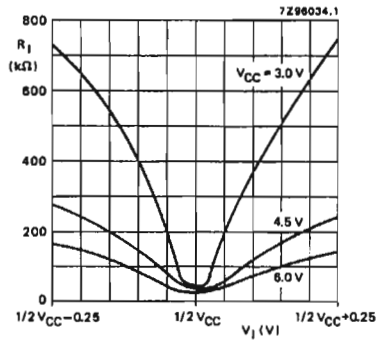


Fig.13 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

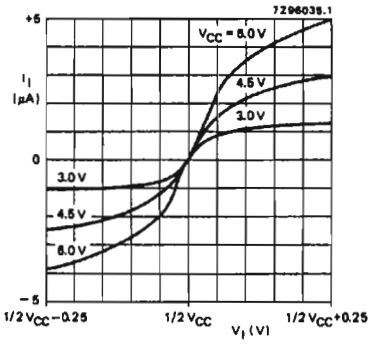
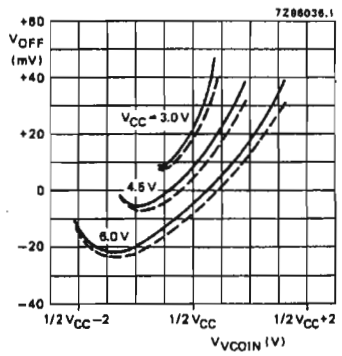


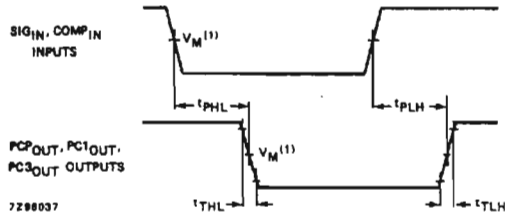
Fig.14 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



—— R_S = 50 kΩ
- - - - R_S = 300 kΩ

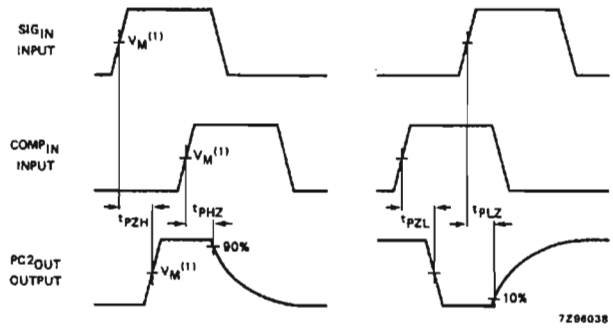
Fig.15 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS



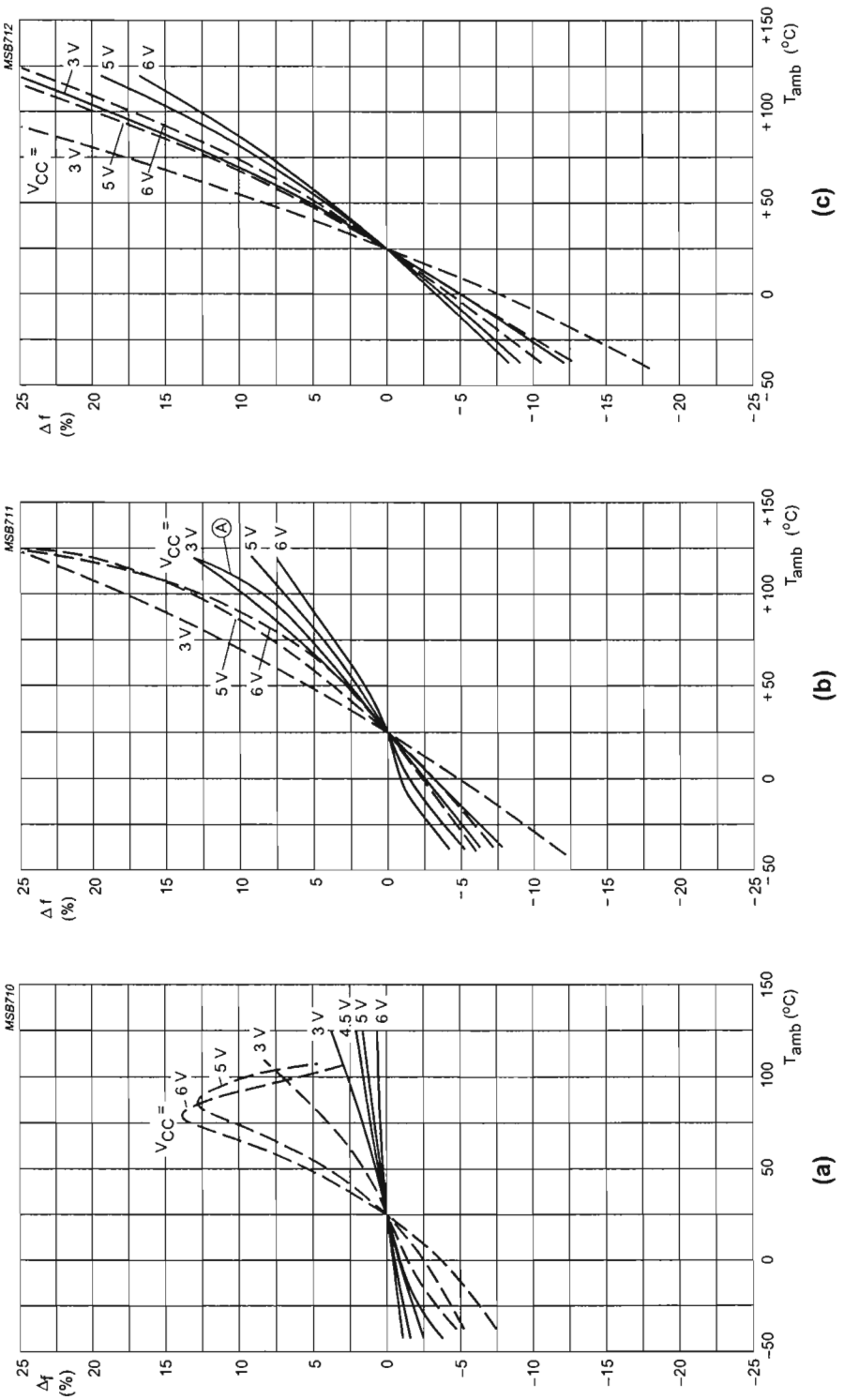
(1) HC : V_M = 50%; V_I = GND to V_{CC}

Fig.16 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.



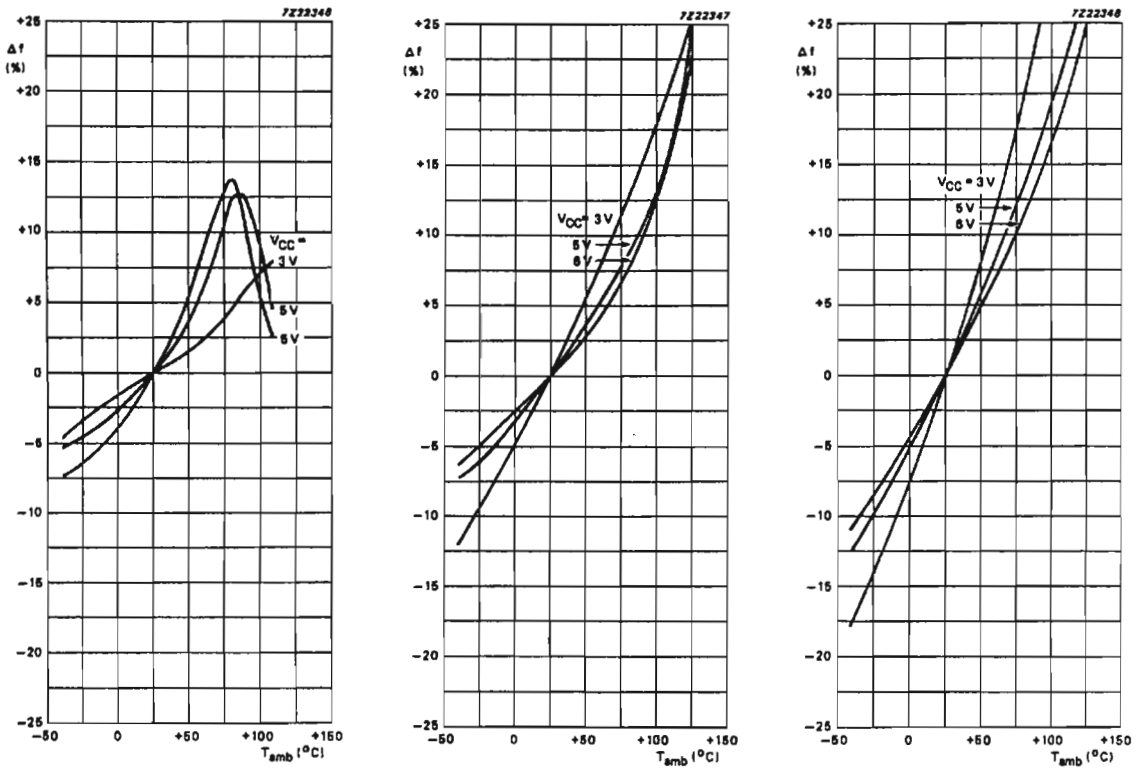
(1) HC : V_M = 50%; V_I = GND to V_{CC}

Fig.17 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.



To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
—— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO\ IN}$ = 0.5 V_{CC}.



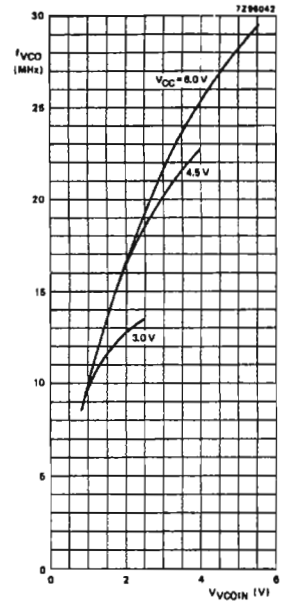
(d) $R_2 = 3\ k\Omega$, $R_1 = \infty$

(e) $R_2 = 10\ k\Omega$, $R_1 = \infty$

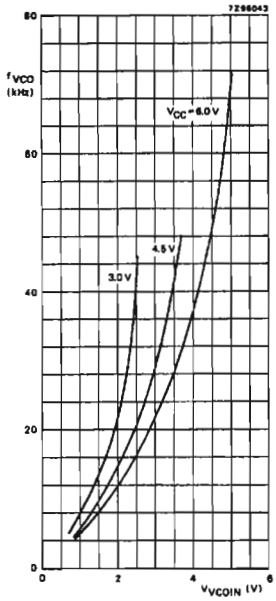
(f) $R_2 = 300\ k\Omega$, $R_1 = \infty$

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

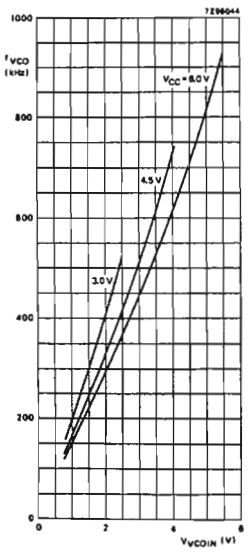
Fig.18 Continued.



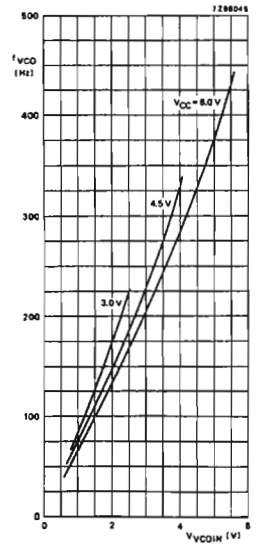
(a) R_1 = 3 kΩ; C_1 = 40 pF



(b) R_1 = 3 kΩ; C_1 = 100 nF



(c) R_1 = 300 kΩ; C_1 = 40 pF



(d) R_1 = 300 kΩ; C_1 = 100 nF

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

Fig.19 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

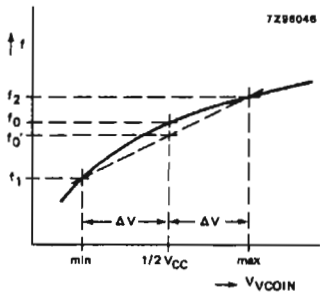


Fig.20 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the V_{CC} range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

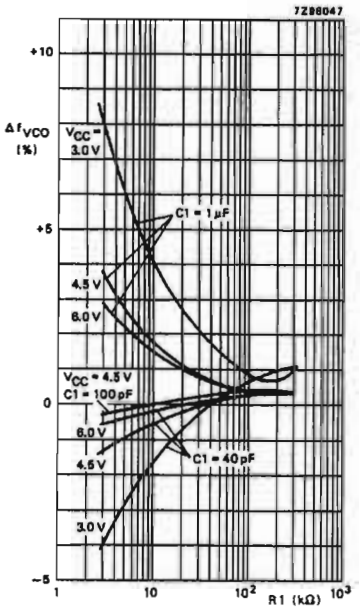
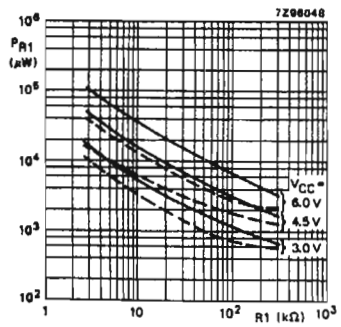
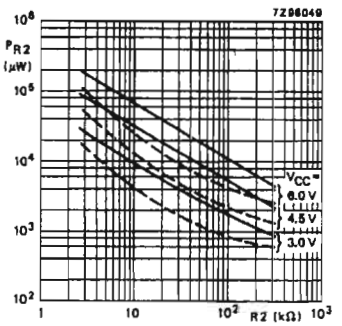


Fig.21 Frequency linearity as a function of R1, C1 and V_{CC}: $R2 = \infty$ and $\Delta V = 0.5$ V.



—— C1 = 40 pF
- - - - C1 = 1 μF

Fig.22 Power dissipation versus the value of R1: $C_L = 50$ pF; $R2 = \infty$; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.



—— C1 = 40 pF
- - - - C1 = 1 μF

Fig.23 Power dissipation versus the value of R2: $C_L = 50$ pF; $R1 = \infty$; $V_{VCOIN} = GND = 0$ V; $T_{amb} = 25$ °C.

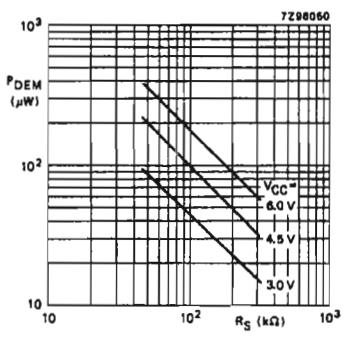


Fig.24 Typical dc power dissipation of demodulator sections as a function of R_S: $R1 = R2 = \infty$; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

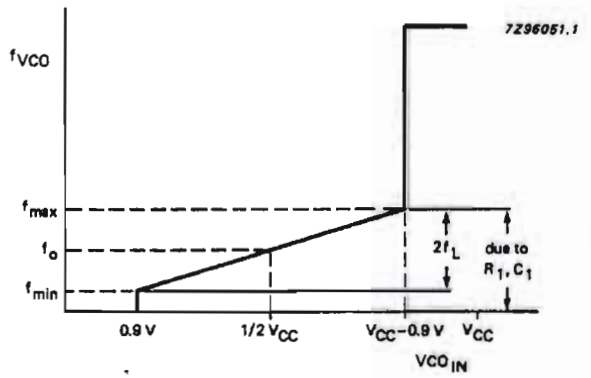
APPLICATION INFORMATION

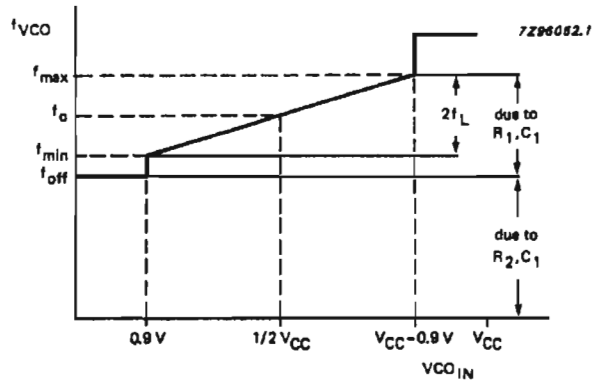
This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

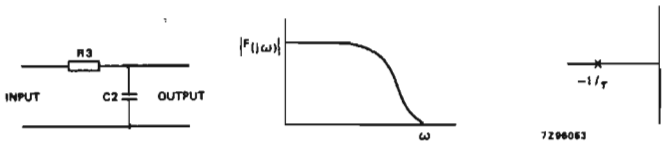
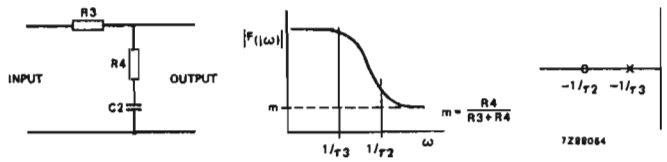
References should be made to Figs 29, 30 and 31 as indicated in the table.

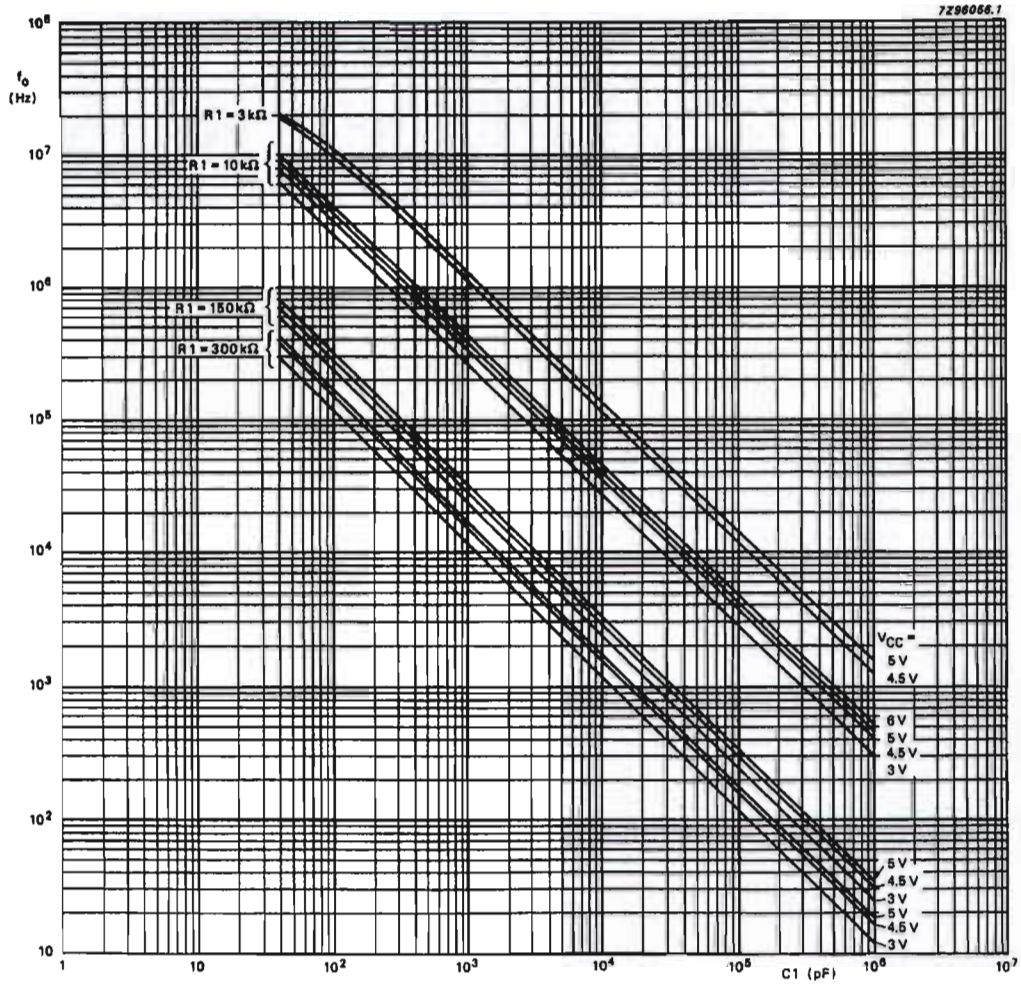
Values of the selected components should be within the following ranges:

R1 between 3 kΩ and 300 kΩ;
R2 between 3 kΩ and 300 kΩ;
R1 + R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.25. (Due to R1, C1 time constant a small offset remains when R2 = ∞.).
		 Fig.25 Frequency characteristic of VCO operating without offset: f_0 = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig.29.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig.29, use Fig.31 to obtain $2f_L$ and then use this to calculate f_{min}.

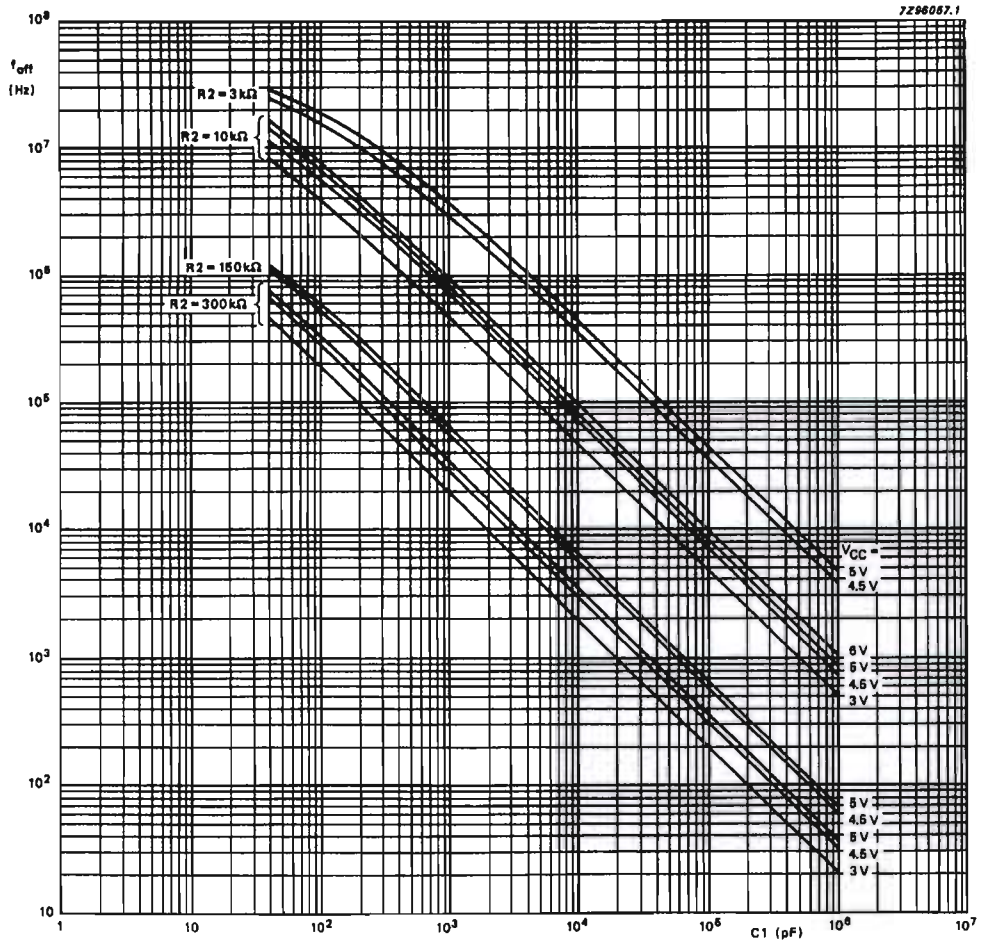
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.26.  Fig.26 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig.31. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig.30. Calculate the value of R1 from the value of C1 and the product R1C1.
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig.6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig.8).
	PC3	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig.10).

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx \frac{1}{\pi}\sqrt{2\pi f_L/\tau}$ Fig. 27 Simple loop filter for PLL without offset; R3 ≥ 500 Ω.  (a) τ1 = R3 x C2; (b) amplitude characteristic (c) pole-zero diagram τ2 = R4 x C2; τ3 = (R3 + R4) x C2 Fig.28 Simple loop filter for PLL with offset; R3 + R4 ≥ 500 Ω.
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°
	PC3	$f_r = f_i$, large ripple content at ϕ_{DEMOUT} = 180°



To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
Interpolation for various values of R1 can be easily calculated because a constant R1C1 product will produce almost the same VCO output frequency.

Fig.29 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.



To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
Interpolation for various values of R2 can be easily calculated because a constant R2C1 product will produce almost the same VCO output frequency.

Fig.30 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

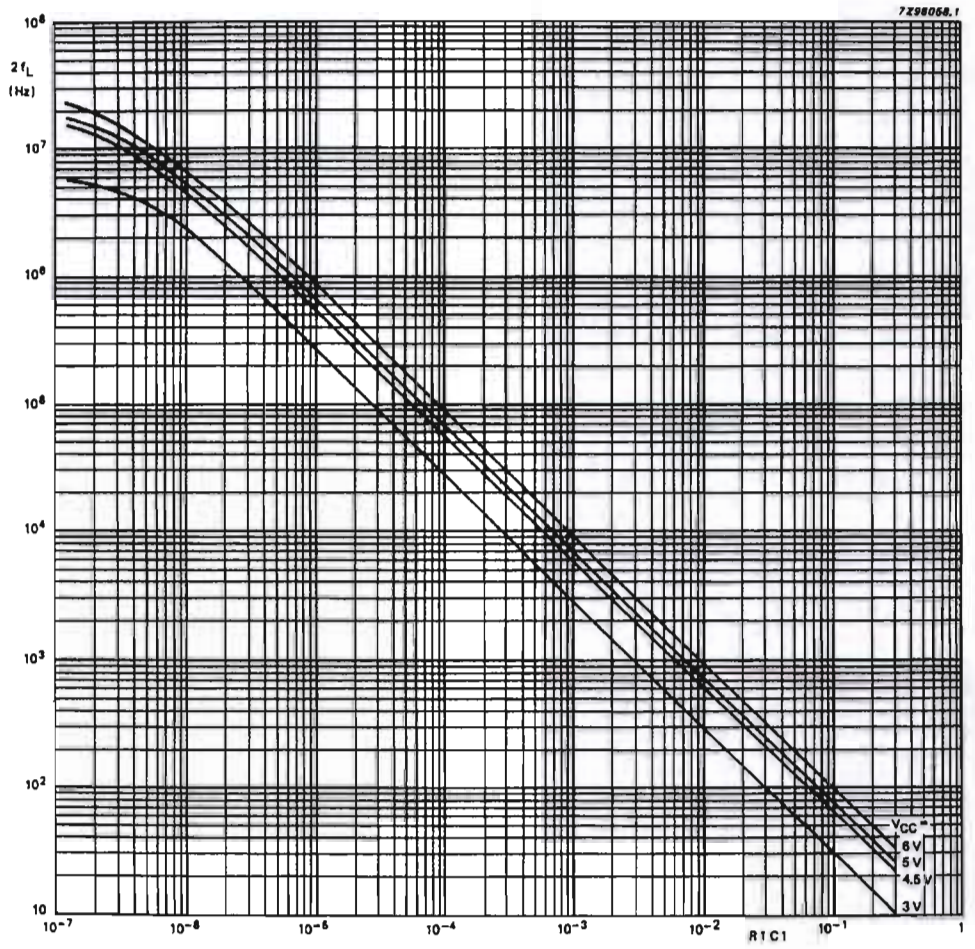


Fig.31 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to (V_{CC} – 0.9) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN}\ \text{range}} 2\pi\ (\text{r/s/V}).$$

PLL design example

The frequency synthesizer, used in the design example shown in Fig.32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : < 20%

The open-loop gain is
$H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
$K_o = K_v/s$ VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable). The values can be determined using the information in the section "DESIGN CONSIDERATIONS". With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} =$$

$$= \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/V$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}.$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:
$1 + H(s) \times G(s) = 0$.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ζ is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}$$

In Fig.33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. From Fig.33 it can be seen that the damping ratio ζ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms.
This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

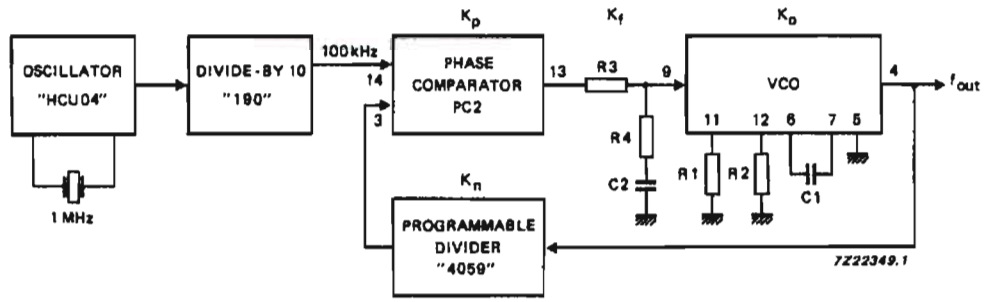


Fig.32 Frequency synthesizer.

note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

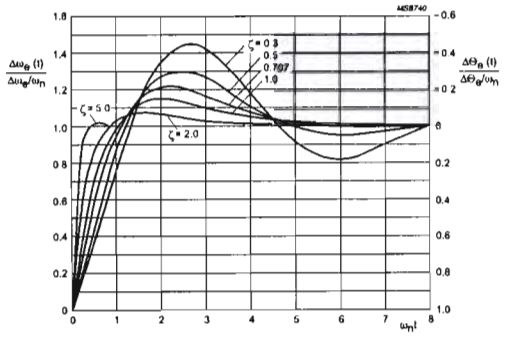


Fig.33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

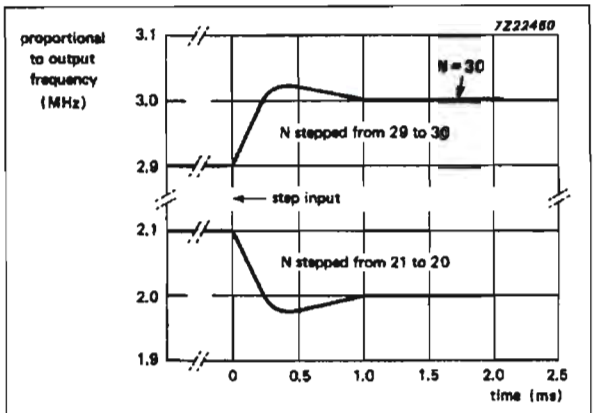


Fig.34 Frequency compared to the time response.

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

Even with these conditions:

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4526B
MSI
Programmable 4-bit binary down counter

Product specification
File under Integrated Circuits, IC04

January 1995

Programmable 4-bit binary down counter

HEF4526B MSI

DESCRIPTION

The HEF4526B is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input (CP_0, $\overline{CP}_1$), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and $\overline{CP}_1$ are LOW, the counter advances on a LOW to HIGH transition of CP_0. When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP}_1$. TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3$ = LOW) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

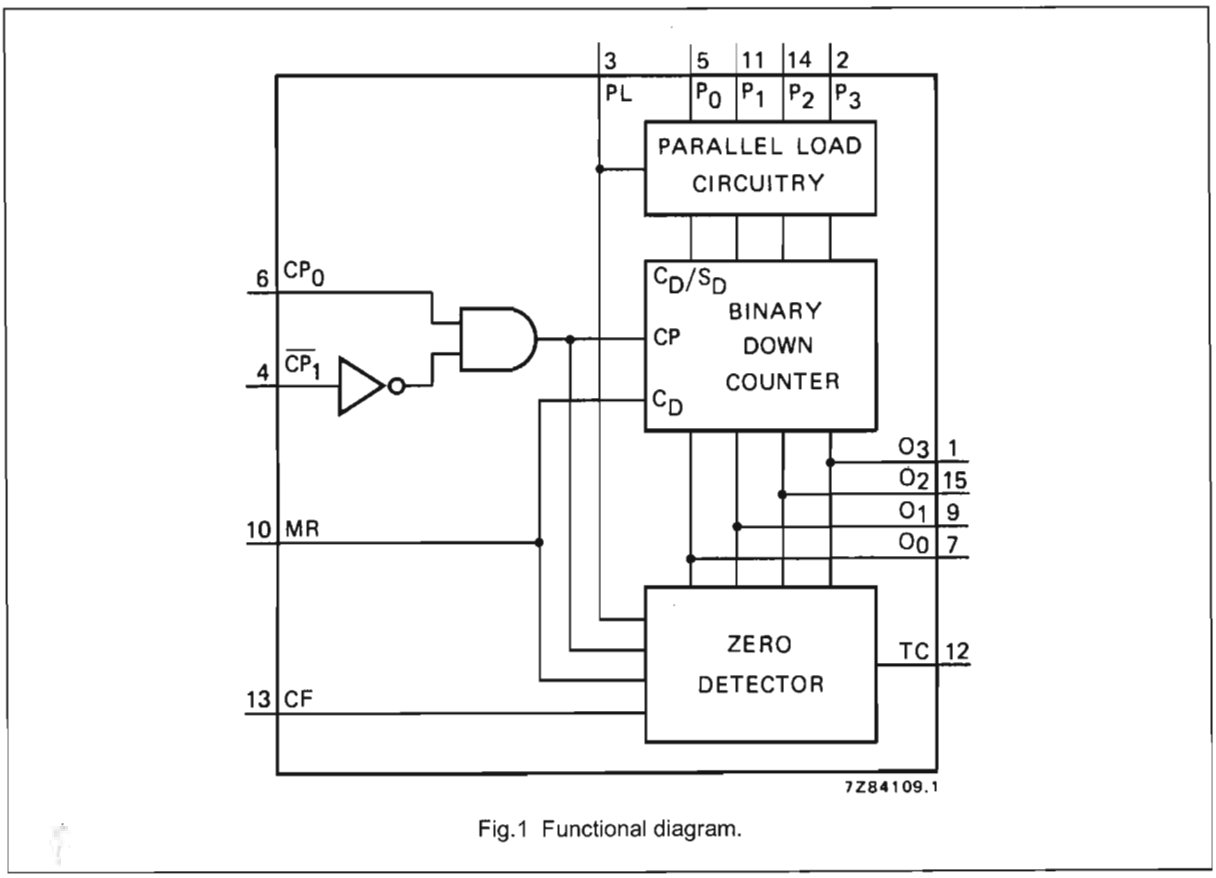


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Programmable 4-bit binary down counter

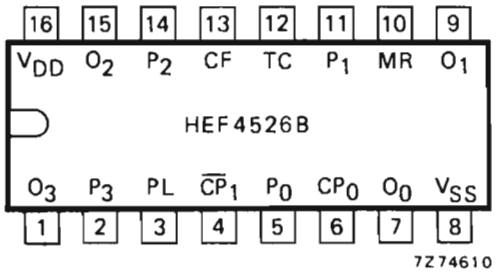


Fig.2 Pinning diagram.

HEF4526BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4526BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4526BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

PL	parallel load input
P_0 to P_3	parallel inputs
CF	cascade feedback input
CP_0	clock input (LOW to HIGH, triggered)
$\overline{CP}_1$	clock input (HIGH to LOW, triggered)
MR	asynchronous master reset input
TC	terminal count output
O_0 to O_3	buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

COUNT	OUTPUTS			
	O_3	O_2	O_1	O_0
15	H	H	H	H
14	H	H	H	L
13	H	H	L	H
12	H	H	L	L
11	H	L	H	H
10	H	L	H	L
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

FUNCTION TABLE

MR	PL	CP_0	$\overline{CP}_1$	MODE
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	↑	H	no change
L	L	L	↓	no change
L	L	↓	X	no change
L	L	X	↑	no change
L	L	↑	L	counter advances
L	L	H	↓	counter advances

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ↑ = positive-going transition
   ↓ = negative-going transition

SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH; $\overline{CP}_1$ = LOW

PL	P_3	P_2	P_1	P_0	DIVIDE BY	TC OUTPUT PULSE WIDTH
L	X	X	X	X	16	one clock period
TC	H	H	H	H	15	clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	

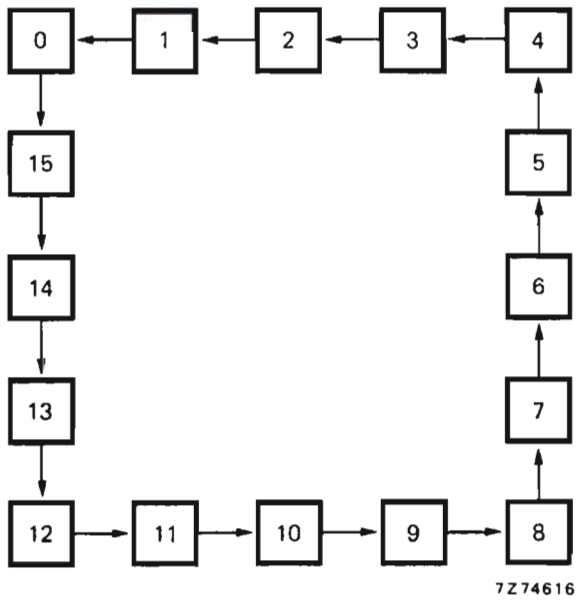


Fig.3 State diagram.

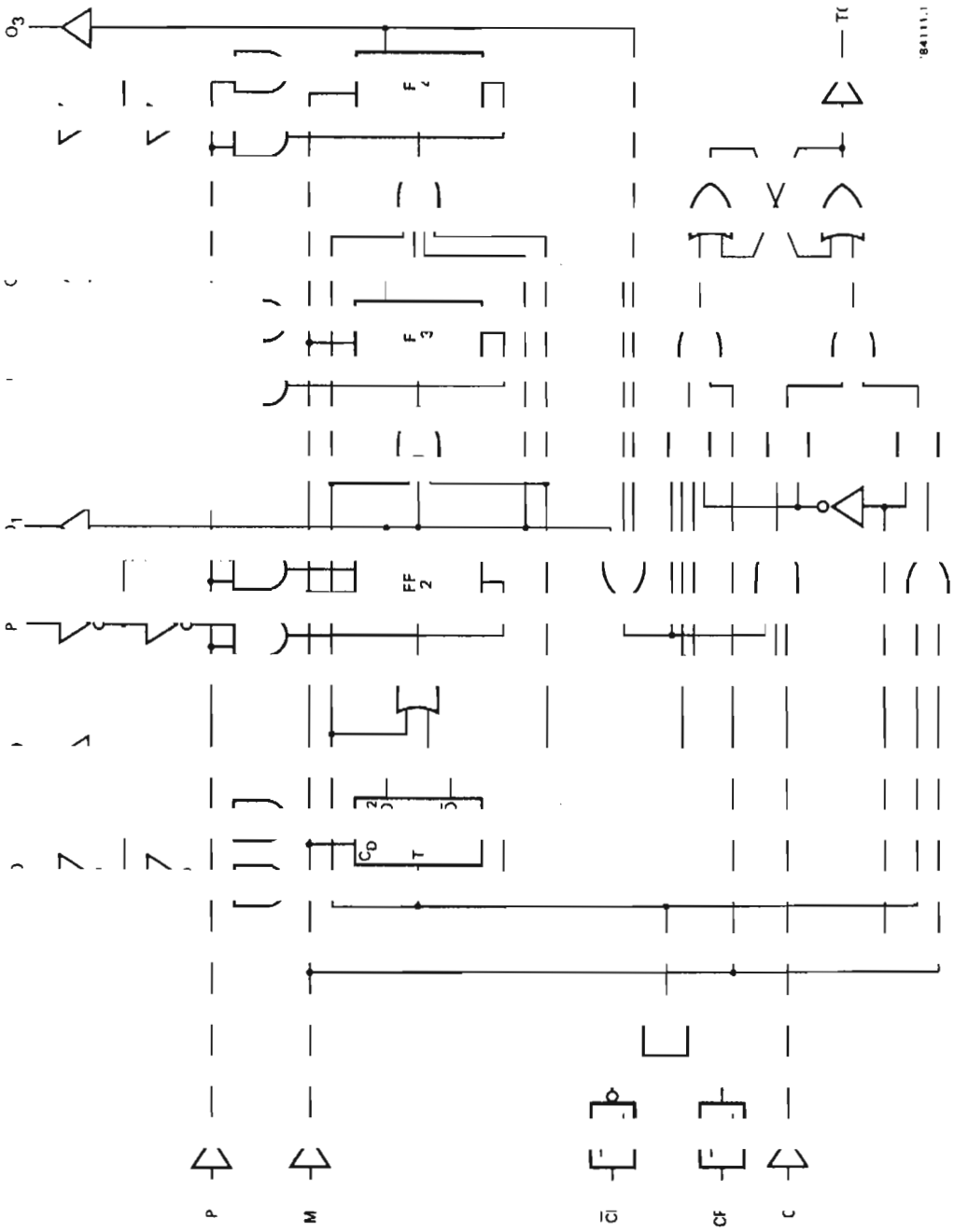


Fig.4 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma\ (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	
	15	$10\ 000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CP_0, $\overline{CP}_1 \rightarrow O_n$	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1 \rightarrow TC$	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
$PL \rightarrow O_n$	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Minimum clock	5			80	40	ns	see also waveforms Figs 5 and 6
pulse width CP_0	10	t_{WCPL}		40	20	ns	
LOW	15			30	15	ns	
Minimum clock	5			80	40	ns	
pulse width $\overline{CP}_1$	10	t_{WCPH}		40	20	ns	
HIGH	15			30	15	ns	
Minimum PL	5			100	50	ns	
pulse width; HIGH	10	t_{WPLH}		40	20	ns	
	15			32	16	ns	
Minimum MR	5			130	65	ns	
pulse width; HIGH	10	t_{WMRH}		50	25	ns	
	15			40	20	ns	
Hold time	5			30	5	ns	
$P_n \rightarrow PL$	10	t_{hold}		20	5	ns	
	15			15	5	ns	
Set-up time	5			30	0	ns	
$P_n \rightarrow PL$	10	t_{su}		20	0	ns	
	15			15	0	ns	
Maximum clock	5			6	12	MHz	see note 1
pulse frequency	10	f_{max}		12	25	MHz	
PL = LOW	15			16	32	MHz	

Note

1. In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.

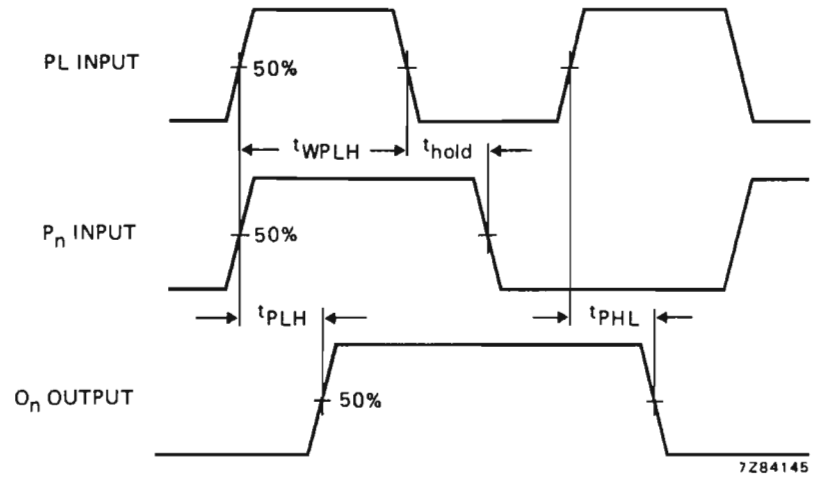


Fig.5 Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n.

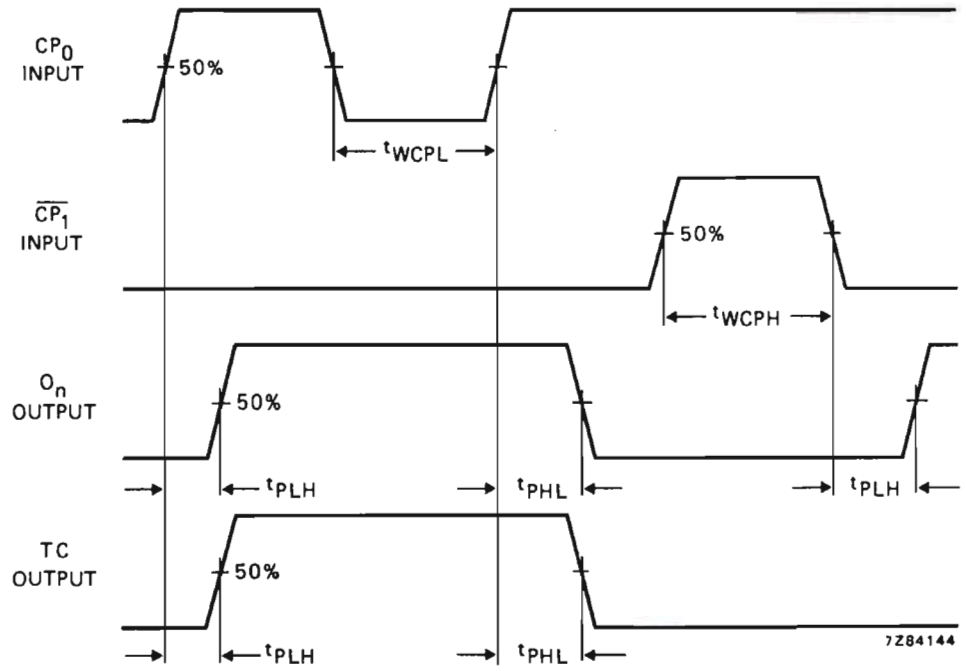
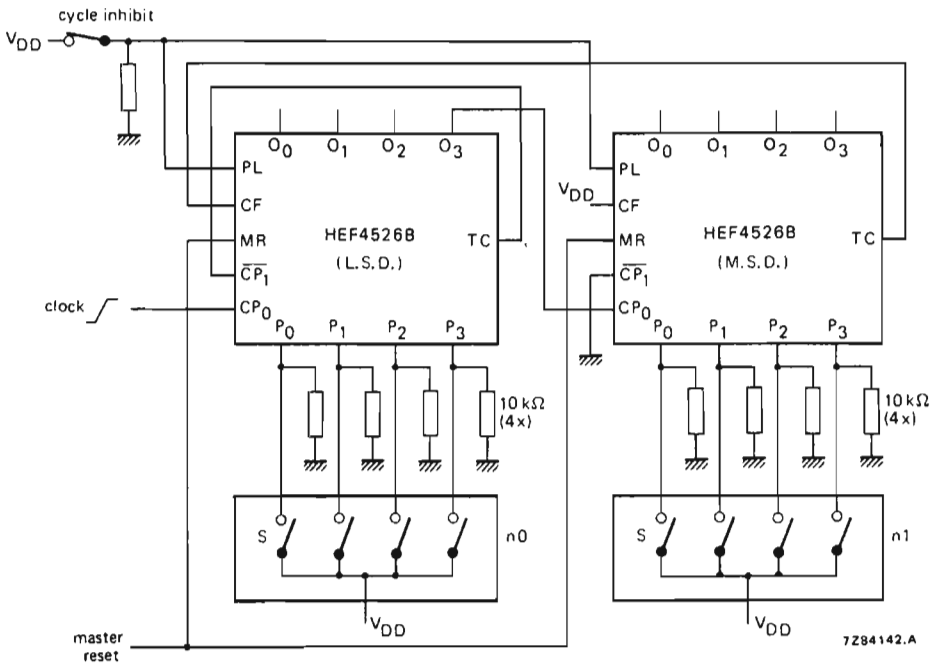


Fig.6 Waveforms showing minimum CP_0 and $\overline{CP_1}$ pulse widths, propagation delays for CP_0, $\overline{CP_1}$ to O_n and TC.

APPLICATION INFORMATION

Some examples of applications for the HEF4526B are:

- Divide-by-n counter
- Programmable frequency divider



Counting cycle:

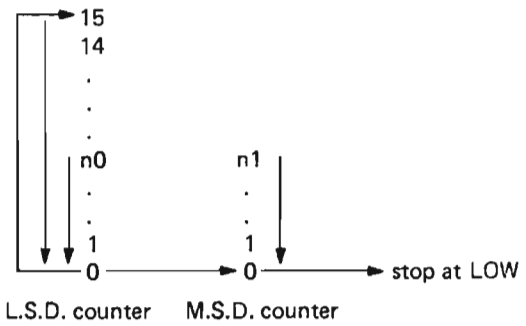
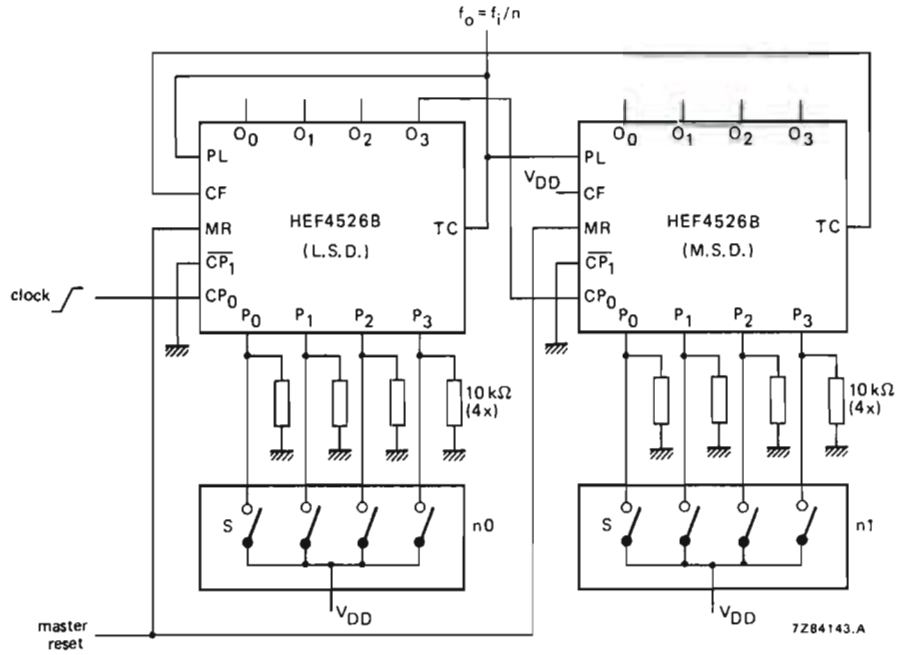


Fig.7 Typical application of two HEF4526B circuits in a 2-stage programmable down counter (one cycle). S are thumbwheel switches; when open: LOW state.



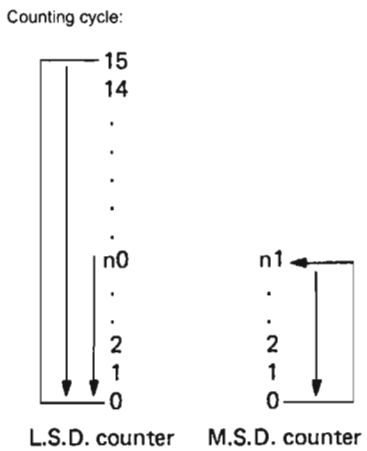


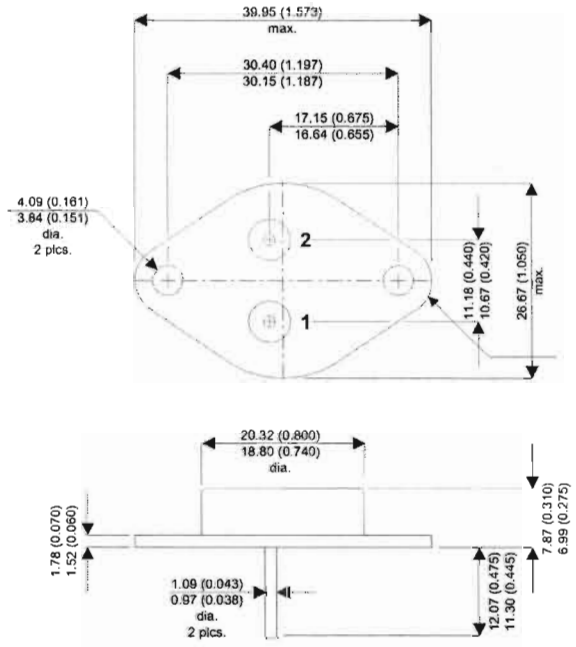
Fig.8 Typical application of two HEF4526B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

SEME LAB

IRF140

MECHANICAL DATA

Dimensions in mm (inches)



TO–3 Metal Package

Pin 1 – Gate Pin 2 – Source Case – Drain

N–CHANNEL POWER MOSFET

V_{DSS}	100V
$I_{D(cont)}$	28A
$R_{DS(on)}$	0.077Ω

FEATURES

- HERMETICALLY SEALED TO–3 METAL PACKAGE
- SIMPLE DRIVE REQUIREMENTS
- SCREENING OPTIONS AVAILABLE

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V_{GS}	Gate – Source Voltage		±20V
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 25°C)	28A
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 100°C)	20A
I_{DM}	Pulsed Drain Current [1]		112A
P_D	Power Dissipation @ T_{case} = 25°C		125W
	Linear Derating Factor		1W/°C
E_{AS}	Single Pulse Avalanche Energy [2]		250mJ
I_{AR}	Avalanche Current [2]		28A
E_{AR}	Repetitive Avalanche Energy [2]		12.5mJ
dv/dt	Peak Diode Recovery [3]		5.5V/ns
T_J , T_{stg}	Operating and Storage Temperature Range		-55 to +150°C
T_L	Lead Temperature 1.6mm (0.63") from case for 10 sec.		300°C

Notes

1) Pulse Test: Pulse Width ≤ 300μs, δ ≤ 2%
2) @ V_{DD} = 25V , L ≥ 480μH , R_G = 25Ω , Peak I_L = 28A , Starting T_J = 25°C
3) @ I_{SD} ≤ 28A , di/dt ≤ 170A/μs , V_{DD} ≤ BV_{DSS} , T_J ≤ 150°C , Suggested R_G = 9.1Ω

Semelab plc. Telephone (01455) 556565. Telex: 341927. Fax (01455) 552612.

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	STATIC ELECTRICAL RATINGS					
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0 I_D = 1mA	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Temperature Coefficient of Breakdown Voltage	Reference to 25°C I_D = 1mA		0.13		V/°C
$R_{DS(on)}$	Static Drain – Source On–State Resistance [1]	V_{GS} = 10V I_D = 20A			0.077	Ω
		V_{GS} = 10V I_D = 28A			0.089	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250mA	2		4	V
g_{fs}	Forward Transconductance [1]	V_{DS} ≥ 15V I_{DS} = 20A	9.1			S (℧)
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V_{DS} = 0.8BV_{DSS}			25	µA
		T_J = 125°C			250	
I_{GSS}	Forward Gate – Source Leakage	V_{GS} = 20V			100	nA
I_{GSS}	Reverse Gate – Source Leakage	V_{GS} = –20V			–100	
	DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance	V_{GS} = 0		1660		pF
C_{oss}	Output Capacitance	V_{DS} = 25V		550		
C_{rss}	Reverse Transfer Capacitance	f = 1MHz		120		
Q_g	Total Gate Charge	V_{GS} = 10V	30		59	nC
Q_{gs}	Gate – Source Charge	I_D = 28A	2.4		12	
Q_{gd}	Gate – Drain ("Miller") Charge	V_{DS} = 0.5BV_{DSS}	12		30.7	
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 50V			21	ns
t_r	Rise Time	I_D = 28A			145	
$t_{d(off)}$	Turn–Off Delay Time	R_G = 9.1Ω			21	
t_f	Fall Time				105	
	SOURCE – DRAIN DIODE CHARACTERISTICS					
I_S	Continuous Source Current				28	A
I_{SM}	Pulse Source Current [2]				112	
V_{SD}	Diode Forward Voltage [1]	I_S = 28A T_J = 25°C V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_F = 28A T_J = 25°C			400	ns
Q_{rr}	Reverse Recovery Charge [1]	d_i / d_t ≤ 100A/µs V_{DD} ≤ 50V			2.9	µC
t_{on}	Forward Turn–On Time			Negligible		
	PACKAGE CHARACTERISTICS					
L_D	Internal Drain Inductance (measured from 6mm down drain lead to centre of die)			5.0		nH
L_S	Internal Source Inductance (from 6mm down source lead to source bond pad)			13		
	THERMAL CHARACTERISTICS					
$R_{\theta JC}$	Thermal Resistance Junction – Case				1.67	°C/W
$R_{\theta CS}$	Thermal Resistance Case – Sink			0.12		
$R_{\theta JA}$	Thermal Resistance Junction – Ambient				30	

Notes

1) Pulse Test: Pulse Width ≤ 300ms, δ ≤ 2%
2) Repetitive Rating – Pulse width limited by maximum junction temperature.

INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40106B gates
Hex inverting Schmitt trigger

Product specification
File under Integrated Circuits, IC04

January 1995

DESCRIPTION

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H).

This device may be used for enhanced noise immunity or to "square up" slowly changing waveforms.

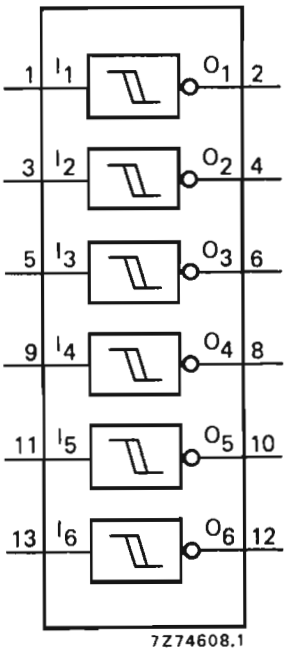


Fig.1 Functional diagram.

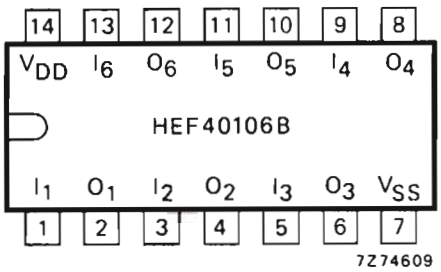


Fig.2 Pinning diagram.

HEF40106BP(N): 14-lead DIL; plastic (SOT27-1)
HEF40106BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF40106BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

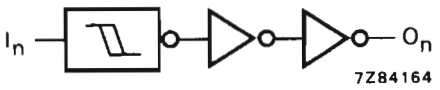


Fig.3 Logic diagram (one inverter).

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Hysteresis	5		0,5	0,8		V
voltage	10	V_H	0,7	1,3		V
	15		0,9	1,8		V
Switching levels	5		2	3,0	3,5	V
positive-going	10	V_P	3,7	5,8	7	V
input voltage	15		4,9	8,3	11	V
negative-going	5		1,5	2,2	3	V
input voltage	10	V_N	3	4,5	6,3	V
	15		4	6,5	10,1	V

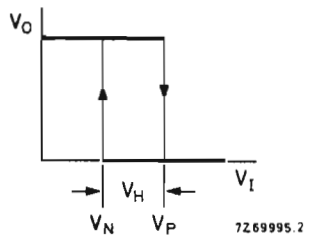


Fig.4 Transfer characteristic.

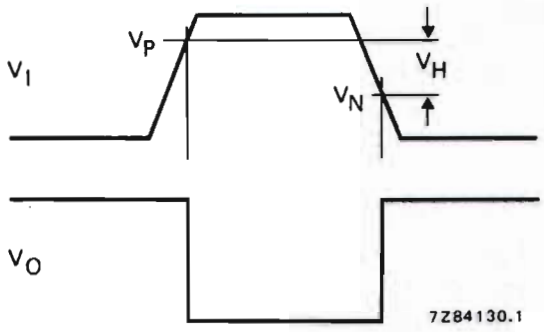


Fig.5 Waveforms showing definition of V_P, V_N and V_H, where V_N and V_P are between limits of 30% and 70%.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n$	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF)
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	2 300 f_i + Σ ($f_o C_L$) × V_{DD}^2	where
dissipation per	10	9 000 f_i + Σ ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz)
package (P)	15	20 000 f_i + Σ ($f_o C_L$) × V_{DD}^2	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			Σ ($f_o C_L$) = sum of outputs
			V_{DD} = supply voltage (V)

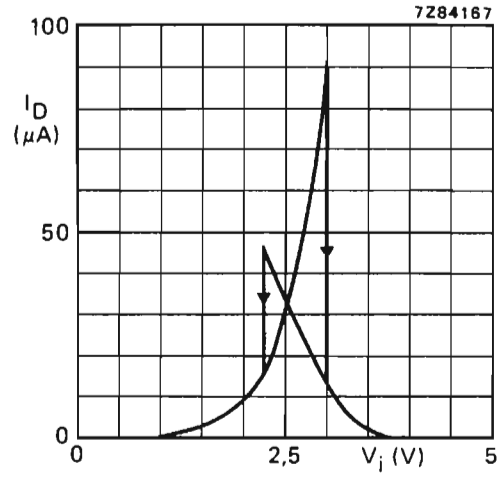


Fig.6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

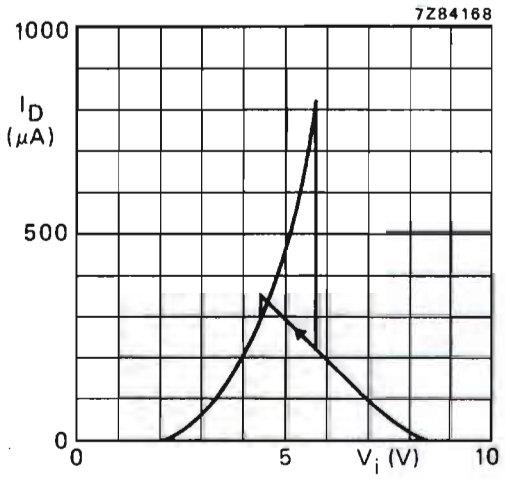


Fig.7 Typical drain current as a function of input voltage; V_{DD} =10 V; T_{amb} = 25 °C.

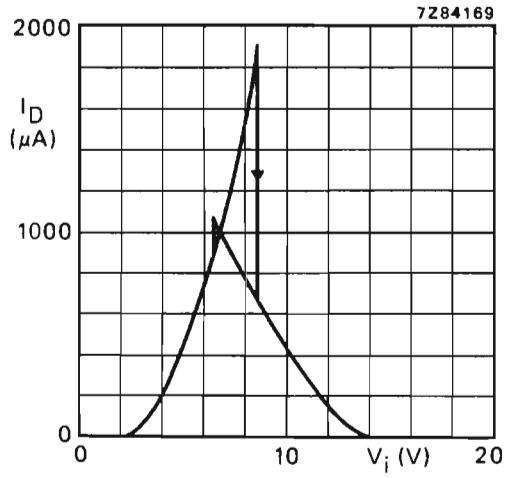


Fig.8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

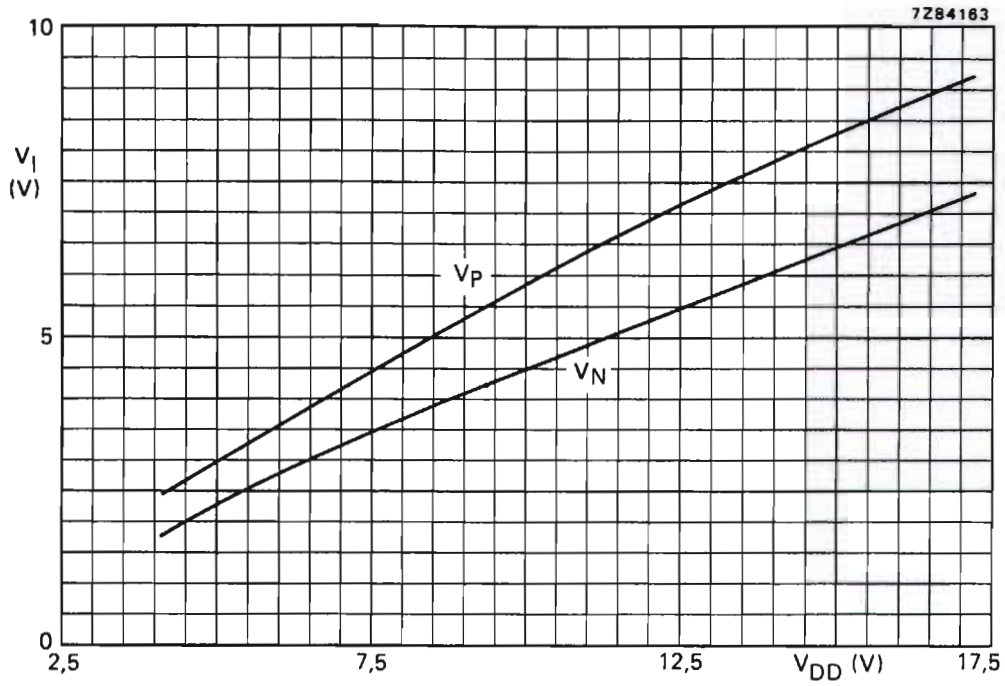


Fig.9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

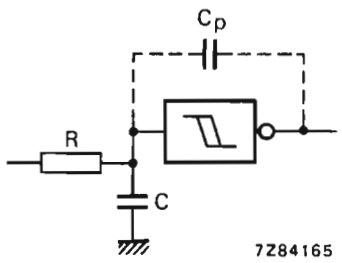


Fig.10 Schmitt trigger driven via a high impedance (R > 1 kΩ).

If a Schmitt trigger is driven via a high impedance (R > 1 kΩ) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

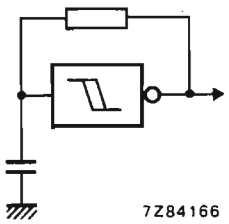
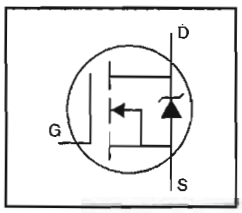


Fig.11 The HEF40106B used as an astable multivibrator.

IOR Rectifier IRF610

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 200V

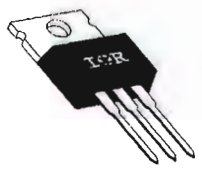
$R_{DS(on)}$ = 1.5Ω

I_D = 3.3A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	3.3	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	2.1	
I_{DM}	Pulsed Drain Current ①	10	
P_D @ T_C = 25°C	Power Dissipation	36	W
	Linear Derating Factor	0.29	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	64	mJ
I_{AR}	Avalanche Current ①	3.3	A
E_{AR}	Repetitive Avalanche Energy ①	3.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS}=0V, I_D= 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V_{GS}=10V, I_D=2.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250µA
g_{fs}	Forward Transconductance	0.80	—	—	S	V_{DS}=50V, I_D=2.0A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS}=200V, V_{GS}=0V
		—	—	250		V_{DS}=160V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	8.2	nC	I_D=3.3A
Q_{gs}	Gate-to-Source Charge	—	—	1.8		V_{DS}=160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.5		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	V_{DD}=100V
t_r	Rise Time	—	17	—		I_D=3.3A
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		R_G=24Ω
t_f	Fall Time	—	8.9	—		R_D=30Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	140	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	53	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	10		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=3.3A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	150	310	ns	T_J=25°C, I_F=3.3A
Q_{rr}	Reverse Recovery Charge	—	0.60	1.4	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=8.8mH R_G=25Ω, I_{AS}=3.3A (See Figure 12)

③ I_{SD}≤3.3A, di/dt≤70A/µs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

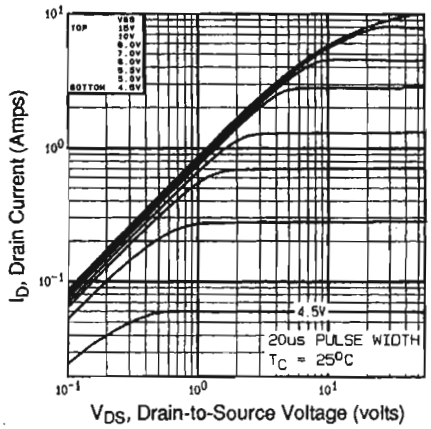


Fig 1. Typical Output Characteristics, T_C=25°C

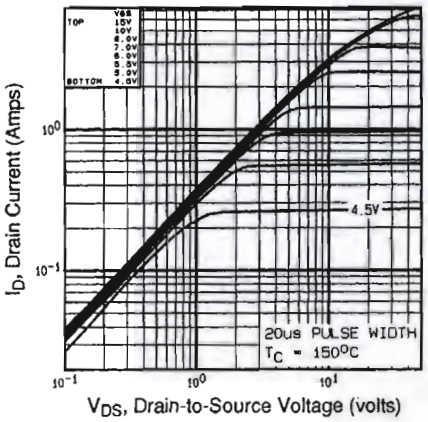


Fig 2. Typical Output Characteristics, T_C=150°C

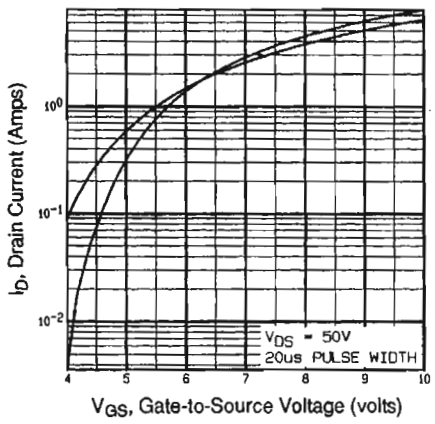


Fig 3. Typical Transfer Characteristics

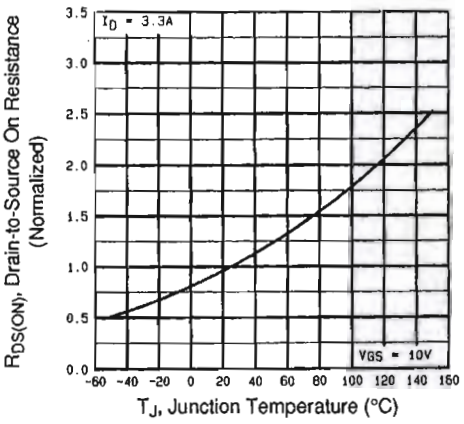


Fig 4. Normalized On-Resisance Vs. Temperature

DATA SHEETS

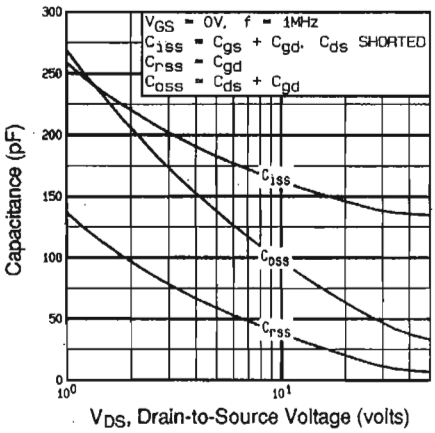


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

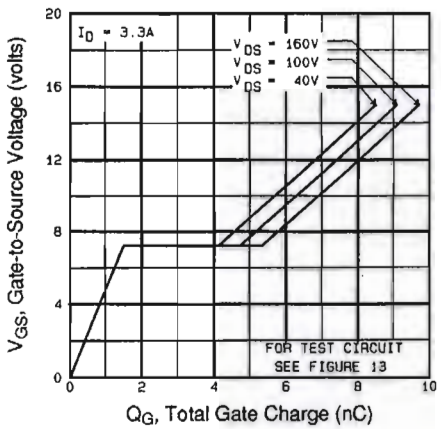


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

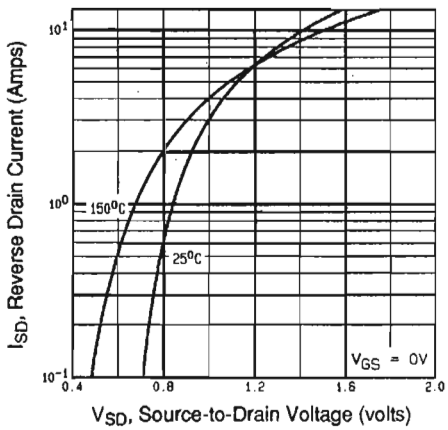


Fig 7. Typical Source-Drain Diode Forward Voltage

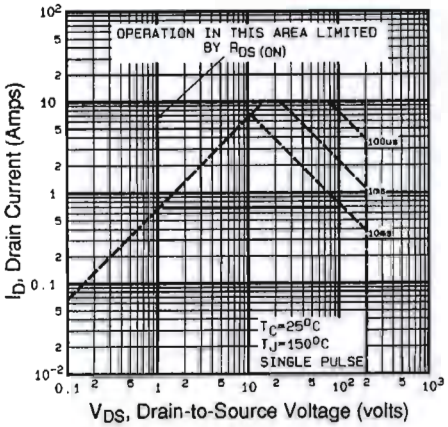


Fig 8. Maximum Safe Operating Area

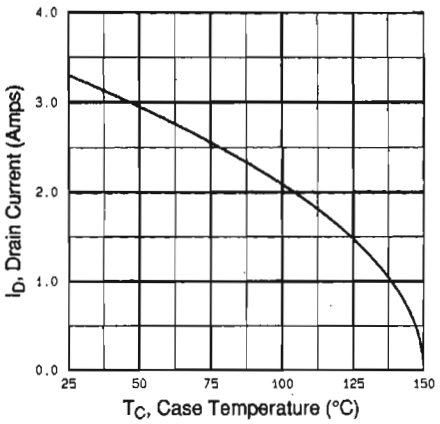


Fig 9. Maximum Drain Current Vs. Case Temperature

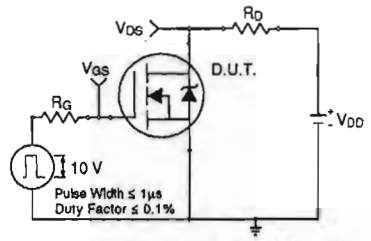


Fig 10a. Switching Time Test Circuit

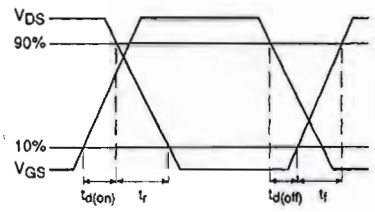


Fig 10b. Switching Time Waveforms

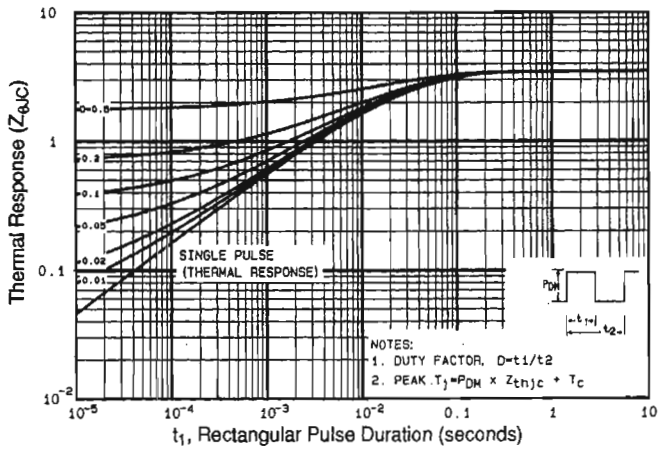


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

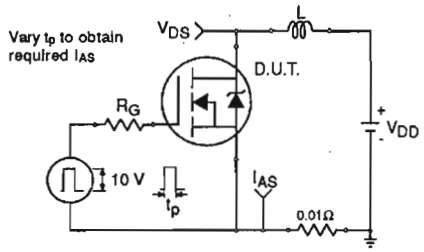


Fig 12a. Unclamped Inductive Test Circuit

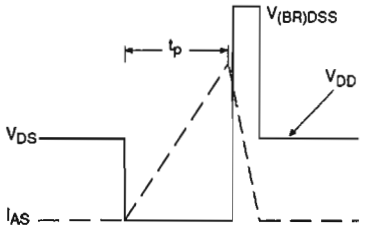


Fig 12b. Unclamped Inductive Waveforms

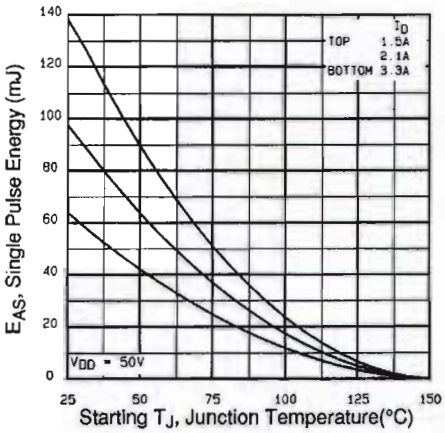


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

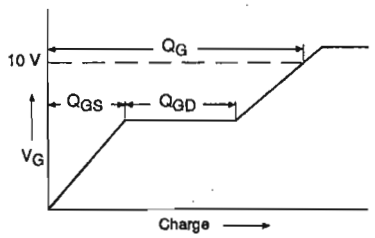


Fig 13a. Basic Gate Charge Waveform

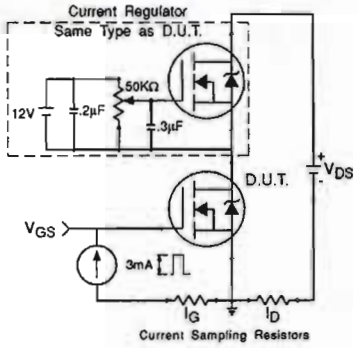


Fig 13b. Gate Charge Test Circuit

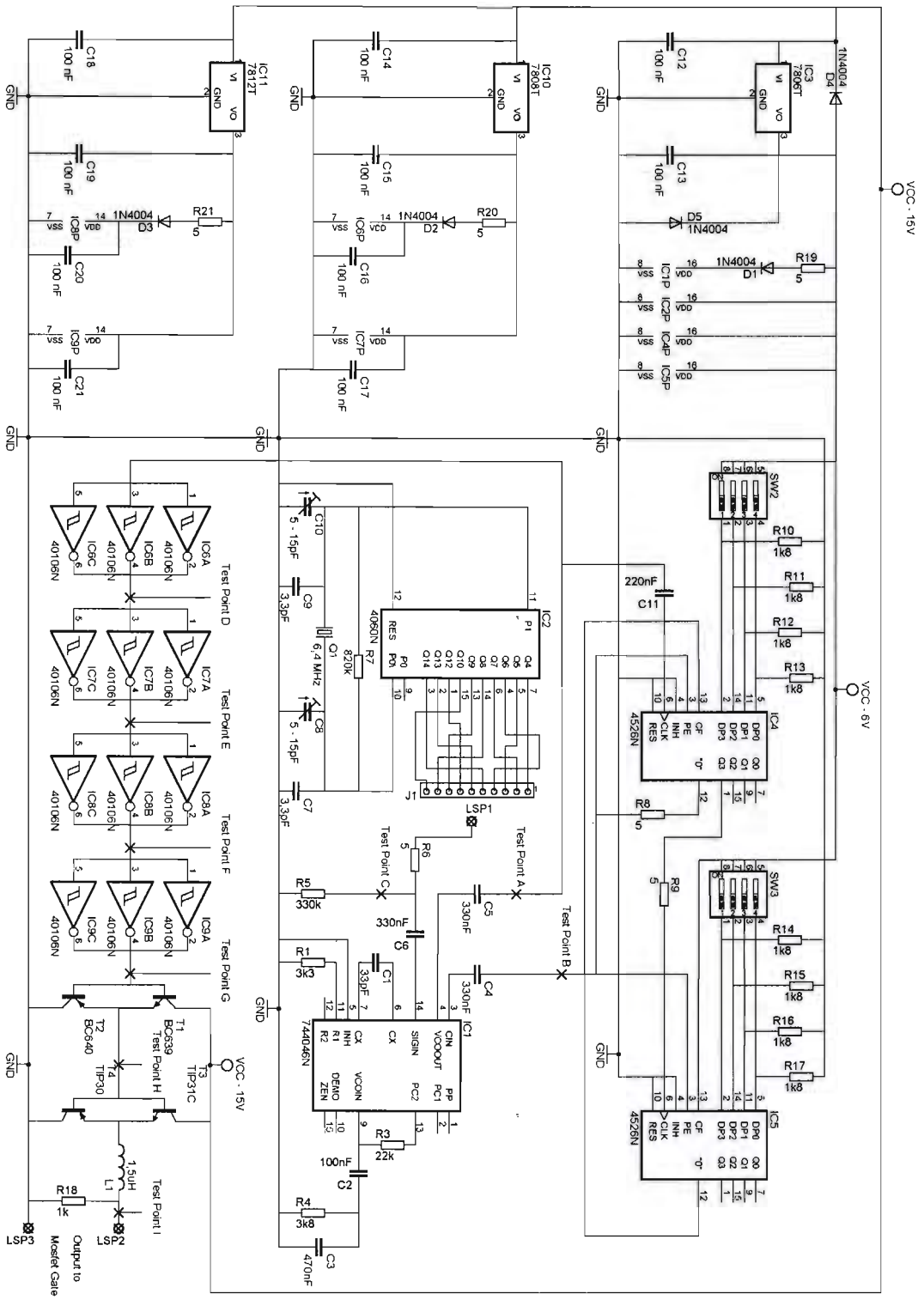
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International IOR Rectifier


VCC - 15V
VCC - 6V
GND
IC11 7812T
IC10 7808T
IC3 7806T
1N4004 D4
D5 1N4004
1N4004 D1
1N4004 D2
1N4004 D3
R19 5
R20 5
R21 5
C12 100 nF
C13 100 nF
C14 100 nF
C15 100 nF
C16 100 nF
C17 100 nF
C18 100 nF
C19 100 nF
C20 100 nF
C21 100 nF
IC1P
IC2P
IC4P
IC5P
IC6P
IC7P
IC8P
IC9P
SW2
SW3
R10 1k8
R11 1k8
R12 1k8
R13 1k8
R14 1k8
R15 1k8
R16 1k8
R17 1k8
220nF C11
IC4 4526N
IC5 4526N
R8 5
R9 5
IC2 4060N
C10 5 - 15pF
C9 3,3pF
Q1 6,4 MHz
R7 820k
C8 5 - 15pF
C7 3,3pF
J1
LSP1
IC1 74HC4046N
R1 3k3
C1 33pF
R5 330k
R6 5
C5 330nF
C6 330nF
C4 330nF
R3 22k
C2 100nF
R4 3k8
C3 470nF
IC6A 40106N
IC6B 40106N
IC6C 40106N
IC7A 40106N
IC7B 40106N
IC7C 40106N
IC8A 40106N
IC8B 40106N
IC8C 40106N
IC9A 40106N
IC9B 40106N
IC9C 40106N
Test Point A
Test Point B
Test Point C
Test Point D
Test Point E
Test Point F
Test Point G
Test Point H
Test Point I
T1 BC639
T2 BC640
T3 TIP31C
T4 TIP30
L1 1,5uH
R18 1k
LSP2
LSP3
Output to Mosfet Gate