# Design and development of a 200 W converter for phosphoric acid fuel cells

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## Declaration

I, Christian Kinsala Kuyula hereby declare that the following research information is my own work. This is submitted in fulfilment of the requirements for the Magister Technologiae: Engineering: Electrical to the Department of Electronic Engineering at the Vaal University of Technology, Vanderbijlpark. This dissertation has never before been submitted for evaluation to any educational institution.

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04 March 2013

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## Dedication

This dissertation is dedicated to my parents, Marc and Lucie, and my beloved wife, Nina, for their support and encouragement.

## Abstract

“If we think oil is a problem now, just wait 20 years. It’ll be a nightmare.” — Jeremy Rifkin, Foundation of Economic Trends, Washington, D.C., August 2003. This statement harmonises with the reality that human civilisation faces today. As a result, humankind has been forced to look for alternatives to fossil fuels. Among possible solutions, fuel cell (FC) technology has received a lot of attention because of its potential to generate clean energy.

Fuel cells have the advantage that they can be used in remote telecommunication sites with no grid connectivity as the majority of telecommunication equipment operates from a DC voltage supply. Power plants based on phosphoric acid fuel cell (PAFC) have been installed worldwide supplying urban areas, shopping centres and medical facilities with electricity, heat and hot water. Although these are facts regarding large scale power plants for on-site use, portable units have been explored as well. Like any other fuel cell, the PAFC output power is highly unregulated leading to a drastic drop in the output voltage with changing load value. Therefore, various DC–DC converter topologies with a wide range of input voltages can be used to regulate the fuel cell voltage to a required DC load.

An interleaved synchronous buck converter intended for efficiently stepping down the energy generated by a PAFC was designed and developed. The design is based on the National Semiconductor LM5119 IC. A LM5119 evaluation board was redesigned to meet the requirements for the application. The measurements were performed and it was found that the converter achieved the expectations. The results showed that the converter efficiently stepped down a wide range of input voltages (22 to 46 V) to a regulated 13.8 V while achieving a 93 percent efficiency. The conclusions reached and recommendations for future research are presented.

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# Glossary of abbreviations and symbols

**A**

A – Amperes

AC – Alternating current

AFC – Alkaline fuel cell

**C**

CCM – Continuous current mode

**D**

DC – Direct current

DCM – Discontinuous current mode

DEM – Diode emulation mode

DMFC – Direct methanol fuel cell

**E**

EMI – Electromagnetic interference

**F**

FC – Fuel cell

**G**

GND – ground

**H**

H – Hydrogen gas molecule

HF – High frequency

$HO_2$ – Water

$H_3PO_4$ – Phosphoric acid

**I**

IGBT – Insulated-gate bipolar transistor

IC – Integrated circuit

**K**

kHz – Kilo hertz being $10^3$

kW – Kilowatt

**L**

LDO – Low drop out

LLP – Leadless package

**M**

MCFC – Molten carbonate fuel cell

MHz – Mega hertz being $10^6$

MOSFET – Metal-oxide-semiconductor field-effect transistor

mV – Milli volt being $10^{-3}$

**N**

nC – Nano coulomb being $10^{-9}$

**O**

$O_2$ – Oxygen

**P**

PAFC – Phosphoric Acid Fuel Cell

PCB – Printed circuit board

PEMFC– Proton Exchange Membrane Fuel Cell

Pt – Platinum

PTFE – Polyetrafluroethylene

PWM – Pulse width modulation

**R**

RFI – Radio frequency interference

**S**

s – Second

SMPS – Switch mode power supply

SOFC – Solid oxide fuel cell

SiC – Silicon carbide

**U**

µs – Micro second being $10^{-6}$

UVLO – Under voltage lockout

**V**

V – Volt

Vgs – The gate to source voltage

Vref – Reference voltage

**W**

W – Watt

**X ,Y,Z**

ZVS – Zero voltage switching

# Chapter 1 Introduction

## 1.1 Background

"If we think oil is a problem now, just wait 20 years. It'll be a nightmare." — Jeremy Rifkin, Foundation of Economic Trends, Washington, D.C., August 2003. This statement harmonises with the reality that human civilization faces today. As a result, humankind has been forced to look for different resources other than fossil fuels. Alternative energy sources such as fuel cells (FCs) have received a lot of attention because they are a potential technology for generating clean energy (Pareta, Choudhury, Somaiah, Rangarajan, Matre & Palande 2011:14772).

A FC is an electrochemical device in which the energy of a chemical reaction is converted directly into electricity. Compared to a battery, a FC works as long as a fuel and an oxidant are supplied continuously from outside the cell (Redmond 2007). There are several different types of FCs, each using a different chemistry. FCs are usually classified according to their operating temperature and the type of electrolyte they use. Applications for FC systems spread from residential applications, uninterruptible power supplies (in houses, industries and remote locations) to automotive applications (Chakraborty 2011:1823).

The main types of FCs are:

- Phosphoric Acid Fuel Cell (PAFC);
- Proton-Exchange Membrane Fuel Cell (PEMFC);
- Molten Carbonate Fuel Cell (MCFC);
- Solid Oxide Fuel Cell (SOFC);
- Direct Methanol Fuel Cell (DMFC); and
- Alkaline Fuel Cell (AFC).

Closely associated to FCs are power electronics modules. Because FCs are used where efficiency is crucial, these modules help in the energy conversion by

improving the efficiency of power utilisation (Bose 2006:4). Thus power conversion is fundamental to FC systems. The operating FC voltage can be stepped down or stepped up. In order to control and shift the FC voltage to a required voltage level, voltage regulators, DC–DC converters and chopper circuits may be used. A range of DC–DC switch-mode converters are used depending on the application. They achieve voltage regulation by varying the ON–OFF ratio or time duty ratio of the switching element. The main types of electronic switches used in modern power electronic equipment are the MOSFET and IGBT. There are two main applications for DC–DC converters in FC systems. One is to provide DC isolation. This type often requires the use of an isolating transformer. The other application is to transfer power from a fixed DC supply, which may be inverted into AC (Cheng, Sutanto, Ho & Law 2001:2201).

Since most telecommunication equipment operates from a DC voltage supply, the most convenient power electronics interface is a DC–DC converter. Decades ago, all equipment was located in a central office and grid supply was all that they needed. Most recently, owing to new telecommunication networks, new challenges have come to the fore. Telecommunication equipment is being located closer to customers organised in diverse networks (Ribero, Cardoso, Boccaletti & Mendes 2009:433-438). However, some areas where this equipment is located lack a proper AC grid especially in remote areas.

Always situated at a distance from any form of grid power or energy supply, remote telecommunication sites' greatest expenditure and largest problem are the supply of energy for electrical devices housed in them. This leads to reliance on small-to-medium-sized generation plants with or without backup batteries, supplying local demand (Swanepoel 2005:1). According to Joubert (2005:1) these small-to-medium-sized generation plants may comprise electrical sources such as fuel cells, batteries, photovoltaic cells, windmill power, hydro-power, bio-energy, generators, devices using heat to generate electricity and the utilisation of storage devices such as super capacitors and ultra capacitors. Some of these technologies are the object of extensive research at the Telkom Centre of Excellence at the Vaal University of

Technology in order to provide solutions for the telecommunication industry in terms of backup power systems and rural power generation plants.

Another big area where the role of power electronics finds importance is when connected to a FC system. In general most common energy storage devices such as batteries, capacitors and ultra-capacitors are needed at various stages either to supply auxiliaries or to improve the slow transient response of the FC used, with a power electronic interface. When series of battery packs are placed across the FC stack, they require an additional circuitry for regulating the DC bus voltage. Although costly, this setup ensures a safe operation of the battery packs (Chakraborty 2011:1824).

In these kind of systems, the FC operates more or less continuously at the average power. When the total system power requirements are low, the surplus electrical energy is stored in a rechargeable battery or capacitor. In the case that power demand exceeds the amount that can be provided by the FC, the energy is drawn from the storage device. It stands to reason that the power requirements are quite variable. Such a situation can happen with data transmitters and certain types of telecommunications equipment where for fairly long periods the device is in 'standby' mode and the FC will be recharging the battery. During transmission periods, the battery supplies most of the power (Larminie & Dicks 2003:362-363).

## 1.2 Phosphoric acid fuel cell and power conditioning

According to Sammes, Bove and Stahl (2004:372), the PAFC is a widely used and well documented type of FC. It is used in stationary power plants ranging from dispersed power to on-site generation plants. Power plants based on a PAFC stack have been installed worldwide supplying urban areas, shopping centres or medical facilities with electricity, heat and hot water. Although these are facts regarding large scale power plants for on-site use, portable units have been explored as well. A study by Sakai, Ito, Takesue, Tsutsumi, Nishizawa and Hamada (1992:49-52) from Sanyo Electric reported on a portable 250 W aircooled PAFC.

As the name implies, the PAFC uses phosphoric acid ($H_3PO_4$) as its electrolyte. The phosphoric acid used is in a highly concentrated form (95 percent or higher). The electrolyte is often immobilised in a porous silicon carbide (SiC) matrix by capillary action. A PAFC works with pure hydrogen or hydrogen rich gases as fuel and air is invariably used as the oxidant (Li 2006:264). PAFCs operate at temperatures between 150 - 220°C. The electro-catalyst in both the anode and cathode is made of platinum (Pt) or Pt alloys. The advantages of the PAFC are its simple construction, its stability both thermally, chemically and electrochemically. In addition, the use of concentrated acid (100%) minimizes the water vapour pressure so water management in the cell is not difficult. These factors probably assisted the earlier deployment into commercial systems compared to the other FC types (Carrette, Friedrich & Stimming 2001:15).

PAFC power generation makes intensive use of power electronics because a PAFC's output voltage is unstable. According to Bernay, Marchand and Cassir (2002: *Prospects of different fuel cell technologies for vehicle applications* as quoted by Sammes 2006:257) the cell voltage decreased from 0.82 V to 0.62 V as the current density increased from 10mA/cm$^2$ to 350mA/cm$^2$ for a PAFC. Similar variations in cell voltage with increasing operating current densities are reported for PEMFC, MCFC, SOFC, DMFC and protonic ceramic FCs. A single FC produces a very low voltage; therefore individual cells are usually piled in stacks as explained earlier. Even if multiple FCs are carefully stacked together in series, the voltage of the system will not be exactly what is desired for a given application. In other words, the electrical output power of a FC will not often be at a suitable voltage and certainly not at a constant voltage.

### 1.3 Problem statement

In order to efficiently regulate and stabilise the output voltage of a PAFC supplying power to remotely located telecommunication equipment, there is a need for a converter with the ability to handle a wide range of input voltages and then to

convert the unstable electrical power generated by a PAFC into usable power for telecommunication equipment operating on DC.

## 1.4 Methodology

The design and development of a converter for a PAFC will be addressed in the following manner. Firstly, an in depth literature study will be conducted on the PAFC and DC–DC converters for FCs. This will be followed by the design of a switched-mode converter utilizing pulse width modulation (PWM).

Once the various components of the converter have been designed, the converter will be constructed; operational tests and refinement of the design will be performed. Then the necessary experiments will be conducted on the PAFC's converter system. Finally, the conclusions and recommendations based upon the analysis of the results, will follow.

## 1.5 Delimitations

The design and development of a converter for PAFCs does not involve any construction of a PAFC or a controller of some sort to prevent overcharging of batteries and will be limited to 200 W.

## 1.6 Importance of the research

"The engagement of South Africa with the potential benefits of fuel cells is centered on the strategic use of the country's natural resources, including minerals, energy resources and technical skills", says the South African Agency for Science and Technology Advancement (SAASTA) science communication manager, Lorenzo Raynard (Burger 2012). Since the FC market in South Africa as well as the technical expertise on FC ancillary technologies are currently soaring, this research will address the need for a switched mode power converter providing usable DC current

from a PAFC in order to supply telecommunication equipment as it is fairly economical and suited for low power applications.

The study will also be of great benefit in the sense that it will constitute a building block for future research on the topic of power conversion for FCs at the Telkom Centre of Excellence.

## 1.7 Overview of the report

Chapter 2 consists of a literature review. After a brief review on PAFCs, key design considerations of DC–DC converters for FCs are presented as well as the different types of power electronic converters. Some 'conventional' and special switched-mode DC–DC converter topologies are also examined.

Chapter 3 deals with the practical design procedure and construction of the 200 W converter.

In Chapter 4, the experimental setup, measurements and results are presented.

Lastly, Chapter 5 contains the conclusions drawn; recommendations are made regarding the PAFC converter as well as suggestions for further improvements.

## 1.8 Summary

In this chapter the background for the design and development of a 200 W converter for PAFCs was presented as well as the methodology, relevance and importance of this research. The methodologies of the study along with its importance and relevance have been presented.

In the next chapter, a literature review on power converters for FCs is considered.

# Chapter 2 Literature review

## 2.1 Introduction

This chapter discusses theoretical considerations on the design of DC–DC converters for PAFCs as well as some converter topologies which can be used with FCs. Before delving into that, an explanation of the structure and working principle of a PAFC and its voltage-current (*V-I*) characteristics are examined in the following section.

## 2.2 Review on the PAFC

Considered the 'first generation' of modern fuel cells, PAFC technology has the most substantial record of operational experience. A photo of a stationary UTC PAFC is shown in Figure 1. PAFC systems produced by UTC Fuel Cells were the world's first commercially available FC product (King & Ishikawa 1996:86). It runs on hydrogen as the fuel and oxygen as the reducing agent. Hydrogen FCs provide a promising new method of power generation and energy storage for both mobility and stationary power applications (Dogterom & Kammerer 2005:401-405).


**Figure 1: UTC PC25 Stationary PAFC**

### 2.2.1 Structure and operation of a PAFC

As illustrated in Figure 2, a phosphoric acid cell is composed of two porous gas diffusion electrodes, namely, the anode and cathode placed side by side against a porous electrolyte matrix. The electrolyte matrix used here is silicon carbide (SiC). The gas diffusion electrodes are porous substrates that face the gaseous feed. On the other side of this substrate, which faces the phosphoric acid electrolyte, a fine platinised carbon powder electrocatalyst is roll-coated with polytetrafluroethylene (PTFE) as a binder. PTFE also acts as a hydrophobic agent to prevent flooding of pores so that reactant gas can easily diffuse to the reaction site. At the anode, hydrogen ionises to H+ and migrates towards the cathode to combine with oxygen, forming water vapour. The steam then comes out to the oxygen stream. An electromotive force or voltage is generated between the two electrodes through conversion of Gibbs free energy – that is, the energy available to do electrical work. This work involves moving electrons around an external circuit so that the electrical power can be extracted (Basu 2007:177).

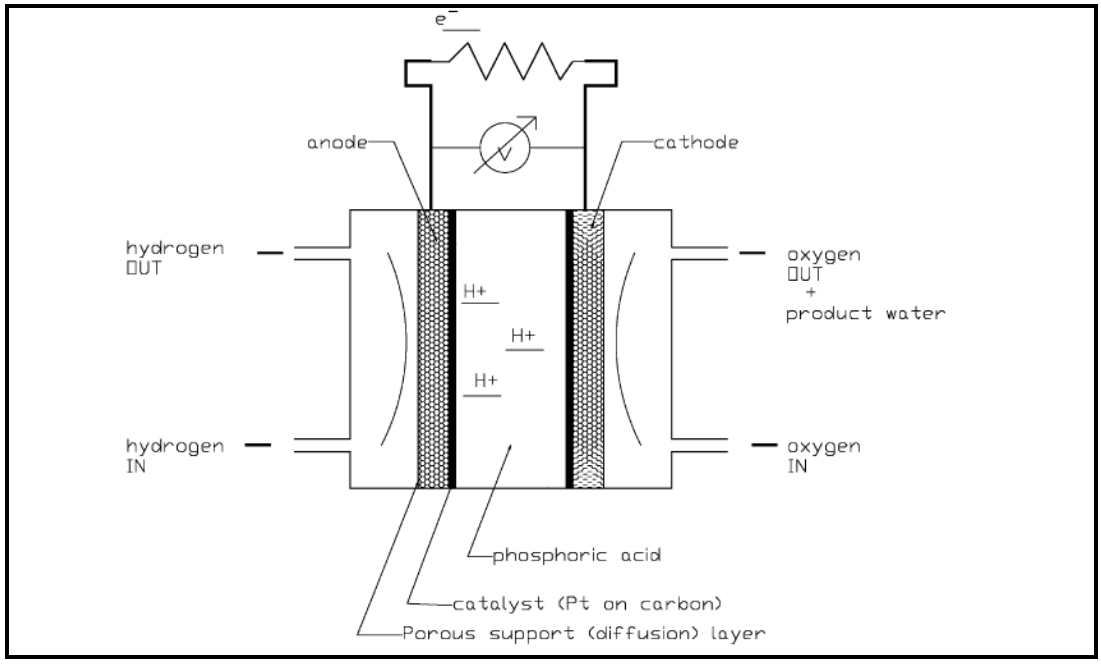



**Figure 2: Structure of a single cell PAFC (Basu 2007:189)**

During operation, especially during high-temperature operation, phosphoric acid must be continually replenished because it gradually evaporates into the environment (O'Hayre, Won Cha, Colella & Prinz 2009:262).

The reactions at the anode and cathode are as follows:

At the anode: $$H_2 \rightarrow 2H^+ + 2e^- \quad (1)$$

At the cathode: $$\frac{1}{2}O_2 + 2H^+ + 2e^- \rightarrow H_2O \quad (2)$$

The only by-products of the FC are water and heat generated by the chemical reaction. The overall reaction of a hydrogen-oxygen FC can be given by:

$$H_2 + \frac{1}{2}O_2 \rightarrow H_2O \quad (3)$$

The operating temperature is found to be comprised between the electrolyte conductivity (which increases with temperature) and cell life which decreases when the temperature is increased (Brandon & Thompsett 2005:157). Pure phosphoric acid solidifies at 42 °C. Therefore, PAFCs must be operated above this temperature. Because freeze-thaw cycles can cause serious stress issues, commissioned PAFCs are usually maintained at an even operating temperature.

### 2.2.2 *V-I* characteristics of a PAFC

A polarisation curve or cell voltage-load current (*V-I*) characteristic may be used to express the performance of a FC. Modelling the *V-I* characteristics of FC systems may well be necessary for the design of the power conditioning unit, FC system controllers, FC stack simulator systems and optimisation of FC operating points, because they are largely dependent on such characteristics. The performance of the FC is improved by thermodynamics and electrical efficiency of the system. The thermodynamic efficiency depends upon the fuel processing, water management and

temperature control of the system. But the electrical efficiency depends on the various losses over the FCs such as ohmic loss, activation loss and concentration loss (Kirubakaran, Shailendra & Nema 2009:2433). These losses contribute to the drop of a FC output voltage as its current increases.

According to Barbir (2005:249) there are three distinct regions on a FC polarisation curve noticeable in Figure 3 which portrays the cell voltage versus current density characteristic of a typical fuel cell system:

- Activation polarisation (region 1),
- Ohmic polarisation (region 2),
- Concentration polarisation (region 3),

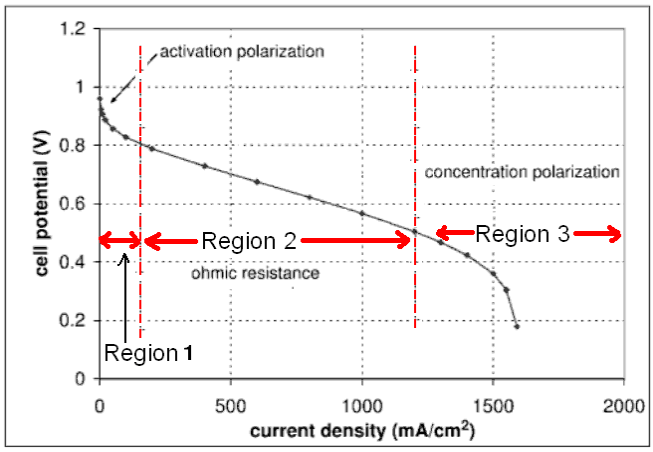



**Figure 3: *V-I* characteristic of a typical FC (Barbir 2005:250)**

These losses are often referred to as polarisation, overpotential or overvoltage, though only the ohmic losses actually behave as a resistance (EG & G Technical Services Inc. 2004:2-10).

Zhao, Kreuer and Nguyen (2007:34-35) explain each of these regions as follows:

- **Activation polarisation:** arises from the slow rate of electrochemical reactions and a portion of the energy is lost (or spent) on driving up the rate

of electrochemical reactions in order to meet the rate required by the current demand. In other words, the activation polarisation loss is dominant at low current density. This is caused by the slowness of the reaction taking place on the surface of the electrodes. These losses are basically representative of a loss of overall voltage at the expense of forcing the reaction to completion, which is forcing the hydrogen to split into electrons and protons and for the protons to travel though the electrolyte and then combine with the oxygen and returning electrons. This loss is often termed over-potential and is essentially the voltage difference between the two terminals.

- **Ohmic polarisation:** arises owing to electrical resistance in the cell, including ionic resistance to the flow of ions in the electrolyte and electronic resistance to the flow of electrons in the rest of the cell components. Normally, the ohmic polarisation is linearly dependent on the cell current. Ways to reduce the value of the ohmic resistance are (Larminie & Dicks 2003:57):
    - To use high conductivity electrodes,
    - Good design of the appropriate materials for the bipolar plates or cell interconnections,
    - Reduce the space of the electrodes in order to minimize the electrolyte resistance.

- **Concentration polarisation:** is caused by the slow rate of mass transfer resulting in the depletion of reactants in the vicinity of active reaction sites and the over-accumulation of reaction products which block the reactants from reaching the reaction sites. It usually becomes significant or even prohibitive, at high current density when the slow rate of mass transfer is unable to meet the high demand required by the high current output.

## 2.3 Fundamentals of converters for a PAFC

The power electronics conditioning systems (inverters or converters) are required in

order to supply normal customer load demand or send electricity into the grid supplied by a PAFC (Chakraborty, Kramer & Kroposki 2009:2327).

However, the electric characteristic of a converter for example should match that of the FC. This is particularly important for three reasons (Xu, Kong & Wen 2004:1136):

- The input side current/voltage ripple of the DC–DC converter should be minimum, so as to reduce the ripple current/voltage of the FC,
- When the FC is working under load current pulses, the DC–DC converter must apply a suitable strategy to adjust the output power of the FC, so as to ensure high-efficiency and reliable operation,
- The DC–DC converter should be able to adjust power distribution in the case of hybrid power configurations. Taking into account the above requirements, a DC–DC converter should be designed using a topology structure and control strategy, which is slightly different from those of conventional converters.

Basu (2007:209) explains that there are various techniques available to stabilise the output potential from a PAFC stack. A typical method is to convert unstabilised low potential DC into a high voltage AC. This is achieved by using switching devices in series with the primary of the transformer. The output from the FC is connected to the primary of the transformer through the switching device. As the device switches ON and OFF at a pre-determined frequency, an AC potential is generated at the secondary of the transformer. The AC frequency is dependent on the switching frequency. The waveform of the AC potential is a square wave and the one of the current is a rounded square to near triangular waveform depending upon the circuit impedance. The potential of the AC generated is dependent upon the transformer windings. The overall stabilisation of the high frequency AC voltage is carried out by dynamically changing the ON and OFF time of the switching device. The high frequency AC is then either converted into a stabilised DC voltage through a rectifier circuit or is converted into a lower voltage AC as required by the application. The

major losses that occur during the overall conversion are at the section where variable DC input is converted to high frequency AC. Hence, the switching devices and the switching control mechanisms are of primary concern to achieve high efficiency. Other aspects that are to be considered involve output voltage regulation and the variable DC input window. All these aspects are interrelated and have to be considered in a holistic manner. The transformer weight (for smaller power plants) needs to be low for easy transportation. To achieve this, a higher frequency AC may be selected but at the cost of more losses in the switching device.

## 2.4 PAFC converter key design considerations

Based on the fact that the behaviour of the output voltage is generally similar for all types of FCs, the following subsections discuss key requirements for FC converters.

### 2.4.1 Wide input voltage and current window

Since the FC voltage varies significantly depending on the current that it is supplying to the load, a wide input range DC–DC converter is required (Todorovic, Palma & Enjeti 2008:1248).

Polenov, Mehlich and Lutz (2006:1974-1979) reported that the wide FC output voltage range results in two main requirements for the dimensioning of the switching devices in converters for FCs which are:

- At no load condition a maximum FC voltage is applied to the converter input. It determines together with topology characteristics the minimum necessary blocking voltage of semiconductor devices at the FC side. For most of the popular topologies, the minimum required MOSFET blocking capability is the maximum converter input voltage which is the FC voltage. The push-pull converter is an exception because its input voltage is twice the maximum FC voltage.

- The main requirement for dimensioning of the MOSFET is the current capability because the FC output current increases nonlinearly with the rising output power.

As the requirement of high efficiency of the PAFC converter is crucial, the power loss caused by the low-voltage MOSFET needs to be analysed and reduced as far as possible. For optimisation of the efficiency of any converter used for power conditioning in FC systems, low $R_{DSon}$ switches are necessary. Paralleling of several MOSFETs is a way to reduce conducting losses. However, this comes at a higher cost as well as the need for additional space on the printed circuit board (PCB).

### 2.4.2 Efficiency

In a low potential high current device such as a PAFC, the target efficiency for the DC–DC converter should be greater than 85 percent (Basu 2007:209). This is due to the fact that the unregulated DC voltage can vary widely with the load and ageing of the stack. In addition, considering the low-voltage, high-current nature of the FC, switching and conduction losses of the converter need to be minimized. A high efficiency converter will contribute to improve the total system efficiency (Huang, Zhang & Jiang 2006:1616).

### 2.4.3 Reverse current

Current flow into the FC is detrimental to it. Therefore to avoid current acceptance to the FC, a diode $D_{FC}$ can be inserted in series with the FC module as depicted in Figure 4.

In applications, where reverse current can be expected, a capacitor $C_{DC}$ is implemented to absorb the current. But caution in selecting the capacitor and operating the system is crucial to ensure that the capacitor is not overly stressed (Yu, Starke, Tolbert & Ozpineci 2007:645-646).

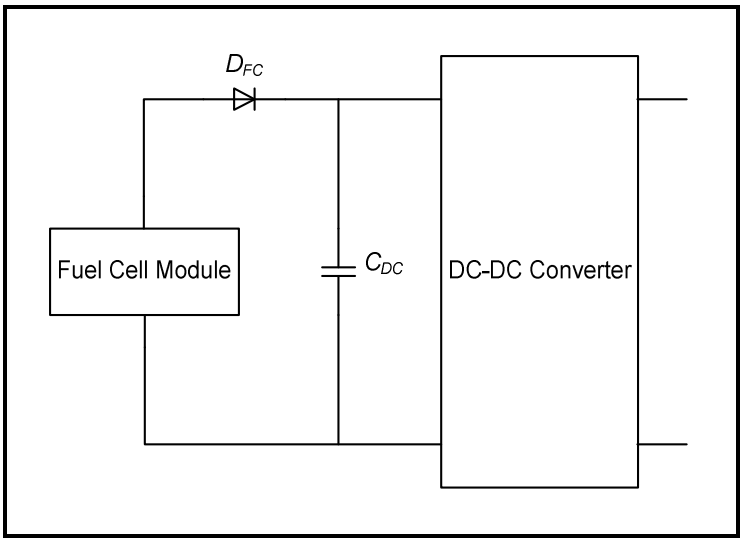



**Figure 4: Reverse current protection (Yu *et al.* 2007:646)**

### 2.4.4 Input ripple current

FCs prefer a pure DC load. Any disturbance on the DC output of the fuel cell can have a significant impact on the conditions within the fuel cell diffusion layer. Some of this ripple current can be absorbed through the addition of a capacitor (Yu *et al.* 2007:646).

### 2.4.5 Electrical isolation

For safety purposes, electric isolation is essential to protect a FC. This is made possible by means of a transformer incorporated in the DC–DC converter interfacing the low voltage output of the FC and high-voltage DC link. This is particularly needed when the difference in voltage is significant (Yu *et al.* 2007:646).

In a DC–DC converter combined with a DC–AC inverter system, the DC–DC converter is used for isolation and voltage step-up while the inverter is needed to provide an AC voltage from a DC source. In general, both DC–DC converters and DC–AC inverters have many topologies for selection, including hard-switching and soft-switching circuits (Blaabjerg, Chen & Kjaer 2004:1188).

## 2.5 Review of power electronics converters

DC–DC conversion technology is a vast subject area. It developed very fast and achieved much. DC–DC converters are power electronics circuits that convert a DC voltage to a different DC voltage level, often providing a regulated output (Hart 1997:185).

There are believed to be more than five hundred existing topologies of DC–DC converters according to current statistics. DC–DC converters have been widely used in industrial applications such as DC motor drives, communication equipment, mobile phones and digital cameras. Many new topologies have been developed in recent decades (Luo & Ye 2010:23).

A converter topology refers to the arrangement of components within the converter. Power DC–DC converters have plenty of topologies and the corresponding conversion technique is a big research topic. Dr F L Luo and Dr H Ye have categorised all existing prototypes of power DC–DC converters into six generations theoretically and evolutionarily since 2001. Their work is an outstanding contribution in the development of DC–DC conversion technology and has been recognized and assessed by experts worldwide (Luo, Ye & Rashid 2005:178). A more detailed description on DC–DC converters can be found in Luo and Ye (2004).

The notion of the DC–DC converter is closely intertwined with that of power supply. A power supply is a constant voltage source with a maximum current capability. According to Dorf (2006:9-14) “DC–DC converters are widely used in switch-mode DC power supplies and in DC motor drive applications”. There are two general classes of power supplies: regulated and unregulated. Figure 5 shows a classification of regulated power supply technologies. Two of the most popular categories of voltage regulators are linear regulators and switching-mode power supplies. There are two basic linear regulator topologies: the series voltage regulator and the shunt voltage regulator. The switching-mode voltage regulators are divided into three

categories: PWM DC–DC converters, resonant DC–DC converters and switched-capacitor (also called charge-pump) voltage regulators (Kazimierczuk 2008:1).

To highlight the benefit of a switching regulator which is intended to be used for this work, an examination of the basic properties of what preceded them is discussed in the following subsection.

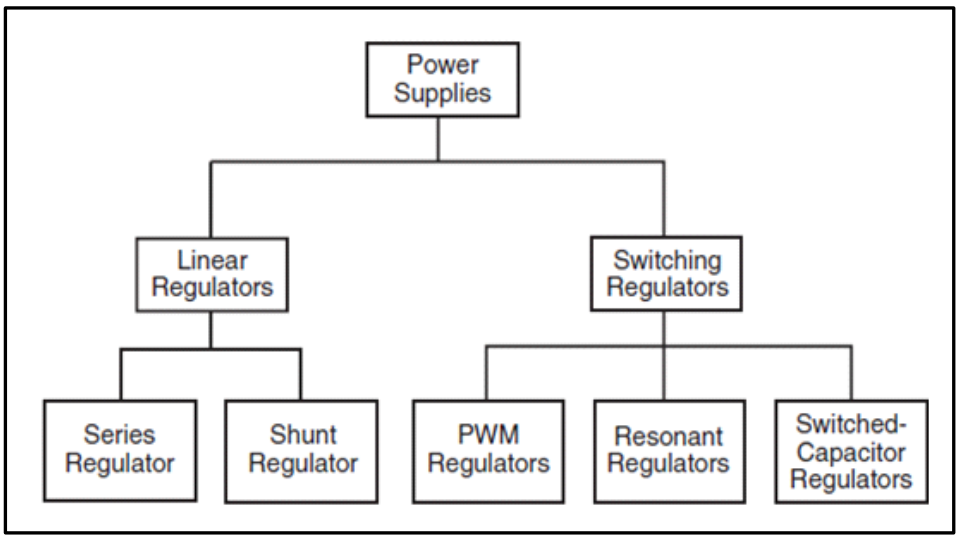



**Figure 5: Classification of power supply technologies (Kazimierczuk 2008:2)**

### 2.5.1 Linear regulators

A linear regulator makes use of an amplifier and a transistor to control the current supplied to the load (Shaffer 2007:187). This type of circuit is called a linear regulator or a linear DC–DC converter because the transistor operates in the linear region, rather than in the saturation or cutoff region. This means that the transistor is used in a manner that it is not switched fully on or fully off. Rather, the gate voltage is adjusted so that its resistance is at the correct value to drop the voltage to the desired value. This resistance will vary continuously depending on the load current and the supply voltage (Larminie & Dicks, 2003:336). The transistor, in effect, operates as a variable resistance (Hart 1997:185). Linear regulators are used predominantly in ground-based equipment where the generation of heat and low

efficiency are not of major concern and also where low cost and a short design period are desired. Figure 6 shows a series pass linear DC–DC regulator.

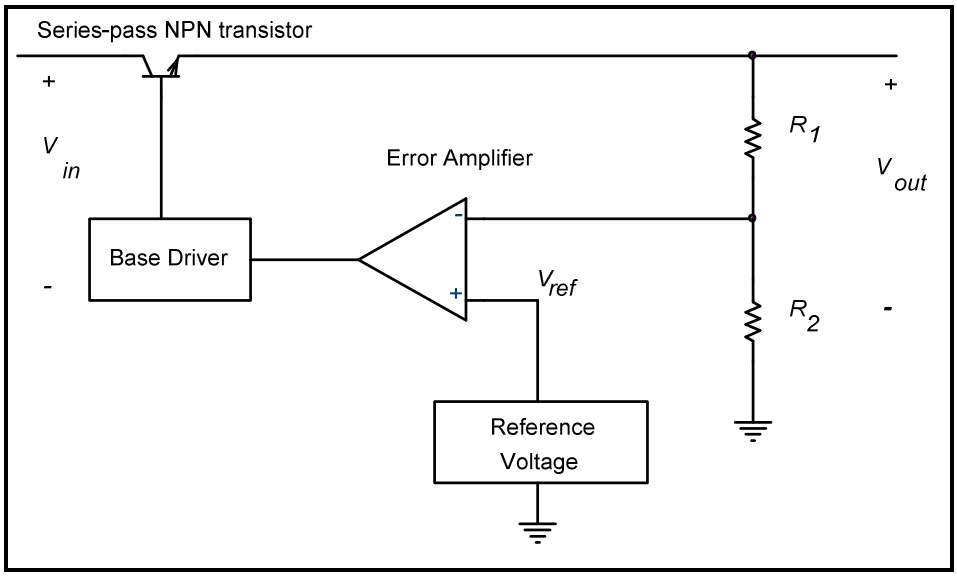



**Figure 6: Series pass linear regulator**

The linear power supply offers three major advantages. The first advantage is its simplicity. The second major advantage is its quiet operation and load-handling capability. The linear regulator generates little or no electrical noise on its output and its dynamic load response time — the time it takes to respond to changes in the load current — is very short. The third advantage is that, for an output power of less than approximately 10 W, its component costs and manufacturing costs are less than the comparable switching regulator (Brown 2001:1). Also, since the power losses are mainly due to the DC current and the voltage across the semiconductor switching element, the loss and the overall efficiency are easily calculated. Lower radio frequency interference (RFI) noise is an advantage in some applications, and for this reason, linear regulators still have a place in modern power supply applications (Pressman, Billings & Morey 2009:5).

According to Kularatna (2008:83) “when high-speed and power-hungry processors were introduced during the mid-1990s, much attention was focused on transient

response and industry trends were to mix linear and switching systems to obtain the best of both worlds". This has led to low dropout (LDO) voltage regulators based on linear designs. LDO regulators were introduced to power noise-sensitive and fast transient loads in many portable products. When compared to a high-frequency switching technique based on switched mode power supply (SMPS) solution, LDOs allow faster transients, have less noise and are more compact on a PCB (Kularatna 2008:83).

The disadvantages of the linear regulators are what limits their range of applications. Firstly, it can be used only as a step-down regulator. Secondly, each linear regulator can have only one output. So for each additional output voltage required, an entire separate linear regulator must be added. This requirement for multiple voltages once again drives up the system cost. Another major disadvantage is the average efficiency of linear regulators. In normal applications, linear regulators exhibit efficiency of 30 to 60 percent (Brown 2001:1-2). Further, the high power loss in the semiconductor device requires a large heat sink and large storage capacitors and makes the linear power supply disproportionately large (Pressman *et al.* 2009:11).

According to Larminie and Dicks (2003:336) linear regulator circuits are widely used in electronic systems, but they must never be utilised with fuel cells. The reason is that they waste energy by converting the surplus voltage into heat.

### 2.5.2 Switched regulators

Ang and Oliva (2005:1) define a switching converter as a power electronic system, which converts one level of electrical energy into another level of electrical energy at the load, by switching action. According to Maniktala (2006:3) DC–DC converters are the basic building blocks of modern high-frequency switching power supplies. Switching power supplies gained popularity in the mid-1970s owing to the fact that they offer many advantages over linear regulators. Switching power supplies are more efficient and smaller in size than linear regulators of similar ratings. They are,

however, more difficult to design and radiate more electromagnetic interference (Brown 2001:21).

Brown (2001:21-22) further says that in this technology, the direct current or the rectified alternating current input voltage is 'chopped' into pulses whose amplitude is the magnitude of the input voltage and whose duty cycle is controlled by a switching regulator controller. Once the input is converted to an AC rectangular waveform, the amplitude can be stepped up or down by a transformer. The AC waveforms are then filtered to provide the DC output voltages. Supplementary output voltages can be derived by adding secondaries to the transformer. Many electronic circuits operating at several different voltage levels using a DC–DC conversion method make it convenient to convert energy from a single source rather than to get the supply from many different supplies. This DC–DC conversion circuit has been classified as SMPS. The SMPS method is more efficient (up to 98 percent) than linear voltage regulation which dissipates losses as heat.

#### 2.5.2.1 PWM regulators

These converters employ square-wave PWM to achieve voltage regulation. The average output voltage is varied by varying the duty cycle of the power semiconductor switch. The voltage waveform across the switch and at the output is square-wave in nature and they generally result in higher switching losses when the switching frequency is increased. Also, the switching stresses are high, accompanied by the generation of a high level of electromagnetic interference (EMI), which is difficult to filter. However, these converters are easy to control, well understood and have a wide load control range (Dorf 2006:9-18).

According to Lee (1993:2) there are three basic types of switched semiconductor DC–DC converters: the buck converter, the boost converter and the buck-boost converter from which many different SMPS circuit topologies have been developed. For example, a buck converter with an isolation transformer is called a forward

converter and buck-boost converter with an isolation transformer is known as a flyback converter. The push-pull converter, half-bridge converter and full-bridge converter are variants of the forward converter. All these converters process power in pulsed form and are called PWM converters or hard-switching converters. This is because in practice, PWM controller ICs are chosen to produce the square pulse to drive the switching elements which are MOSFETs or IGBTs. The advantage of using PWM controller ICs is their compatibility with voltage or current mode topologies as well as with different switching power supply topologies.

The methods of control of PWM converters are discussed next. According to Dorf (2006:9-18) the PWM converters operate with a fixed frequency and a variable duty cycle. Depending on the duty cycle, they can operate in either continuous current mode (CCM) or discontinuous current mode (DCM). If the current through the output inductor never reaches zero then the converter operates in CCM; otherwise DCM occurs.

PWM converters are suited for fuel cells because they make it possible for the energy produced by a fuel cell to be converted efficiently without significant losses compared to linear regulators. PWM switched-mode DC–DC converter topologies which are at the heart of switching power supplies for fuel cells are examined later in this chapter. Other types of DC–DC converters are also briefly examined.

#### 2.5.2.2 Resonant regulators

The term ‘resonant’ here refers to a continuous sinusoidal signal. Resonant converters which use the principle of a resonating LC tank circuit are those which process power in a sinusoidal form and have long been used with high-power systems. However, owing to its circuit complexity, it had not found application in low-power DC–DC converters until the early 1990s. The thrust toward resonant supplies has been fueled by the industry’s demand for miniaturisation, together with increasing power densities and overall efficiency as well as low EMI. All resonant control circuits keep the pulse width constant and vary the frequency, whereas all

PWM control circuits keep the frequency constant and vary the pulse width (Kularatna 2008:137).

The advantages of resonant DC–DC converters are that they have a drastic reduction of the switching losses within the supply, which is one of the top heat-generating losses. This removes 30 to 40 percent of the losses within a comparable PWM supply when operated at the same frequency. The designer can then increase the operating frequency in order to reduce the major component sizes, hence increasing the power density. As a result power supplies operating at 500 kHz and higher is definitely achievable. An added advantage that is in the designer's favour is the significant reduction in radio frequency interference (RFI) or electromagnetic interference (EMI). By eliminating the very rapid transitions in current and voltage, the harmonic-rich waveforms are also eliminated. This makes it easier to pass the RFI requirements imposed by the approval bodies with less RFI filtering (Brown 1990:171).

However, the disadvantages of resonant converters are that they are more complex than their PWM counterparts and consequently require a longer time to design and cost more to implement.

#### 2.5.2.3 Switched capacitors regulators

According to Kularatna (2008:84) charge pumps, switched capacitors, flying capacitors, and inductorless converters are all different names for DC–DC converters that use a set of capacitors rather than an inductor or transformer for energy storage and conversion. For many years, designers have used charge pumps for DC–DC conversion in applications for which the regulation tolerance, current conversion efficiency and noise specifications are not very stringent. These circuits use capacitors combined with switches to boost or invert the input voltage and they do not occupy more PCB or silicon area than a single-chip converter, to implement. Recent generations of charge pumps have become viable DC–DC conversion methods for cellular phones, portable wireless equipment, notebook computers and

PDAs, where high-density DC–DC conversion is necessary and circuit area is at a premium.

## 2.6 FC converter topologies

Conventional converter topologies used with FC systems are first examined. These converters are not only implemented in FC applications, but have also been heavily employed in everyday applications. Following the discussion of conventional converters, a section representing DC–DC converter topologies specifically designed for FC usage is introduced (Yu *et al.* 2007:647). Basically popular converter topologies fall into two main categories: non-transformer-isolated and transformer-isolated.

### 2.6.1 Non-transformer-isolated converter topologies

Non-transformer-isolated converters such as the buck, boost and buck-boost converter topologies are generally used for lower-power level converter circuits and are not so popular for higher-power applications (Kularatna 2008:108). These converters have two main problems: linkage between input and output and very large output voltage ripple.

#### 2.6.1.1 Step-down (buck) converter

The step-down DC–DC converter, commonly known as a buck converter, is shown in Figure 7. It consists of a DC input voltage source $V_S$, controlled switch $Q_S$, diode $D$, filter inductor $L$, filter capacitor $C$ and load resistance $R_L$. Typical waveforms in the converter are shown in Figure 8 under the assumption that the converter works in CCM. It can be seen from the circuit that when the switch $Q_S$ is commanded to the ON state, the diode $D$ is reverse-biased. When the switch $Q_S$ is OFF, the diode conducts to support an uninterrupted current in the inductor (Rashid 2001:213).

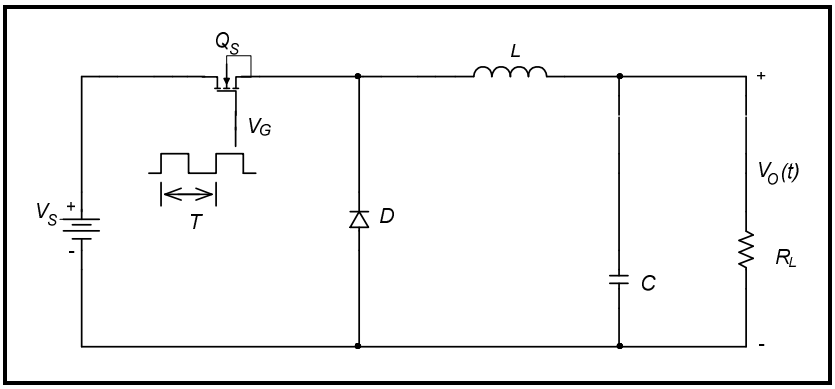



**Figure 7: Buck converter topology**

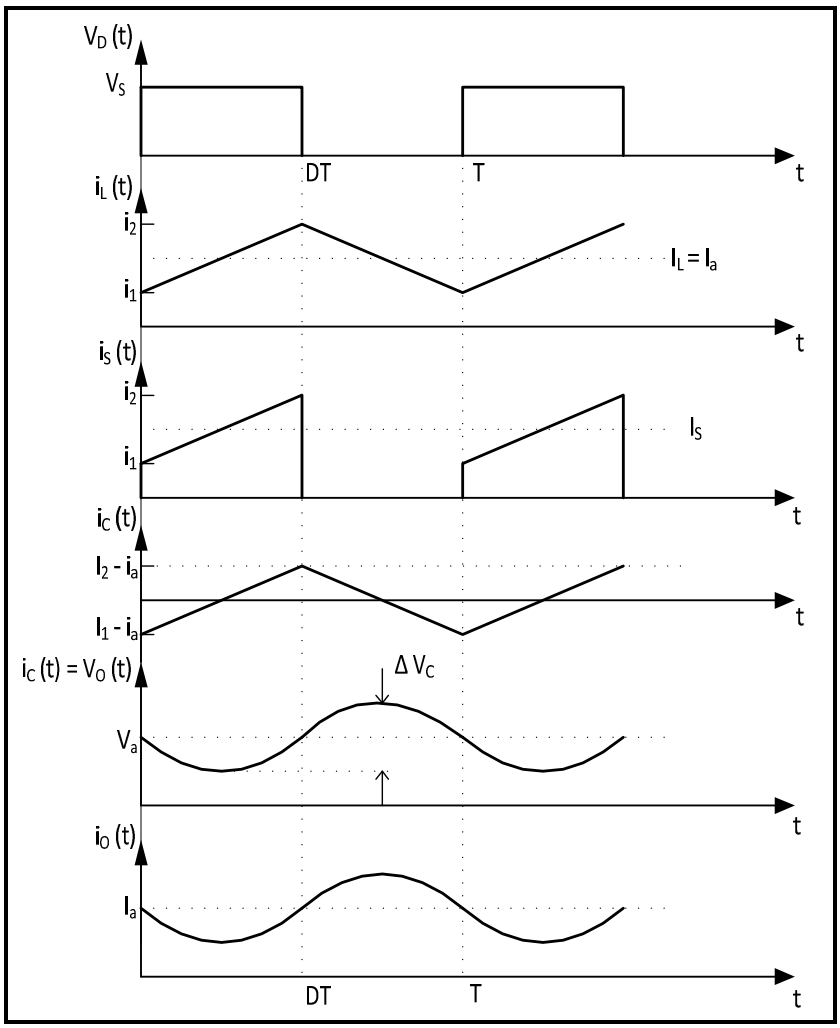



**Figure 8: Voltages and currents during on-off cycle of the buck topology (Ang & Oliva 2005:23)**

The output voltage of a buck converter is always less than the input voltage. The switch produces a pulse-width-modulated waveform to the passive components. When the regulator is at steady state, the average output voltage is:

$$V_o = V_s \cdot \frac{t_{on}}{T} = V_s \cdot D \tag{4}$$

where $T \equiv$ total period in s = 1/$f$, (where $f$ is the switching frequency)

$t_{on} \equiv$ power device ON time in s

$D \equiv$ duty cycle = $t_{on}/T$

A prominent application of the buck converter is a DC-regulated power supply in which the output voltage is regulated against the variations in the load resistance and the input voltages. These power supplies are used in computers and portable instruments in the medical and communication fields (Agrawal 2001:178). According to Mohan, Undeland and Robbins (2003:164), it is also used in DC motor speed control.

The buck regulator topology has the limitation that it can only produce a lower voltage from a higher voltage (Pressman *et al.* 2009:31).

#### 2.6.1.2 Step-up (boost) converter

The boost converter or step-up converter is a well-known switched-mode converter capable of producing an output voltage larger than the input (Hart 2006:211). Its circuit diagram is shown in Figure 9. An inductor $L$ is placed in series with $Vs$ and a controlled switch $Q_S$ to common or ground. The converter waveforms are presented in Figure 10. When the switch $Q_S$ is in the ON state, the current in the boost inductor increases linearly and the diode $D$ is OFF at that time. When the switch $Q_S$ is turned OFF, the energy stored in the inductor is released through the diode to the output circuit formed by $R_L$ and $C$ (Rashid 2001:216).

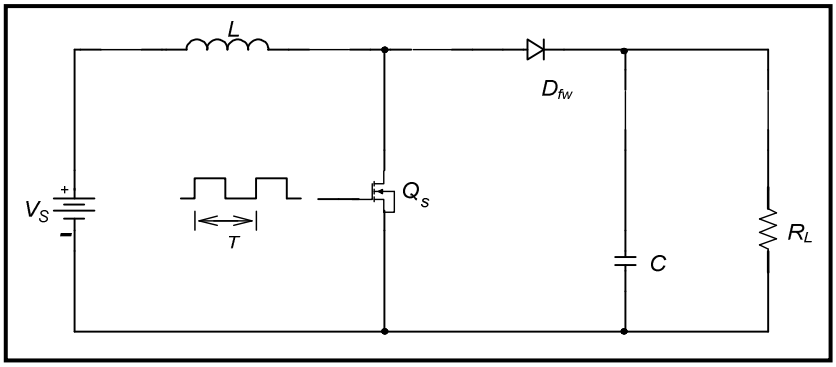



**Figure 9: Boost converter topology**

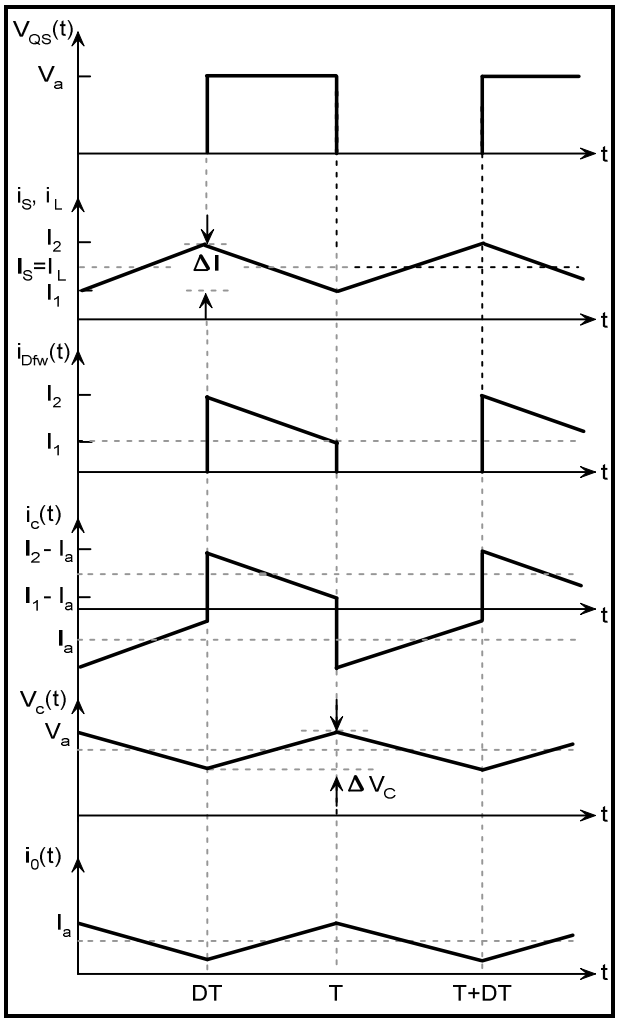



**Figure 10: Voltage and current waveforms of a boost topology (Ang & Oliva 2005:33)**

Zhang, Pittini, Andersen and Thomsen (2012:3) report that as to the non-isolated converters, normally, boost-type converters are favourable to fuel cell application. Still they require a bulky input inductor to limit the current ripple in the components, especially when high voltage gains are required. To minimize the input inductor size and the current ripple, as well as to reduce the switch current stress, the converter can be designed with multiple legs interleaving each other by means of the input coupling inductors and high efficiency can thereby be obtained. In DC–DC converters the efficiency of the conventional boost converter is always greater than the other converter topologies such as the push-pull, half-bridge, full-bridge, etc., because it has a reduced component count and simplicity in control. But from the protection point of view, electrical isolation is not possible in a boost converter (Kirubakaran *et al.* 2009:2437).

In the CCM of operation, considering *D* as the duty ratio, the input-output relation is as follows:

$$\frac{V_o}{V_s} = \frac{1}{1-D} \tag{5}$$

The use of this topology to boost the voltage supplied by fuel cells is feasible when the ratio between the output voltage and the input voltage is not higher than two or three times and when galvanic isolation is not required.

#### 2.6.1.3 Buck-boost converter

The buck-boost regulator is shown in Figure 11. It can provide both a step-down and a step-up function. With the switch ON, the inductor current increases while the diode is maintained OFF. When the switch is turned OFF, the diode provides a path for the inductor current. The buck-boost converter waveforms are depicted in Figure 12.

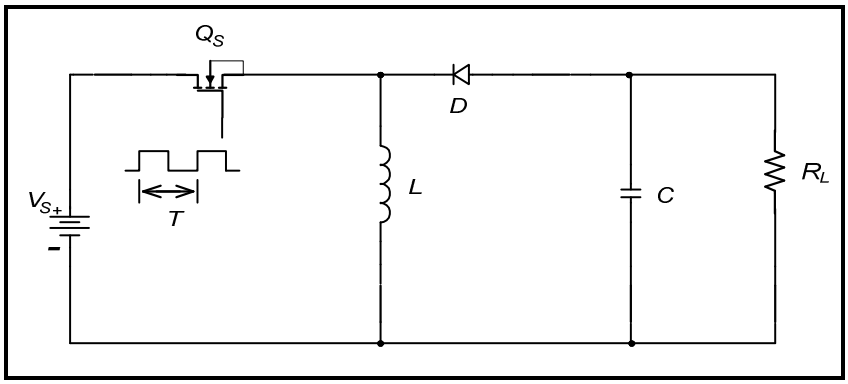



**Figure 11: Buck-boost converter topology**

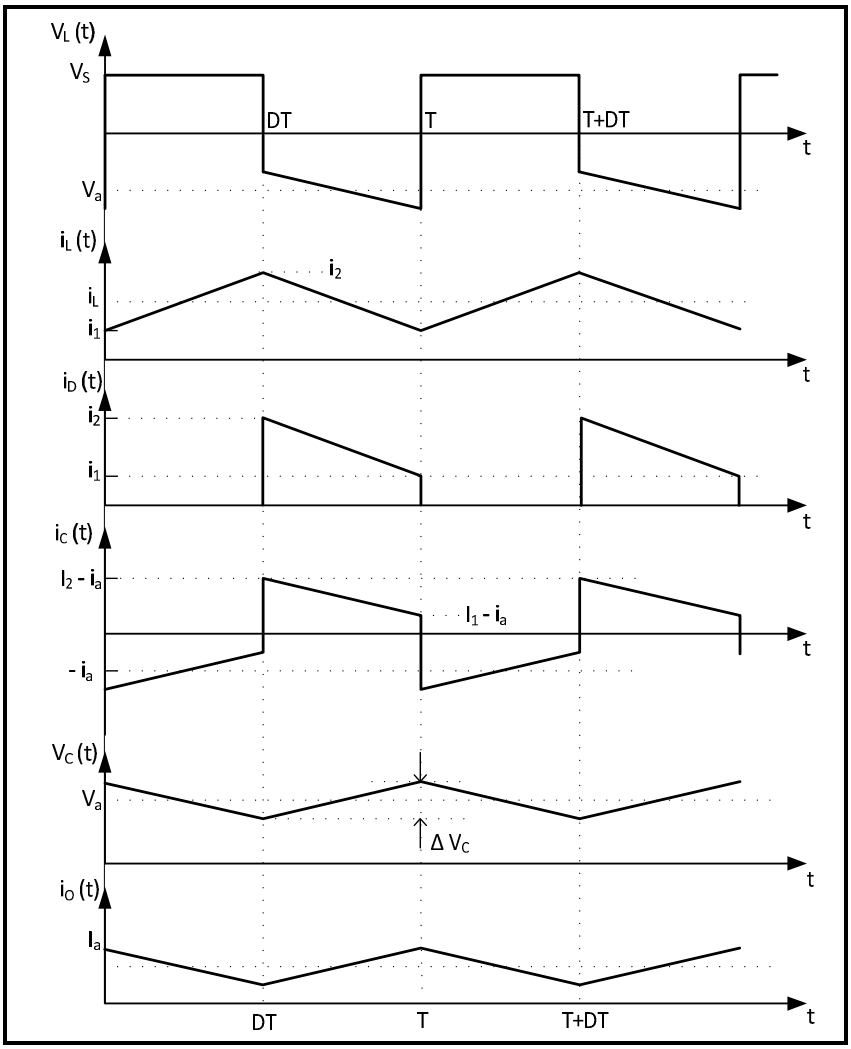



**Figure 12: Waveforms inside the components of a buck-boost topology (Ang & Oliva 2005:44)**

The input-output relation over one complete cycle is:

$$\frac{V_o}{V_s} = \frac{t_{on}}{t_{off}} = \frac{D \cdot T}{(1-D) \cdot T} = -\left( \frac{D}{1-D} \right) \tag{6}$$

The main application of the buck-boost converter is in regulated DC power supplies, where a negative-polarity output with respect to the common terminal of the input voltage may be desired and the output voltage can be higher or lower than the input voltage (Mohan *et al.* 2003:178).

When applied to FCs, the final output of the buck-boost converter is usually set somewhere within the operating range of the FC. While such circuits are technically possible, their efficiency tends to be rather poor, certainly no better than the boost, mostly worse. The consequence is that this is not a good approach (Larminie & Dicks 2003:338).

#### 2.6.1.4 Çuk converter

The circuit of the Çuk converter is shown in Figure 13. This topology consists of a DC input voltage source $V_s$, input inductor $L_i$, controllable switch $Q_s$, energy transfer capacitor $C_t$, diode $D_{fw}$, filter inductor $L_o$, filter capacitor $C_o$ and load.

According to Rashid (2001:218) an important advantage of this topology is a continuous current at both the input and the output of the converter. Disadvantages of the Çuk converter are a high number of reactive components and high current stresses on the switch $Q_s$, the diode $D_{fw}$ and the capacitor $C_t$. The main waveforms in the converter are presented in Figure 14. When the switch is ON, the diode is OFF and the capacitor $C_o$ is discharged by the inductor $L_o$ current. With the switch in the OFF state, the diode conducts the currents of the inductors $L_i$ and $L_o$, whereas capacitor $C_t$ is charged by the inductor $L_i$ current.

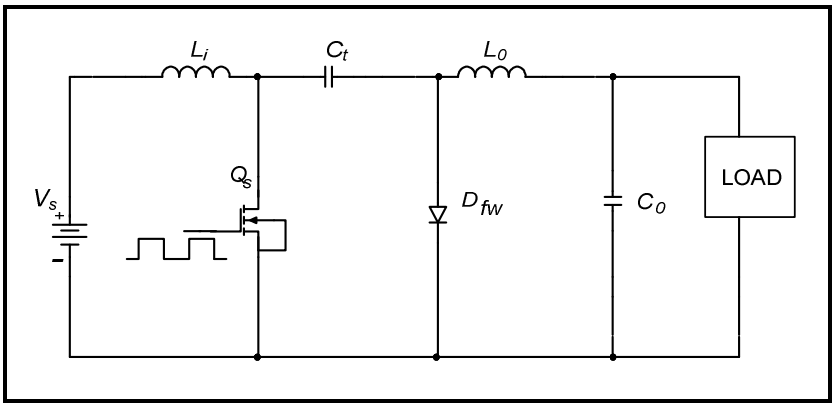



**Figure 13: Çuk converter topology**

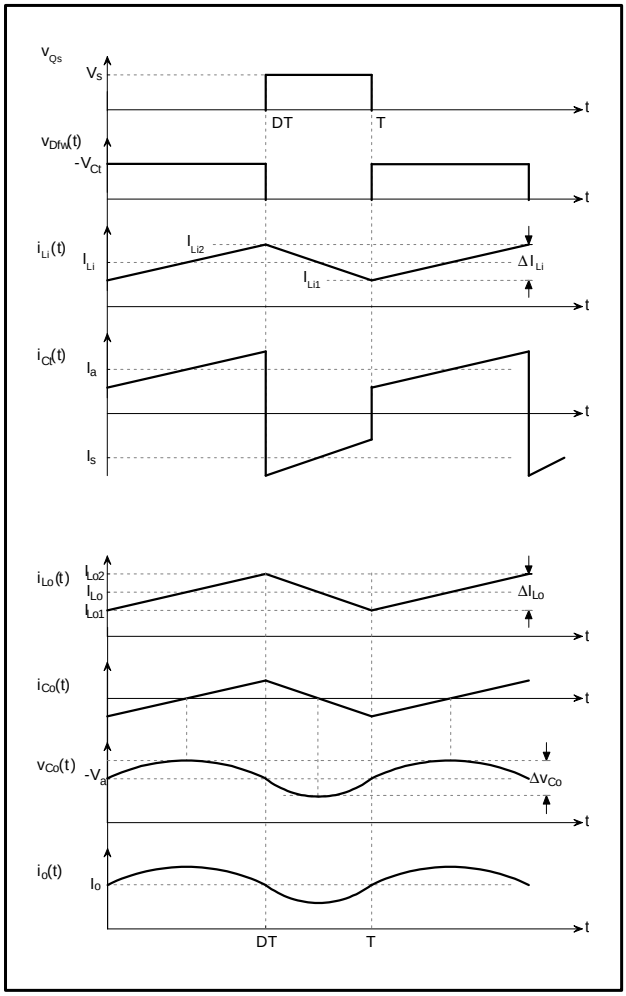



**Figure 14: Voltage and current waveforms of the Çuk converter topology (Ang & Oliva 2005:54)**

The input-output voltage relation is the same as that for the buck-boost converter. Hence, the DC gain of the Çuk converter is:

$$\frac{V_o}{V_s} = \frac{D}{1-D} \tag{7}$$

The advantage of this circuit is that both the currents at input and output stages are reasonably ripple free (unlike the buck-boost converter where both these currents are highly discontinuous). It is possible to simultaneously eliminate the ripples in $i_{Li}$ and $i_{Lo}$ completely, leading to lower external filtering requirements. A significant disadvantage is the requirement of a capacitor $C_t$ with large ripple-current-carrying capability (Mohan *et al.* 2003:186).

### 2.6.2 Transformer-isolated converters

Transformer-isolated converters such as forward, push-pull, half-bridge and full-bridge, etc. are particularly appreciated for electrical isolation and high boost ratio. In this section, these converter topologies are examined.

#### 2.6.2.1 Flyback converter

The flyback converter is shown in Figure 15 and its waveforms are shown in Figure 16. In this converter, when the transistor is ON, energy is stored in the coupled inductor (not a transformer) and this energy is transferred to the load when the switch is OFF (Dorf 2006:9-18).

The output voltage is calculated by means of the formula,

$$V_o = \frac{D}{1-D} \cdot n \cdot V_s \tag{8}$$

where $n$ is the transformer turns ratio.

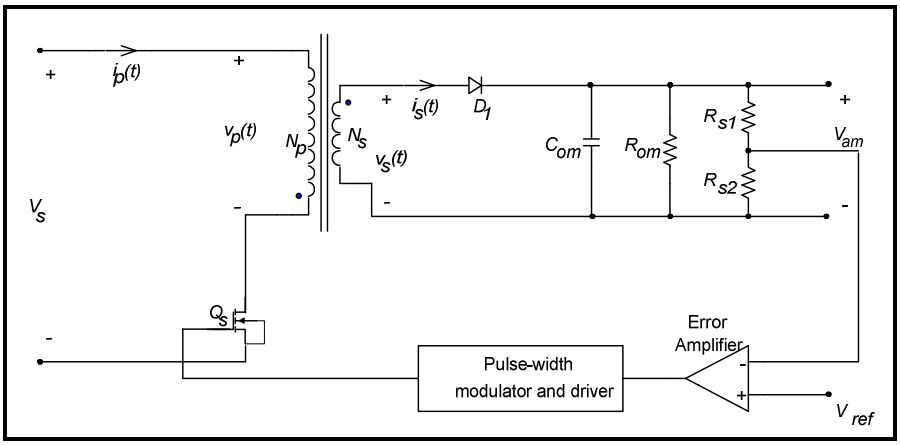



**Figure 15: Flyback converter topology**

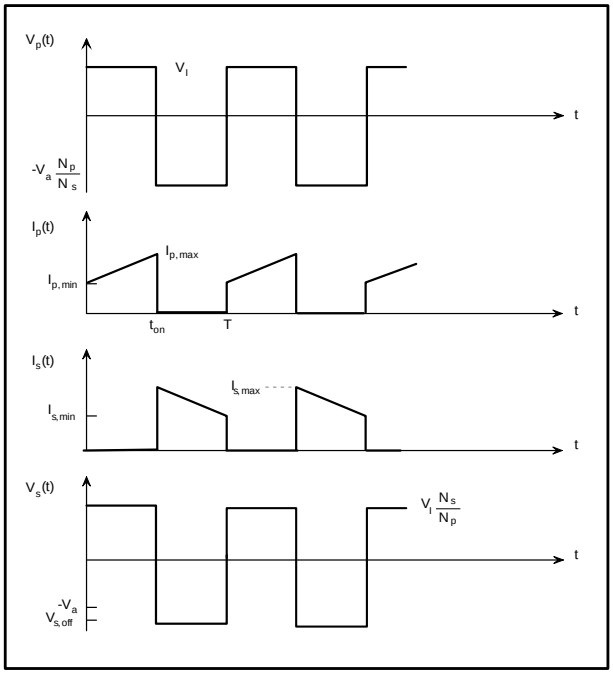



**Figure 16: Voltage and current waveforms of the flyback converter topology (Ang & Oliva 2005:149)**

Flyback converter operation can lead to confusion if the approach in the design of its magnetics is considered to be a transformer. Except for the case of multiple output windings, the magnetics in a flyback converter are not a transformer. An easy way to

view this is as an energy bucket that is alternately filled (when the switch is ON) and dumped (when the switch is OFF). In other words, a flyback magnetic (sometimes called a transformer choke) is an energy-in, energy-out power transfer device where input and output windings do not conduct current simultaneously. A gapped core is used in general to have adequate leakage inductance at the input side for energy storage during the switch-on period (Kularatna 2008:109).

Low cost and simplicity are the major advantages of the flyback topology. These converters are inexpensive because the transformer (which really works as a coupled inductor) is part of the output filter and generating multiple outputs merely requires the addition of another secondary winding along with diodes and output filter capacitors (Kularatna 2008:129).

Other advantages of this converter are that the leakage inductance is in series with the output diode when current is delivered to the output and, therefore, no filter inductor is required. It is ideally suited for high-voltage output applications. Flyback converters are used in the power range of 20 to 200 W. However, at power levels greater than 200 W, because of excessive peak currents in the switching transistor and excessive voltages across the switches, this topology reaches its limitations.

Some of the disadvantages are that large output filter capacitors are required to smooth the pulsating output current, inductor size is large since air-gaps are to be provided and owing to stability reasons, flyback converters are usually operated in DCM, which results in increased losses. To avoid the stability problem, flyback converters are operated with current mode control (Dorf 2006:9-18, 9-19).

#### 2.6.2.2 Forward converter

The forward converter represented in Figure 17 is derived from the buck topology family, generally employing a single switch. The power switch in the forward topology is ground referenced (also called a low-side switch), whereas in buck topology the switch source terminal floats on the switching node (Kularatna

2008:108). It is usually operated in CCM to reduce the peak currents and does not have the stability problem of the flyback converter. Figure 18 shows the waveforms associated with the forward converter.

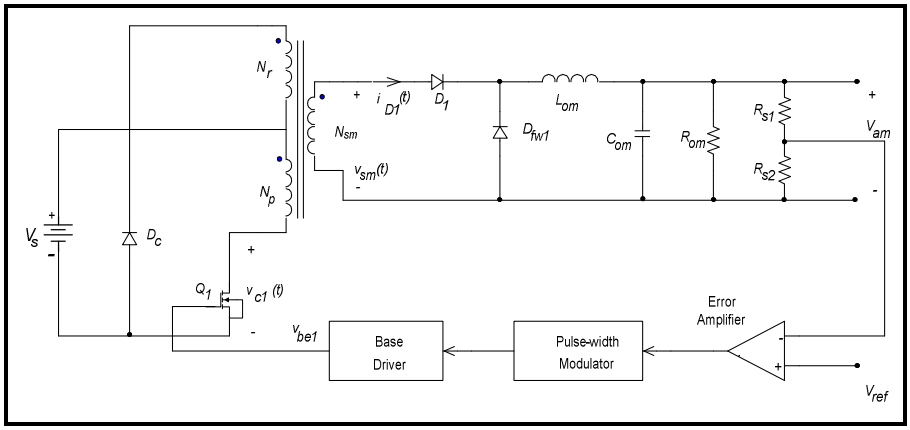



**Figure 17: Forward converter topology**

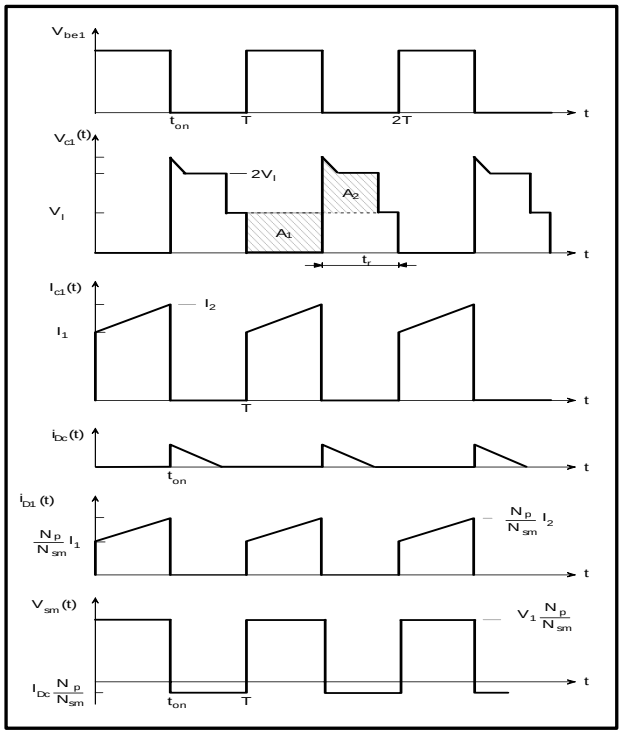



**Figure 18: Voltage and current waveforms of the forward converter (Ang & Oliva 2005:133)**

The output voltage is calculated by means of the equation:

$$V_o = D \cdot n \cdot V_s \tag{9}$$

The high frequency (HF) transformer transfers energy directly to the output with very little stored energy. The output capacitor size and peak current rating are smaller than they are for the flyback. A reset winding is required to remove the stored energy in the transformer. Maximum duty cycle is about 0.45 and limits the control range (Dorf 2006:9-20).

The main advantage of the forward topology is that it provides isolation and the capability to provide a step-up or step-down function (Kularatna 2008:108). Additionally, it has the advantage of having a low output ripple voltage.

The main limitation of the topology eventually comes about, rather, from the available size of MOSFETs. Increased power translates into increased currents and eventually losses in the MOSFETs become unacceptable. When this is the case, a topology with more than one transistor to share the burden is desirable (Lenk 2005:31). It also has a poor transient response and its efficiency is low owing to poor transformer utilisation.

#### 2.6.2.3 Push-pull converter

A push-pull topology is shown in Figure 19. This converter is used to produce a square-wave AC signal at the input of the high-frequency transformer. The square wave is then fed to the transformer in order to step-up or step-down the voltage. Finally, this voltage is rectified by output diodes to get a DC output. The duty ratio of each switch in a push–pull is less than 0.5. Since there are two switches, which work alternately, the output voltage is doubled.

The output voltage is calculated with the formula:

$$V_o = 2 \cdot D \cdot n \cdot V_s \tag{10}$$

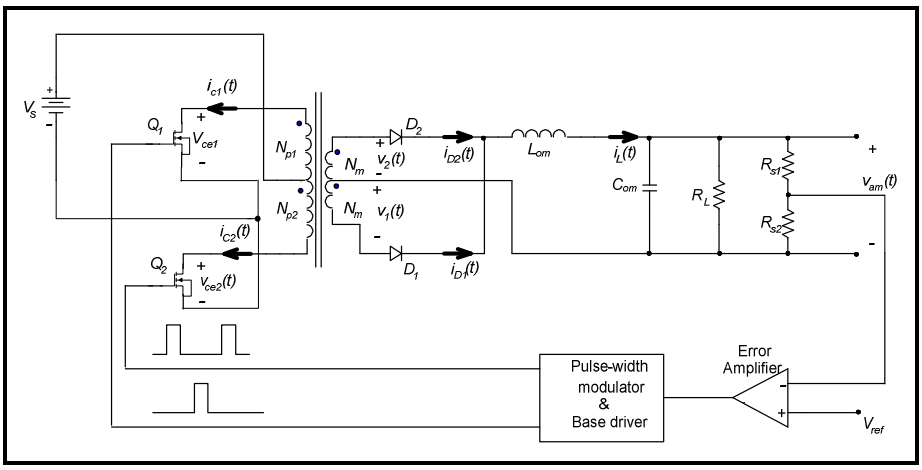



**Figure 19: Push-pull converter topology**

Each secondary delivers a pair of 180º out-of-phase square-wave power pulses whose amplitude is fixed by the input voltage and the number of primary and secondary turns (Pressman *et al.* 2009:45). The waveforms within a push-pull converter are given in Figure 20.

A push-pull converter is used to reduce the conduction loss in switches by operating only one switch at any time to interface the FC voltage to the DC bus. But the major problem is the transformer saturation which results in converter failure because the two half portions of the centre-tapped transformer windings cannot be equally or symmetrically wound. Therefore the push-pull converter is suitable for low and medium power applications only (Kuribakaran *et al.* 2009:2437).

Two of the advantages are that the transformer flux swings fully and thereby the size of the transformer is much smaller (typically half the size) than single-ended converters and output ripple is twice the switching frequency of the transistors, therefore needing smaller filters. Some of the disadvantages of this configuration are that the transistors must block twice the supply voltage, flux symmetry imbalance can cause transformer saturation with special control circuitry required to avoid this

problem and use of a centre-tap transformer requires extra copper resulting in a higher volt–ampere (VA) rating. Current mode control (for the primary current) can be used to overcome the flux imbalance. This configuration is used in the 100 to 500 W output range (Dorf 2006:9-21).

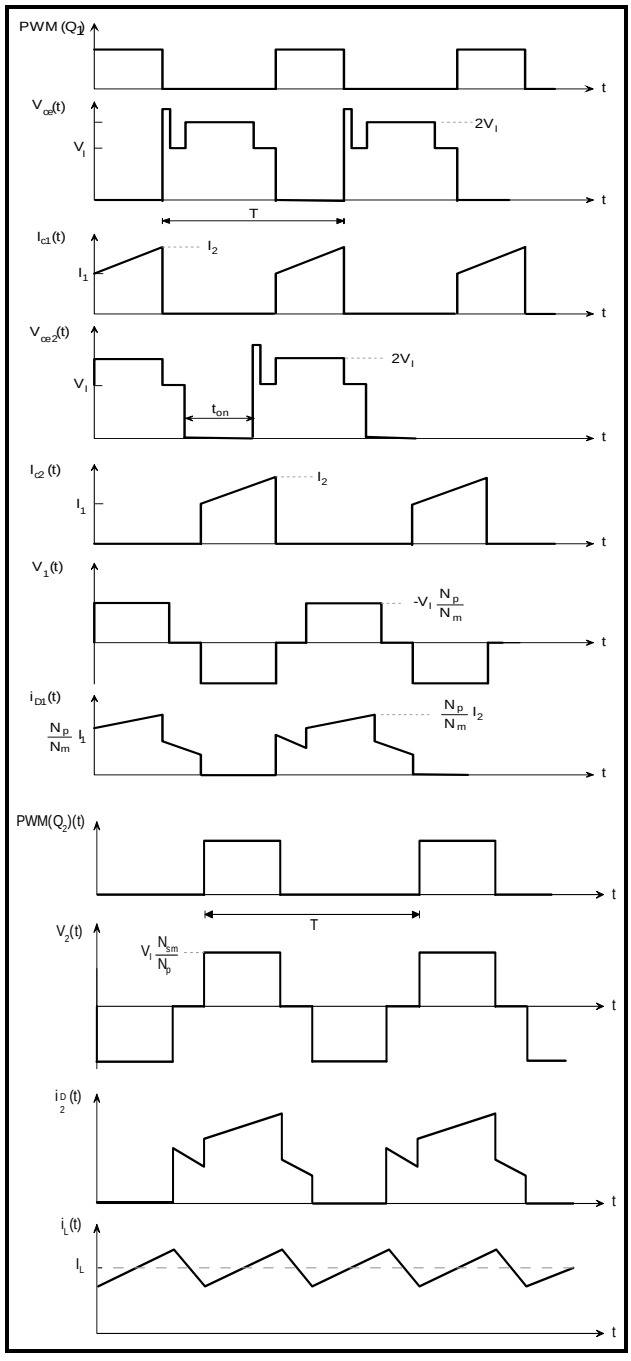



**Figure 20: Push-pull topology waveforms (Ang & Oliva 2005:138,139)**

### 2.6.2.4 Weinberg converter

The Weinberg converter is a push-pull converter with an inductor in series with the input power source as shown in Figure 21.

Basu (2007:336) explains that using an input and output magnetic coupling, the Weinberg converter overcomes the strict switching requirements for a voltage-fed push-pull converter. Further, no output inductor is employed. Nonetheless, the Weinberg converter is also susceptible to voltage spikes owing to the existence of leakage inductance in not only the centre-tapped transformer but also the input magnetics.

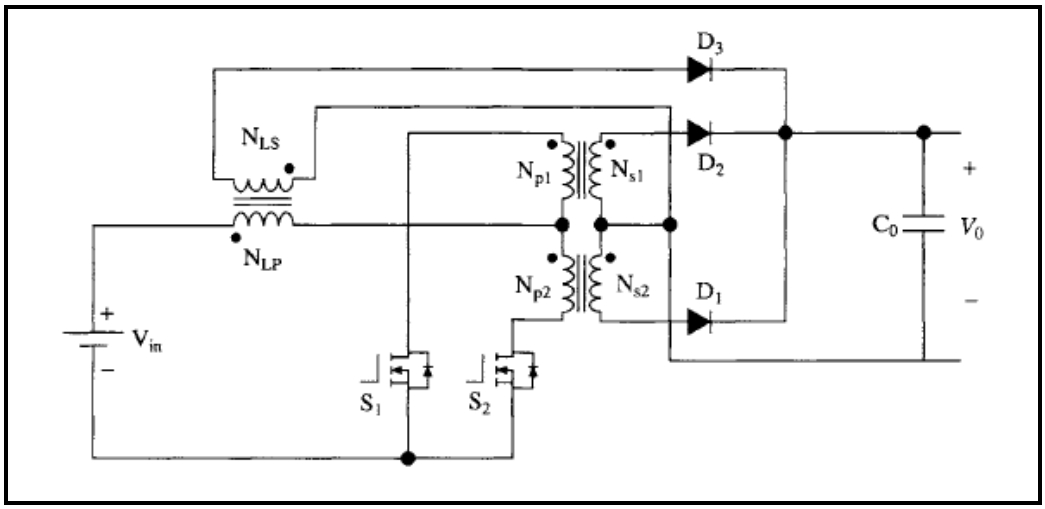



**Figure 21: Weinberg converter topology (Basu 2007:337)**

### 2.6.2.5 Half-bridge converter

As depicted in Figure 22, in the half-bridge configuration a centre-tapped DC source is created by two smoothing capacitors ($C_{11}$ and $C_{12}$), and this configuration utilizes the transformer core efficiently. The voltage across each transistor is equal to the supply voltage (half of push–pull) and, therefore, suitable for high voltage inputs. The equation for the half-bridge converter output voltage is:

$$V_o = D \cdot n \cdot V_s \tag{11}$$

The disadvantage of this configuration is the requirement for large-size input filter capacitors. The half-bridge configuration is used for power levels on the order of 500 to 1000 W (Dorf 2006:9-21). The ideal waveforms of the half-bridge converter are given in Figure 23.

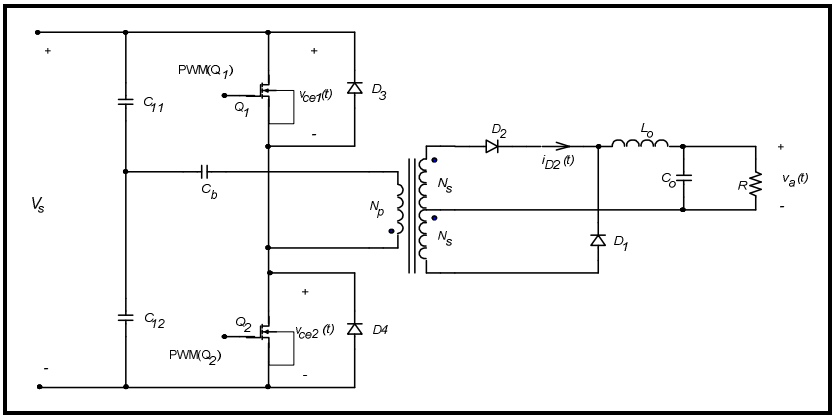



**Figure 22: Half-bridge topology**

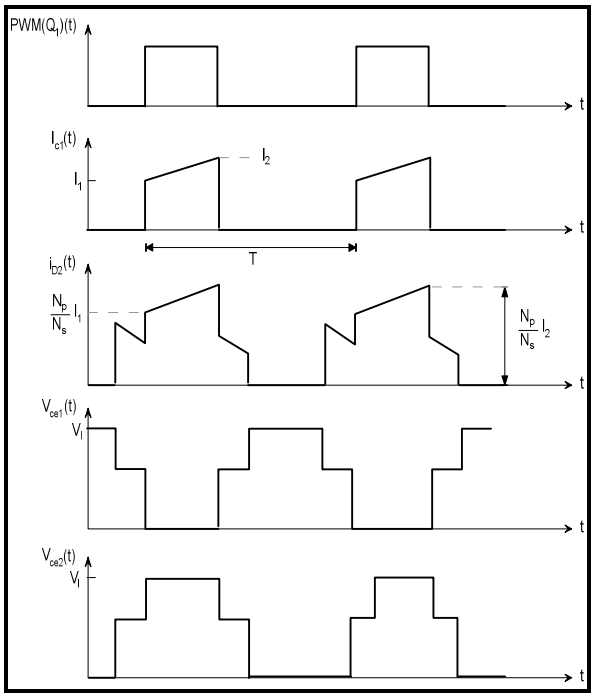



**Figure 23: Waveforms of the half-bridge converter (Ang & Oliva 2005:142)**

### 2.6.2.6 Full-bridge converter

The full-bridge converter, as shown in Figure 24, is the most frequently implemented circuit configuration for FC power conditioning when electrical isolation is required (Yu *et al.* 2007:647). The output voltage is calculated according to the formula:

$$V_o = 2 \cdot D \cdot n \cdot V_s \tag{12}$$

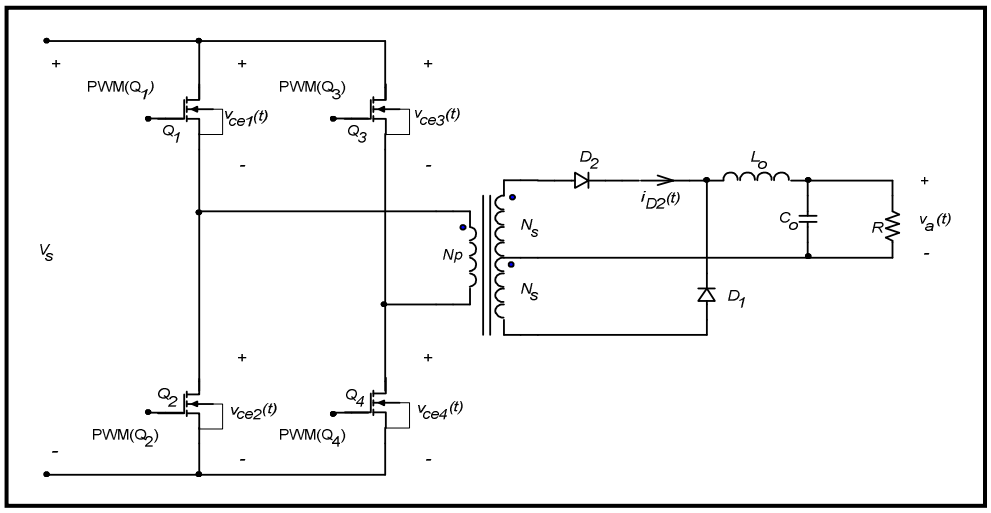



**Figure 24: Full-bridge topology**

The full-bridge converter is well developed and frequently used for FC applications. The main advantage of this topology is its short-circuit protection and it does not have transformer saturation problems (Cheng, Sutanto, Ho & Law 2001:2201).

One of the salient features of a full-bridge converter is that, by using a proper control technique, it can be operated in zero-voltage switching (ZVS) mode, which results in negligible switching losses. However, at reduced load currents, the ZVS property is lost. Recently, there has been a lot of effort made to overcome this problem. Full-bridge topology is used for very high-power applications. The use of this topology requires the consideration of losses in the circuit and the design complications due to high-side switches operating with their source terminals (in the case of MOSFETs)

or emitters (in IGBTs or power transistors) at floating levels (Kularatna 2008:129). Typical waveforms of the full-bridge converters are shown in Figure 25.

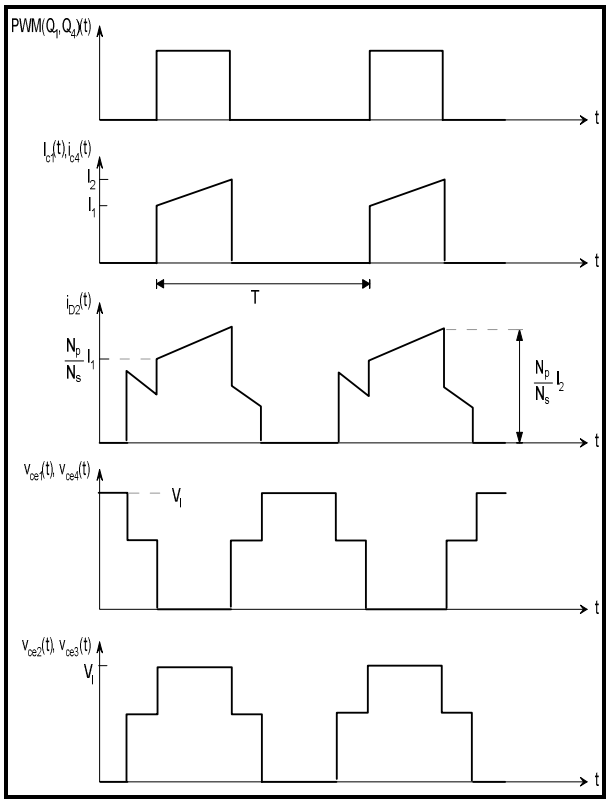



**Figure 25: Waveforms of a full bridge topology (Ang & Oliva 2005:145)**

### 2.6.3 Specialised DC–DC converters for FCs

Although conventional DC–DC converters are often implemented in FC applications, not all of the problems encountered with FC conditioning have been resolved (Yu *et al.* 2007:647).

In the following sections, some DC–DC converters designed specifically for application in FC power conditioning are the following:

- **Multiphase isolated boost converter:** the circuit schematic of a multiphase isolated boost converter is shown in Figure 26. The circuit consists of twelve

controlled switches ($S_1$-$S_{12}$) and six diodes ($D_1$-$D_6$) to generate a DC voltage output. Because the current is shared by three phases, the current stress on each device reduces. As a result, the problems of diode recovery and higher switch and diode losses are substantially alleviated. Also, because the topology is a buck-derived type of converter, the controller implementation is simplified (Basu 2007:335).

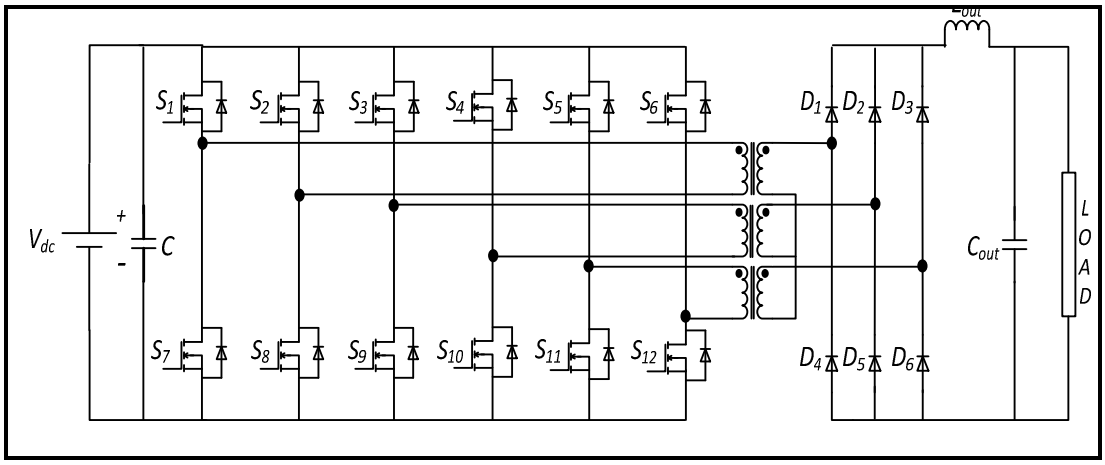



**Figure 26: Multiphase isolated boost converter (Basu 2007:335)**

- **Isolated Çuk converter:** The isolated Çuk converter in Figure 27 steps up the input voltage to a high intermediate DC voltage and provides galvanic isolation as well. The isolated Çuk converter attains fewer components, enables integrated magnetics leading to low input and output current ripples and lower electromagnetic interference (EMI) as compared to other conventional isolated step-up converters. The magnetic integration yields significant savings in weight and volume as well. However, because the current through the transformer sees an almost instantaneous change owing to the switching of $S_1$, the leakage inductance of the Çuk converter has to be really low, otherwise, the voltage spike across $S_1$ (and $S_2$) could potentially destroy the device. A higher voltage rating of $S_1$ ($S_2$) leads to higher losses. Non-dissipative (resonant) or dissipative snubbers (RC and RCD) can be used to overcome the voltage spike problem. Also, a resonant clamp circuit across

the transformer primary can be used to clamp the voltage overshoot to a predetermined value. However, all of these options have a drawback from the standpoint of efficiency (Basu 2007:335-336).

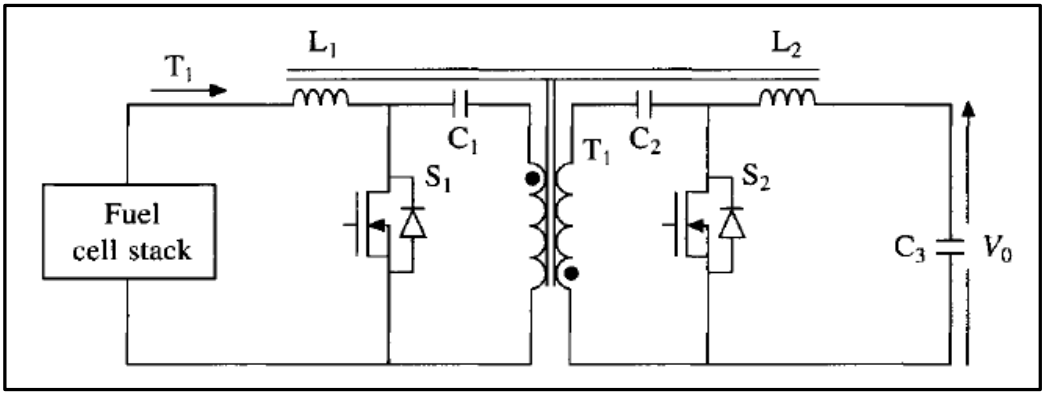



**Figure 27: Schematic of the isolated Çuk converter with integrated magnetics (Basu 2007:336)**

- **Full-bridge converter with multiple secondary coils:** According to Yu *et al.* (2007:647) the full-bridge converter with multiple secondary coils (shown in Figure 28) utilises a transformer with multiple secondary coils connected in series. This full-bridge converter topology has the capability to achieve ZVS allowing for high-efficiency operation. Furthermore, if the correct control algorithm is implemented, this converter topology can shift the phase as much as 180°, thus regulating the output voltage. This converter also has the capability to operate either under constant-voltage mode or constant current affording flexibility for the designer.

  To control the amount of voltage gain, the converter utilises electromechanical relays in the transformer secondary coils that manipulate the transformer turns ratio. Through this methodology, if the FC's stack voltage decreases because of increasing load, a higher transformation ratio can be chosen to maintain the output voltage.

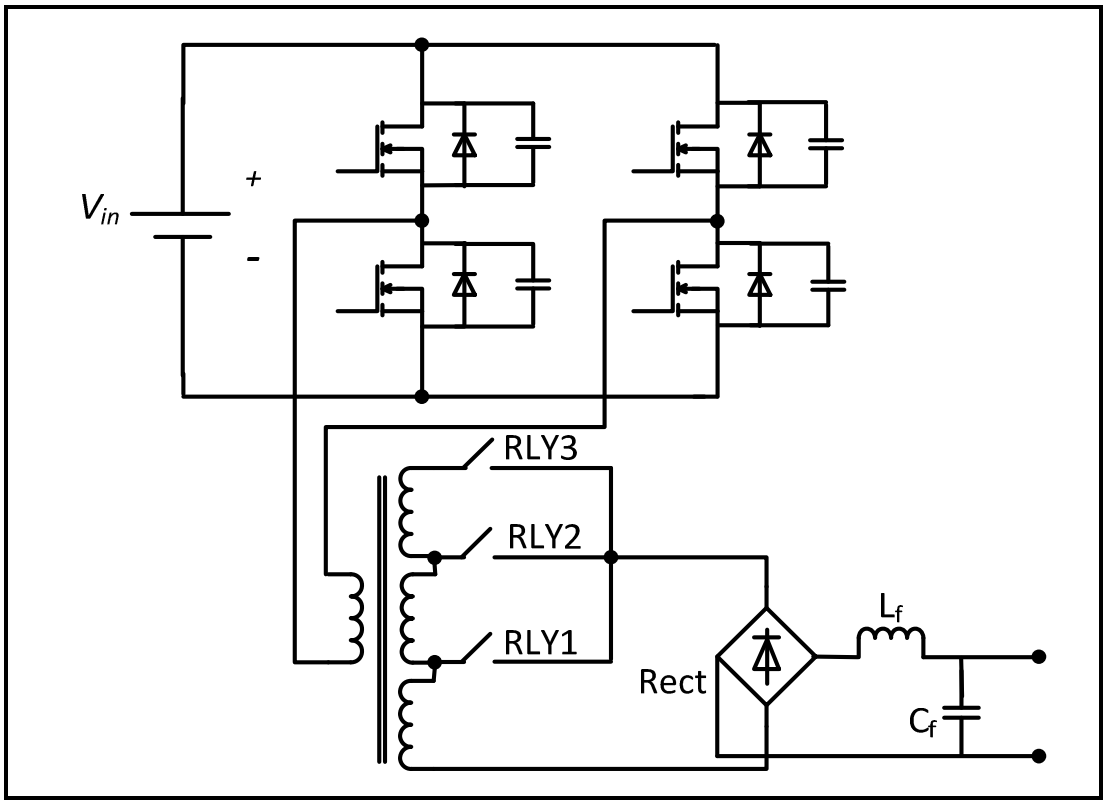



**Figure 28: Full-bridge converter with multiple secondary coils (Yu *et al.* 2007:647)**

### 2.6.4 Interleaved multiphase converters

According to Ang and Oliva (2005:321) a parallel connection of switching converters results in what is called interleaved converters. Compared to single power stage converters these converters offer numerous advantages such as:

- Low current ripple on the input and output capacitors,
- Fast transient response to load changes,
- Improved power handling capabilities at greater than 90 percent efficiency.

Interleaved converters are used in applications with low ripple such as the new generation of personal computers and switching audio amplifiers (Ang & Oliva 2005:321).

According to Eirea and Sanders (2008:137) this topology has some drawbacks such as the fact that it requires more components and a more complex controller. Additionally, it suffers from current unbalance. This occurs when there exist small variations in the characteristics of each channel and this situation generates a significant current unbalance. This needs to be looked at closely because many advantages of the multiphase topology are lost if currents in each phase are unbalanced.

## 2.7 Choice of topology

Topology selection is a crucial task because all other design selections such as component selection, magnetic design, loop compensation and so on depend on it. If the topology changes, these must change as well. So before getting started, it is always a good idea to spend some time, carefully looking at the power supply's requirements and specifications to ensure that a proper topology is selected (Lenk 2005:17).

Furthermore, it is essential to be familiar with the merits, drawbacks and areas of usage of all converter topologies. Table 1 summarizes the merits and as well as the drawbacks of some of the converter topologies examined. It is very important to select the right converter in order to achieve the maximum utilisation of the FC energy and to minimise losses. The investigation on design considerations of FC and PAFC converter systems made possible the establishment of the requirements for the DC–DC converter so that design choices can be made upfront. Making a proper choice at the beginning is vastly less costly and time-consuming than trying to make corrections later (Lenk 2005:22).

**Table 1: Comparison of converter topologies (Kularatna 1997:68)**

| Topology | $V_{in}$ /$V_{out}$ | Advantages | Disadvantages | Typical Application Environment | Typical Efficiency (%) |
|---|---|---|---|---|---|
| Buck | *D* | High efficiency, simple, low switch stress, low ripple | No isolation, potential over-voltage if switch shorts | Small-sized imbedded systems | 78 |

**Table 1: Comparison of converter topologies (Kularatna 1997:68) continued**

| Topology | $V_{in}/V_{out}$ | Advantages | Disadvantages | Typical Application Environment | Typical Efficiency (%) |
|---|---|---|---|---|---|
| Boost | *1/( 1-D)* | High efficiency, simple, low input ripple current | No isolation, high switch peak current, regulator loop hard to stabilise, high output ripple, unable to control short circuit current | Power-factor correction, battery up-converters | 80 |
| Buck-boost | *-(D/1-D)* | Voltage inversion without a transformer, simple, high frequency operation | No isolation, regulator loop hard to stabilise, high output ripple | Inverse output voltages | 80 |
| Flyback | *n·D/(1-D)* | Isolation, low parts count, has no secondary output inductors | Poor transformer utilisation, high output ripple, fast recovery diode required | Low output power, multiple output | 80 |
| Push-pull | *2·n·D* | Isolation, good transformer utilisation, good at low input voltages, low output ripple | Cross conduction of switches possible, high parts count, transformer design critical, high voltage required for switches | Low output voltage | 75 |
| Half-bridge | *n·D* | Isolation, good transformer utilisation, switches rated at the input voltage, low output ripple | Poor transient response, high parts count, cross conduction of the switches possible | High input voltage, moderate to high power | 75 |
| Full-bridge | *2·n·D* | Isolation, good transformer utilisation, switches rated at the input voltage, low output ripple | High parts count, cross conduction of switches possible | High power, high input voltage | 73 |

When comparing the efficiencies presented in Table 1 with the target efficiency for FC's DC–DC converters (which should be greater than 85 percent), it is clear that these efficiencies are too low. In order to achieve higher efficiencies, a multiphase synchronous buck converter circuit topology can be used. This topology will be expounded in the next chapter.

## 2.8 Summary

This chapter presented some facts regarding the PAFC. It also highlighted the broad range of DC–DC converters which can be used with FCs although this list is not comprehensive. Conventional and some specific converters used with FC technology were reviewed. In Chapter 3, the design procedure of the proposed DC–DC converter is presented.

# Chapter 3 Design aspects of the converter

## 3.1 Introduction

The choice of the most suitable DC–DC converter for a specific application may prove to be a daunting challenge (Nowakowski & Tang 2009:15). In the case of FCs, the requirement for greater efficiency is a typical issue. Kuyula and van Rensburg (2012) presented the experimental results of the development of a push-pull converter for FC applications with 63 percent efficiency at the SATNAC 2012 conference held at Fancourt, George, South Africa. Because FCs are used where conversion efficiency is a key requirement, another topology with the possibility of achieving more than 90 percent efficiency was selected. Achieving high energy conversion efficiency by means of a switching regulator is key to prolong a FC's life and improve its power reliability (Basu 2007:333). Most applications in telecommunications today, require DC–DC converters capable of regulating a relatively low output voltage at increasing load currents from a wide range of input voltages while meeting efficiency requirements (National Semiconductor 2010). Taking this trend into account, Chapter 3 presents a design of a 200 W converter using an interleaved multiphase synchronous buck topology. The hardware construction is shown as well.

## 3.2 Interleaved multiphase synchronous buck converter

According to Hegarty (2007) a poly-phase or multiphase synchronous buck converter is a suitable topology for various applications. In recent decades, interleaved multiphase buck converters have received considerable attention with regard to applications in computing. This topology has found its way into many other spheres such as telecommunications and others. Depicted in Figure 29 is a *N*-phase synchronous buck converter. It consists of *N* synchronous buck converters (two or more single phase converters) operated in parallel feeding the same filter capacitor and load. (Kazimierczuk 2008:77).

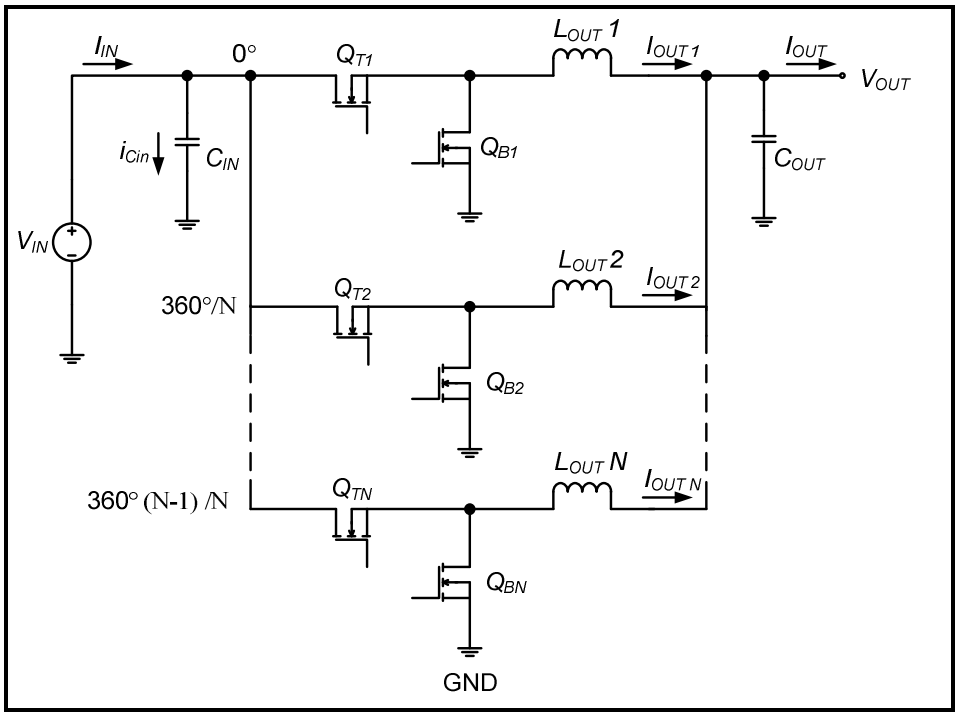



**Figure 29: *N*-phase interleaved buck converter (Hegarty 2007)**

This topology has the following advantages (Hegarty 2007):

- Minimum EMI filtering requirements,
- Excellent transient response,
- High efficiency,
- Small size and low cost,
- The effective switching frequency is multiplied by the number of phases while the load current is divided by the number of phases.

## 3.3 Operation of the multiphase synchronous buck converter

Before explaining the operation of this topology, it is fitting to understand what a synchronous buck converter is. A noticeable difference between a conventional buck converter and a synchronous buck converter is the substitution of the freewheeling diode by a second switch as illustrated in Figure 30. This results in an improvement

of the efficiency of the buck converter. The diode that is replaced by the second switch, is accountable for substantial losses leading to poor efficiency of the buck converter (Hart 2011:207). The connecting point where the two switches and inductor of a switching converter meet is called the switch node.

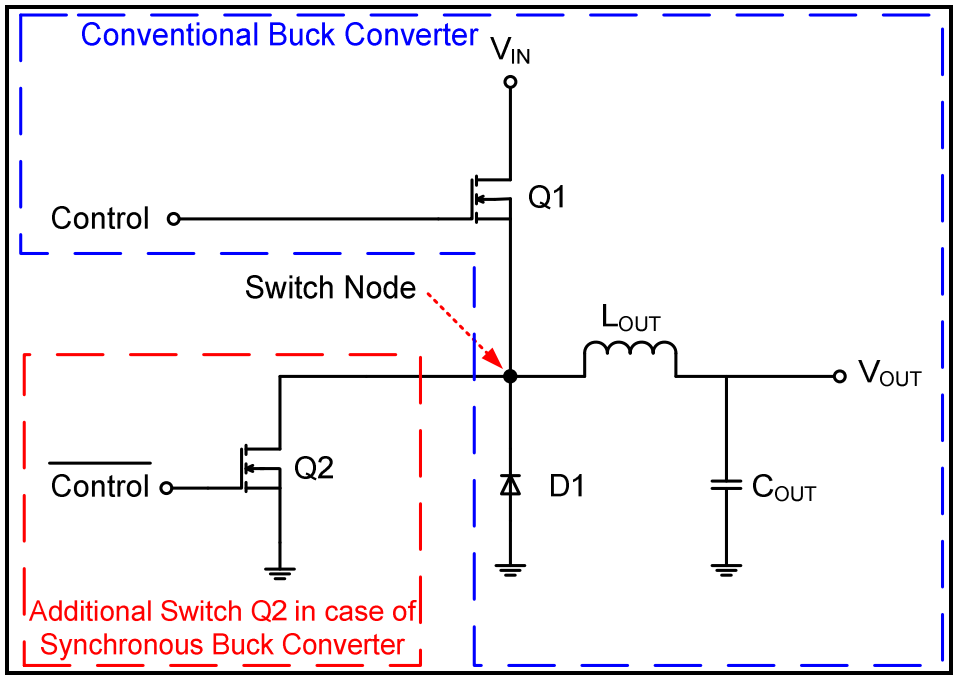



**Figure 30: Synchronous and nonsynchronous buck circuits (Nowakowski & Tang 2009:15)**

To illustrate how the multiphase synchronous buck converter works, a two-phase interleaved buck converter is shown Figure 31. The boxes with dashed lines represent the individual phases. In other words each phase corresponds to one synchronous buck converter.

The duty cycle *D* is expressed as:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{13}$$

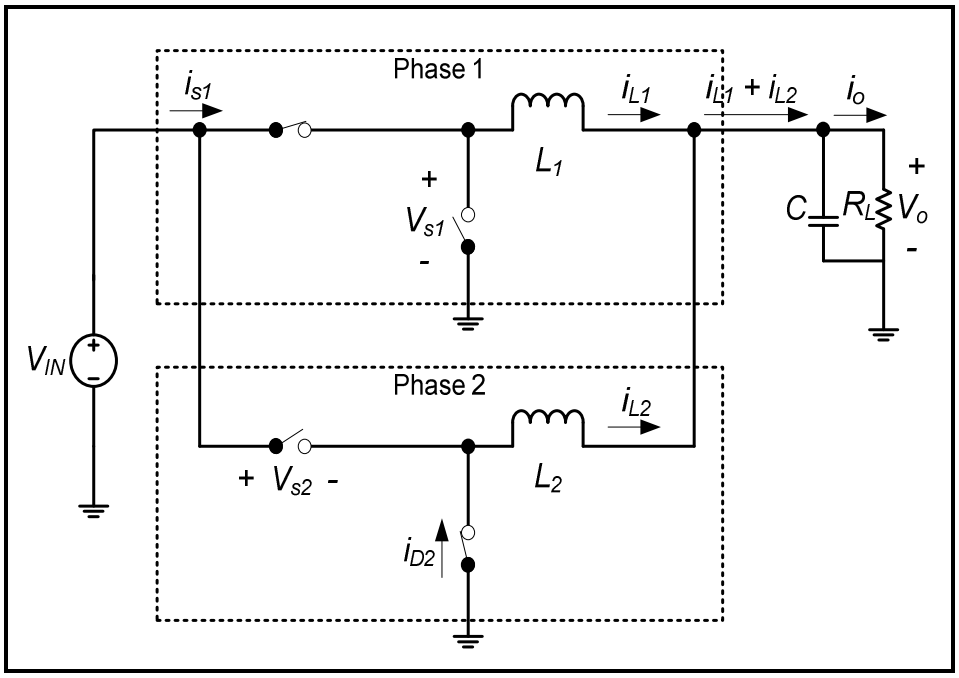



**Figure 31: Two-phase interleaved buck converter (Kazimierczuk 2008:78)**

The waveforms of a two-phase buck converter are shown in Figure 32. The control drive signals $V_{GS1}$ and $V_{GS2}$ are separated from each other by a 180° phase. For this topology, the output voltage ripple is reduced considerably owing to ripple cancellation when each phase of the converter is switched complementarily (Kazimierczuk 2008:78).

Furthermore, according to Kazimierczuk (2008:78) in a two-phase buck converter, the sum of $i_{L1}$ and $i_{L2}$ is a constant at duty cycle $D = 0.5$. The AC component of the sum of the two currents is zero. Hence, this results in a zero ripple voltage as the AC component of the current through the filter capacitor is zero. However, partial ripple cancellation occurs at $D \neq 0.5$.

It is important to mention that a dead time is required to avoid simultaneous conduction of high-side and low-side switches. During this time both high-side and low-side switches are OFF (Perutka 2011:161).

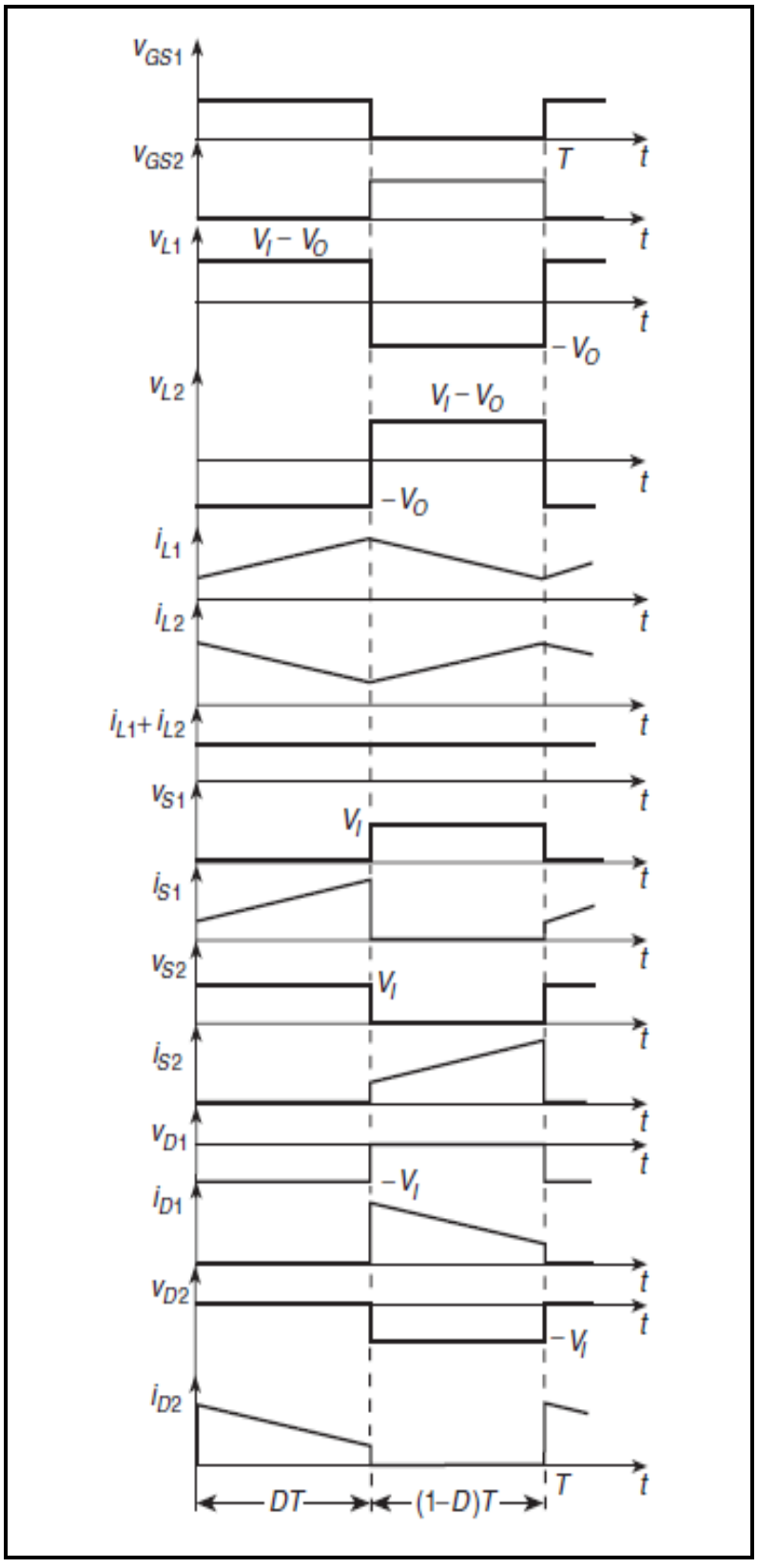



**Figure 32: Waveforms in two-phase buck converter (Kazimierczuk 2008:79)**

## 3.4 Specifications

The first step in any successful design is to determine the power supply specifications (Brown 2001:5). The following specifications are used for the design of the prototype:

- Input DC voltage range: 22 – 46 V
- Output DC voltage: 13.8 ± 0.5V at 1 A – 14 A
- Efficiency: > 85 percent

## 3.5 Webench® designer

The Webench® Designer (online software package from Texas Instruments) was used to design the converter. The converter specifications were entered in the software as shown in Figure 33.

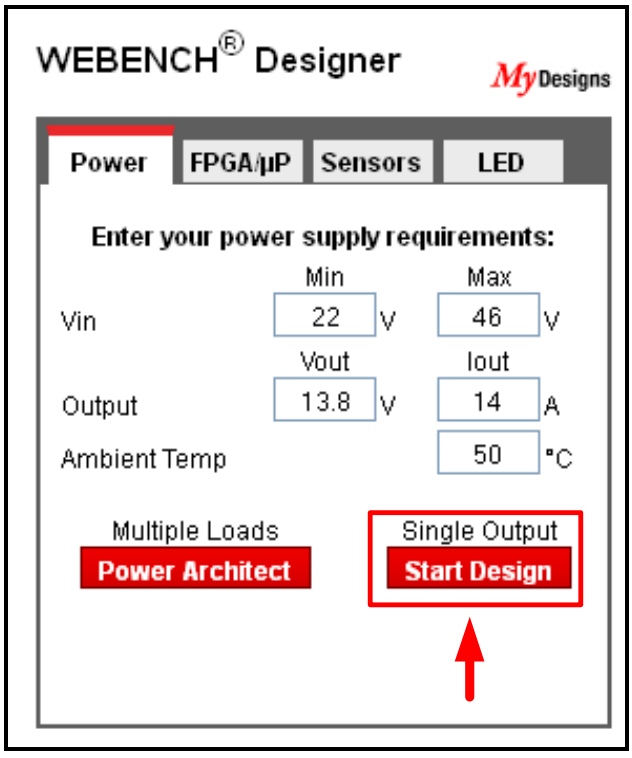



**Figure 33: Specifications entered in Webench® Designer**

Figure 34 shows the suggested design solution in Webench® Designer. The PWM controller proposed for this design was the LM5119 from National Semiconductor. Additionally, a basic schematic is provided as well as other design considerations such as the bill of materials, type of topology, efficiency, the operating frequency and so on.

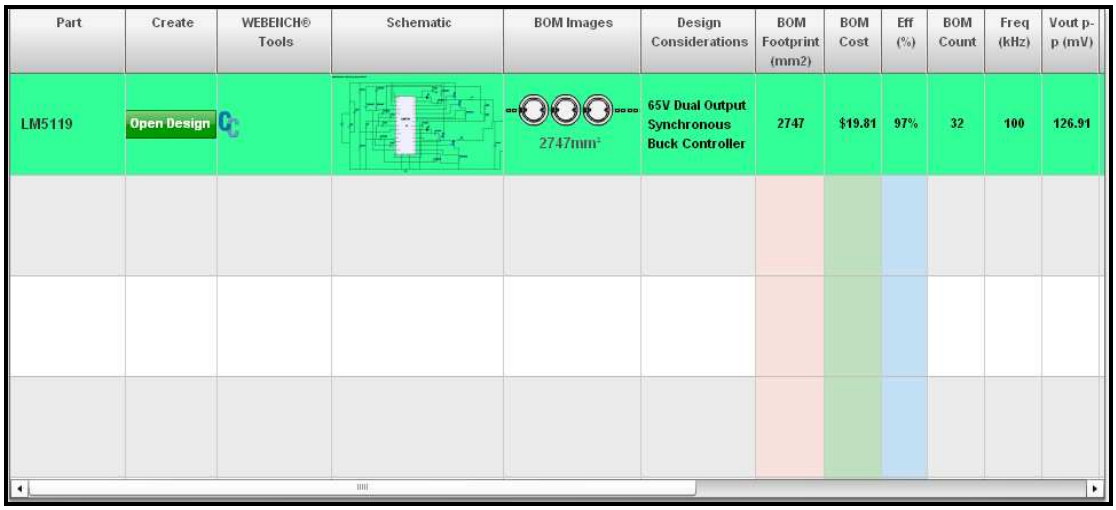



**Figure 34: Webench® Designer solution for a synchronous buck converter with the LM5119**

As it can be seen from Figure 34, the design using the LM5119 achieves a higher efficiency (97 percent) and it has a low peak-to-peak output ripple voltage (126 mV). Besides, the circuit is relatively small in size. Hence, the LM5119 synchronous buck controller was selected for the DC–DC converter to be used in conjunction with the PAFC.

### 3.6 LM5119 controller

The LM5119 is a dual-phase or dual channel synchronous buck controller intended for step-down regulator applications for a high voltage or widely varying input supply (See Annexure B). It has several interesting features such as a wide $V_{in}$ range, multiphase operation, programmable soft-start and diode emulation mode (DEM).

Additional features include thermal shutdown, cycle-by-cycle and hiccup mode current limit and adjustable line under-voltage lockout (UVLO). All these characteristics give the designer a variety of options for control of all applications (Pur 2010). For more details on the LM5119 controller see Annexure B.

The LM5119 is available in 5 mm by 5 mm 32-pin LLP package (National Semiconductor 2010). Figure 35 depicts the actual size of the LM5119 and next to it is a South African five cent coin which has diameter of 21 mm.

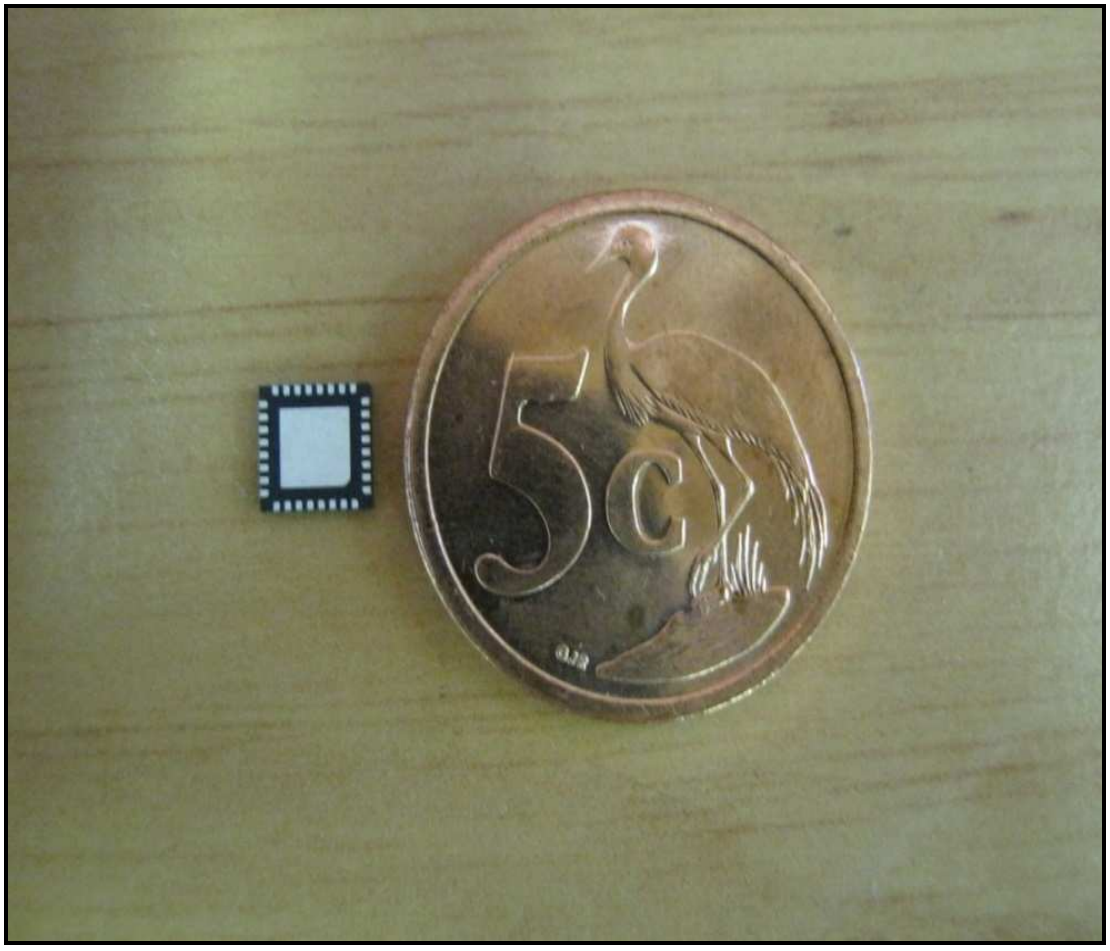



**Figure 35: Size of the LM5119 Controller**

## 3.7 Design calculations

Based on the LM5119 datasheet (see Annexure B) the following parameters were calculated.

### 3.7.1 Oscillator frequency

$R_T$ is used to set the switching frequency of each regulator phase or channel. However, the oscillator frequency is twice the switching frequency. The converter's oscillator frequency can be adjusted by means of $R_T$. Its value is calculated using the following formula, obtained from the LM5119 datasheet (see Annexure B):

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948 \tag{14}$$

The frequency selected for this design was 230 kHz. Thus the value of $R_T$ is calculated:

$$R_T = \frac{5.2 \times 10^9}{230 \times 10^3} - 948 = 21.7 \times 10^3\ \Omega$$

The value of $R_T$ used for the prototype is 22 kΩ.

### 3.7.2 Choice of output inductor per phase

The inductor value is determined using the operating frequency $f_{SW,}$ ripple current $I_{PP}$, the maximum input voltage $V_{IN(MAX)}$ and output voltage $V_{OUT}$ according to the following equation:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \tag{15}$$

Taking into account that the maximum ripple current is generally between 20 and 40 percent of the total load current, for this design a 15 percent current ripple of the output current $I_{OUT}$ was assumed. The reason behind this assumption is to avoid putting unnecessary burden on the output capacitor $C_{OUT}$. On the contrary, $C_{OUT}$ will have to smooth a consistent amount of ripple current.

Since $I_{OUT}$ is 7 A per phase, the ripple current $I_{PP}$ is calculated as follows:

$$I_{PP} = \frac{15 \times I_{OUT}}{100} = \frac{15 \times 7\ \text{A}}{100} = 1.05\ \text{A}$$

Hence, according to Equation (15) the inductor value is:

$$L = \frac{13.8\ \text{V}}{1.05\ \text{A} \times 230 \times 10^3\ \text{Hz}} \times \left(1 - \frac{13.8\ \text{V}}{46\ \text{V}}\right) = 31.1 \times 10^{-6}\ \text{H}$$

The closest standard inductor value selected per channel was a 33 µH, 12 A from Wurth Elektronik with a tolerance of 15%.

### 3.7.3 Current sense resistor

According to National Semiconductor (Annexure B) prior to determining the value of the current sense resistor $R_S$, it is essential to understand the K factor notion, which is defined as the ramp slope multiple chosen for slope compensation. It is common practice that the K factor is varied from 1 to 3 and it is expressed as:

$$K = \frac{L}{10 \times R_S \times R_{RAMP} \times C_{RAMP}} \tag{16}$$

It is important to mention that the K factor has a bearing on the performance. Table 2 gives a summary of how this notion affects the converter performance. For this design, a K factor of 2.5 was selected.

**Table 2: Performance variation owing to K factor**

| | **K < 1** | **1 ← K → 3** | | **K > 3** |
|---|---|---|---|---|
| **Peak inductor current with short output condition** | Subharmonics oscillation may occur | Lower | Higher | Introduces additional pole near cross-over frequency |
| **Inductor Size** | | Smaller | Larger | |
| **Power dissipation fo $R_S$** | | Higher | Lower | |
| **Efficiency** | | Lower | Higher | |

The current sense resistor value is calculated using the equation:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(MAX)} + \frac{V_{OUT} \times K}{f_{SW} \times L} - \frac{I_{PP}}{2}} \tag{17}$$

where $V_{CS(TH)}$ ≡ Current limit threshold voltage,

$K$ ≡ K factor,

$I_{OUT(MAX)}$ ≡ The maximum current capability.

The maximum current capability needs to be 20-50 percent higher than the required output current to account for tolerances and ripple current. Therefore, for this design, a 120 percent of 7 A (8.4 A) was chosen to ensure safe operation.

Calculating $R_S$ using equation (17):

$$R_S = \frac{0.12}{8.4\ \text{A} + \frac{13.8\ \text{V} \times 2.5}{230 \times 10^3\ \text{Hz} \times 33 \times 10^{-6}\ \text{H}} - \frac{1.05\ \text{A}}{2}} = 10 \times 10^{-3}\ \Omega$$

A current resistor of 10 mΩ was used because it was available.

### 3.7.4 Ramp resistor and ramp capacitor

To enable full discharge of the LM5119 internal switch between cycles, the capacitor $C_{RAMP}$ should be of a good quality, thermally stable ceramic capacitor with a 5 percent or less tolerance as recommended and it should be not more than 2 nF.

The value of the ramp capacitor was chosen to be 820 pF.

With the ramp capacitor selected as well as the *K* factor, the sense resistor and output inductor calculated, the ramp resistor is calculated using the equation:

$$R_{RAMP} = \frac{L}{10 \times R_s \times K \times C_{RAMP}} \tag{18}$$

Hence the value of ramp is:

$$R_{RAMP} = \frac{33 \times 10^{-6}\ \text{H}}{10 \times 0.01 \times 2.5 \times 820 \times 10^{-12}\ \text{F}} = 161 \times 10^{3}\ \Omega$$

A ramp resistor of 200 kΩ was used instead of the calculated one. The reason for this choice is that the 200 kΩ is in the range of resistors that can be used according to Webench® Designer.

### 3.7.5 Output capacitors

The role of the output capacitor is to smooth the inductor ripple current. A 470 uF, 25 V surface mount electrolytic capacitor from KJ Electronics was selected. To negate the output voltage ripple and spikes, two 22 uF low ESR and ESL capacitors are connected in parallel with $C_{OUT}$ for each channel.

### 3.7.6 Output voltage divider

Figure 36 highlights the output voltage divider of the voltage feedback loop. To obtain an output voltage of 13.8 V, the values of $R_{FB2}$ and $R_{FB1}$ needed to be determined.

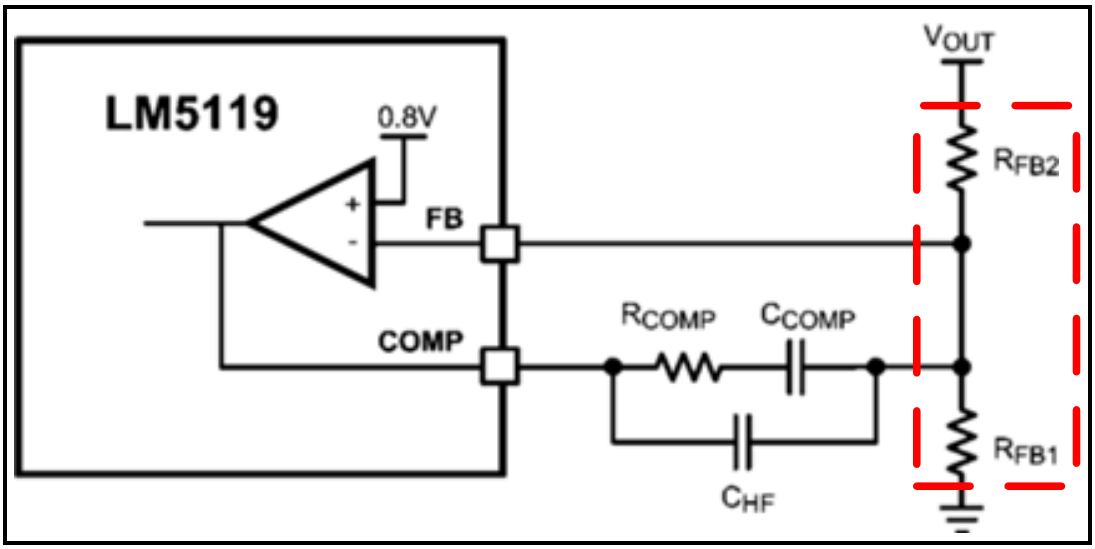



**Figure 36: Output voltage divider of the converter feedback loop**

The ratio of these resistors is calculated from the following equation:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8\ \text{V}} - 1 \tag{19}$$

Hence the ratio of $R_{FB2}$ and $R_{FB1}$ is:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8\ \text{V}} - 1 = \frac{13.8\ \text{V}}{0.8\ \text{V}} - 1 = 16.25$$

In order to obtain a 13.8 V output voltage for this design, the value of $R_{FB2}$ was chosen to be 19.1 kΩ which results in a $R_{FB1}$ value of 1.18 kΩ calculated as follows:

$$R_{FB1} = \frac{R_{FB2}}{16.25} = \frac{19.1\ \text{k}\Omega}{16.25} = 1.18\ \text{k}\Omega$$

### 3.7.7 Error amplifier compensation

In order to configure the error amplifier gain characteristics so as to achieve a stable voltage, the network consisting of $R_{COMP}$, $C_{COMP}$ and $C_{HF}$ is required (See Figure 37). However, only $R_{COMP}$ and $C_{COMP}$ are needed to close the voltage loop and improve the phase margin of the voltage loop with increased stability. The voltage loop gain is the product of the modulator gain and the error amplifier gain.

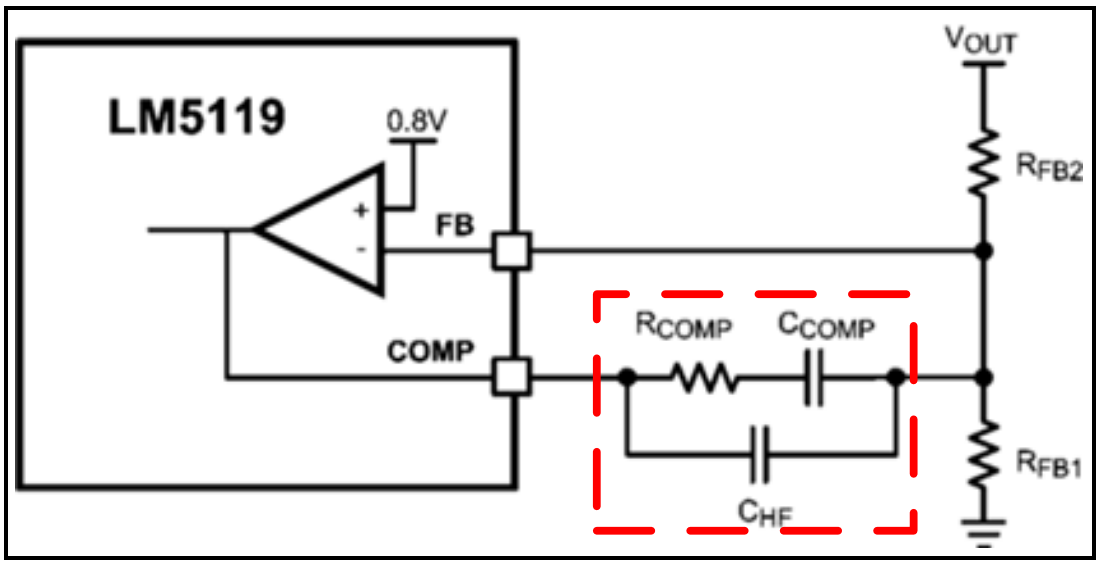



**Figure 37: Error amplifier compensation network**

The DC modulator gain of the LM5119 is modeled as follows:

$$DC\_GAIN_{(MOD)} = \frac{R_{LOAD}}{(A \times R_S)} \quad (20)$$

where $A \equiv$ Gain of the current sense amplifier (For the LM5119, A = 10),

$R_{LOAD} \equiv$ Ratio of $V_{OUT} / I_{OUT}$

The dominant low frequency pole of the modulator is determined by the load resistance $R_{LOAD}$ and the output capacitor $C_{OUT}$. The corner frequency of this pole is obtained by means of the equation:

$$f_{P(MOD)} = \frac{1}{(2\pi \times R_{LOAD} \times C_{OUT})} \tag{21}$$

Hence, $R_{LOAD} = \frac{13.8\ \text{V}}{7\ \text{A}} = 1.971\ \Omega$,

The total output capacitance $C_{OUT}$ = 514 uF,

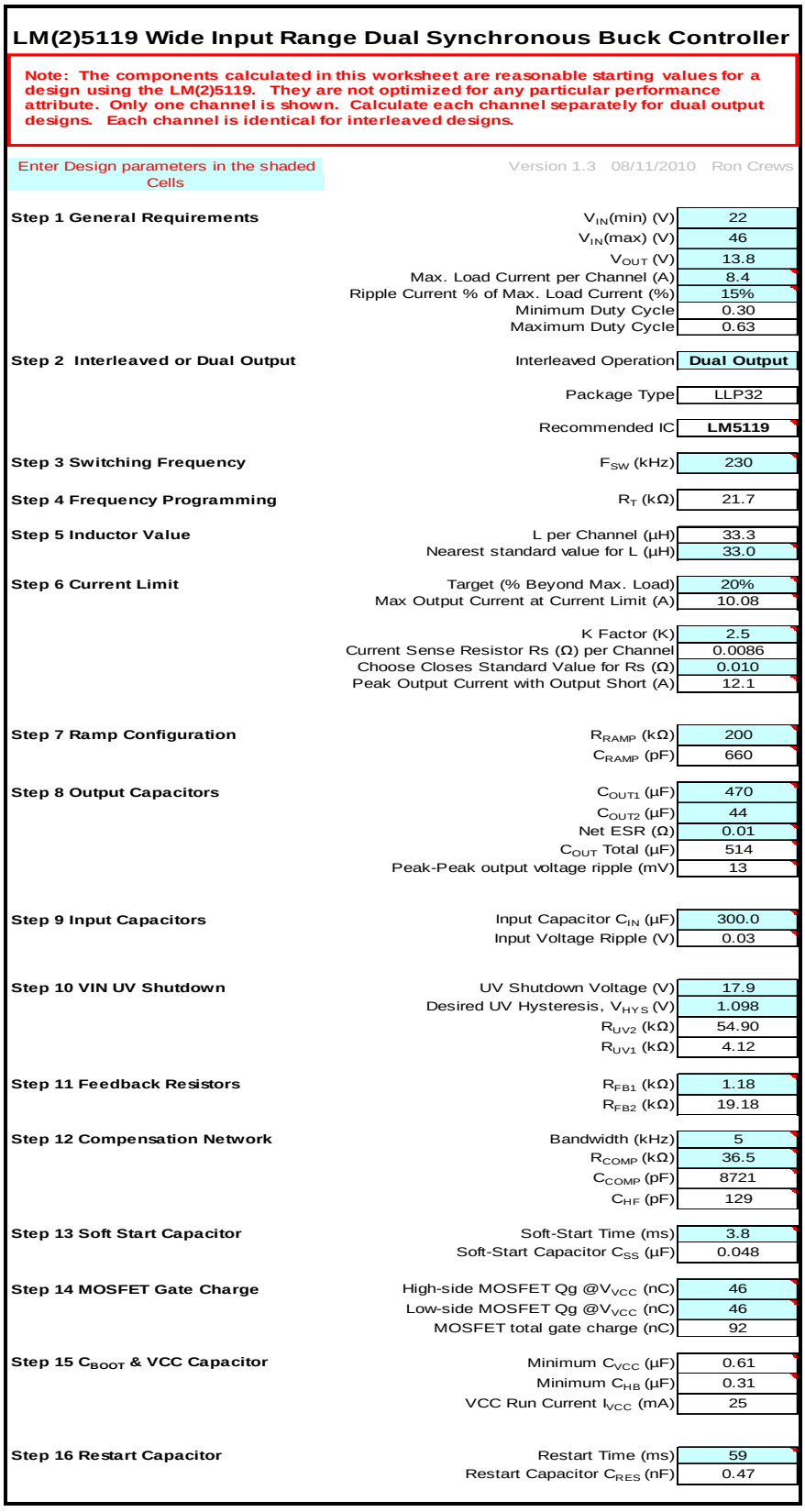
Thus, $f_{P(MOD)} = \frac{1}{2\pi \times 1.971\ \Omega \times 514 \times 10^{-6}\ \text{F}} = 157.064$ Hz

And the $DC\_GAIN_{(MOD)} = \frac{1.971\ \Omega}{\left(10 \times 10 \times 10^{-3}\ \Omega\right)} = 19.714 = 25.9$ dB

The Bode plots of the system were obtained from the LM5119 quick start worksheet calculator available on the Texas Instruments website. This calculator was used to ascertain whether the system is stable or not. A picture of the Excel worksheet is shown in Figure 38. The Bode plots are shown in Figures 39 (the modulator gain vs. frequency characteristic), Figure 40 (error amplifier gain and phase) and Figure 41 (overall voltage loop gain and phase).

The error amplifier of the LM5119 is configured as a Type II amplifier by means of $R_{COMP}$ and $C_{COMP}$. This configuration enables the error amplifier zero to cancel the dominant modulator pole leaving a single pole response at the crossover frequency of the voltage loop. This yields a stable voltage loop with 90° of phase margin.

For this design a 71.5 kΩ resistor was selected for $R_{COMP}$ and a 1.8 nF capacitance was selected for $C_{COMP}$. Figure 40 shows the error amplifier gain and phase plot.



**LM(2)5119 Wide Input Range Dual Synchronous Buck Controller**

Note: The components calculated in this worksheet are reasonable starting values for a design using the LM(2)5119. They are not optimized for any particular performance attribute. Only one channel is shown. Calculate each channel separately for dual output designs. Each channel is identical for interleaved designs.

Enter Design parameters in the shaded Cells

Version 1.3 08/11/2010 Ron Crews

| | | |
|---|---|---|
| **Step 1 General Requirements** | $V_{IN}$(min) (V) | 22 |
| | $V_{IN}$(max) (V) | 46 |
| | $V_{OUT}$ (V) | 13.8 |
| | Max. Load Current per Channel (A) | 8.4 |
| | Ripple Current % of Max. Load Current (%) | 15% |
| | Minimum Duty Cycle | 0.30 |
| | Maximum Duty Cycle | 0.63 |
| **Step 2 Interleaved or Dual Output** | Interleaved Operation | **Dual Output** |
| | Package Type | LLP32 |
| | Recommended IC | **LM5119** |
| **Step 3 Switching Frequency** | $F_{SW}$ (kHz) | 230 |
| **Step 4 Frequency Programming** | $R_T$ (kΩ) | 21.7 |
| **Step 5 Inductor Value** | L per Channel (µH) | 33.3 |
| | Nearest standard value for L (µH) | 33.0 |
| **Step 6 Current Limit** | Target (% Beyond Max. Load) | 20% |
| | Max Output Current at Current Limit (A) | 10.08 |
| | K Factor (K) | 2.5 |
| | Current Sense Resistor Rs (Ω) per Channel | 0.0086 |
| | Choose Closes Standard Value for Rs (Ω) | 0.010 |
| | Peak Output Current with Output Short (A) | 12.1 |
| **Step 7 Ramp Configuration** | $R_{RAMP}$ (kΩ) | 200 |
| | $C_{RAMP}$ (pF) | 660 |
| **Step 8 Output Capacitors** | $C_{OUT1}$ (µF) | 470 |
| | $C_{OUT2}$ (µF) | 44 |
| | Net ESR (Ω) | 0.01 |
| | $C_{OUT}$ Total (µF) | 514 |
| | Peak-Peak output voltage ripple (mV) | 13 |
| **Step 9 Input Capacitors** | Input Capacitor $C_{IN}$ (µF) | 300.0 |
| | Input Voltage Ripple (V) | 0.03 |
| **Step 10 VIN UV Shutdown** | UV Shutdown Voltage (V) | 17.9 |
| | Desired UV Hysteresis, $V_{HYS}$ (V) | 1.098 |
| | $R_{UV2}$ (kΩ) | 54.90 |
| | $R_{UV1}$ (kΩ) | 4.12 |
| **Step 11 Feedback Resistors** | $R_{FB1}$ (kΩ) | 1.18 |
| | $R_{FB2}$ (kΩ) | 19.18 |
| **Step 12 Compensation Network** | Bandwidth (kHz) | 5 |
| | $R_{COMP}$ (kΩ) | 36.5 |
| | $C_{COMP}$ (pF) | 8721 |
| | $C_{HF}$ (pF) | 129 |
| **Step 13 Soft Start Capacitor** | Soft-Start Time (ms) | 3.8 |
| | Soft-Start Capacitor $C_{SS}$ (µF) | 0.048 |
| **Step 14 MOSFET Gate Charge** | High-side MOSFET Qg @$V_{VCC}$ (nC) | 46 |
| | Low-side MOSFET Qg @$V_{VCC}$ (nC) | 46 |
| | MOSFET total gate charge (nC) | 92 |
| **Step 15 $C_{BOOT}$ & VCC Capacitor** | Minimum $C_{VCC}$ (µF) | 0.61 |
| | Minimum $C_{HB}$ (µF) | 0.31 |
| | VCC Run Current $I_{VCC}$ (mA) | 25 |
| **Step 16 Restart Capacitor** | Restart Time (ms) | 59 |
| | Restart Capacitor $C_{RES}$ (nF) | 0.47 |

**Figure 38: LM5119 Excel sheet used to obtain the Bode plots**

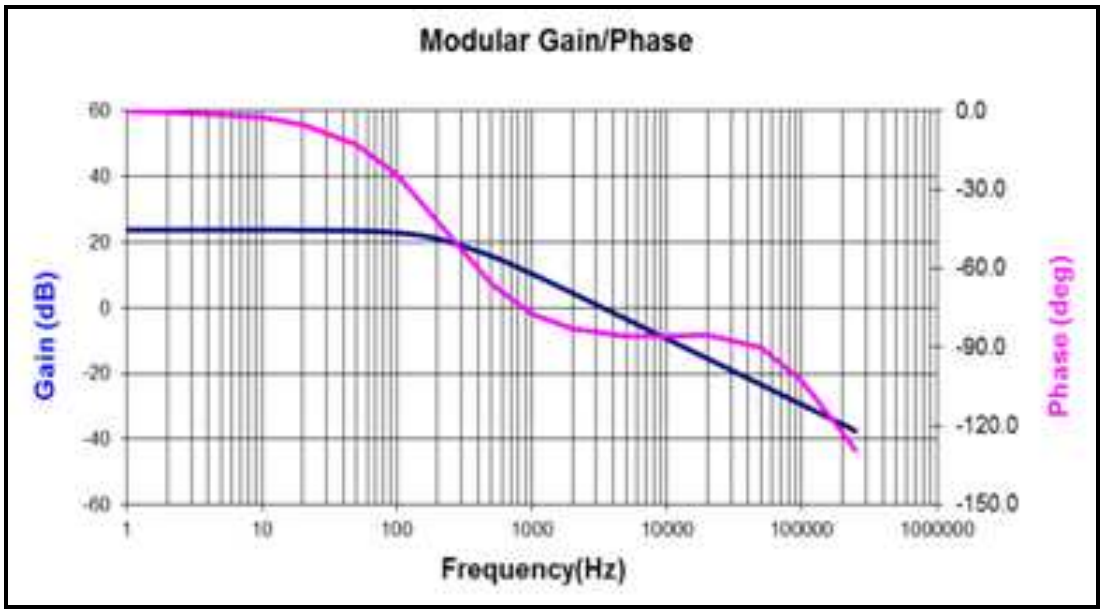



**Figure 39: Modulator gain and phase**

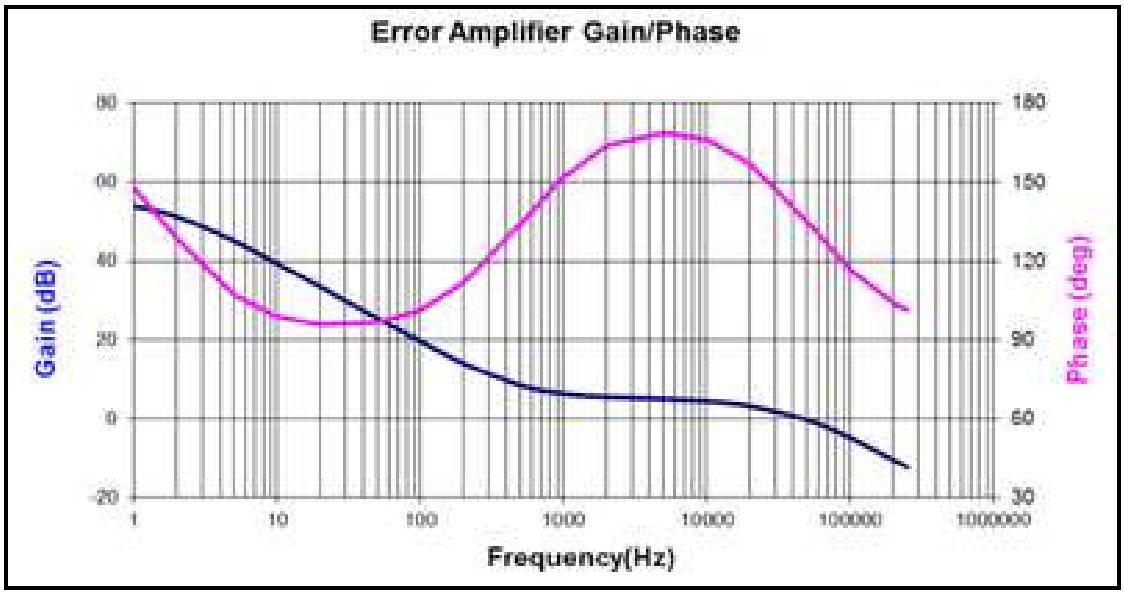



**Figure 40: Error amplifier gain and phase**

The overall voltage loop gain can then be predicted because it is the product of the modulator gain and the error amplifier gain. The overall loop gain plot is shown in Figure 41.

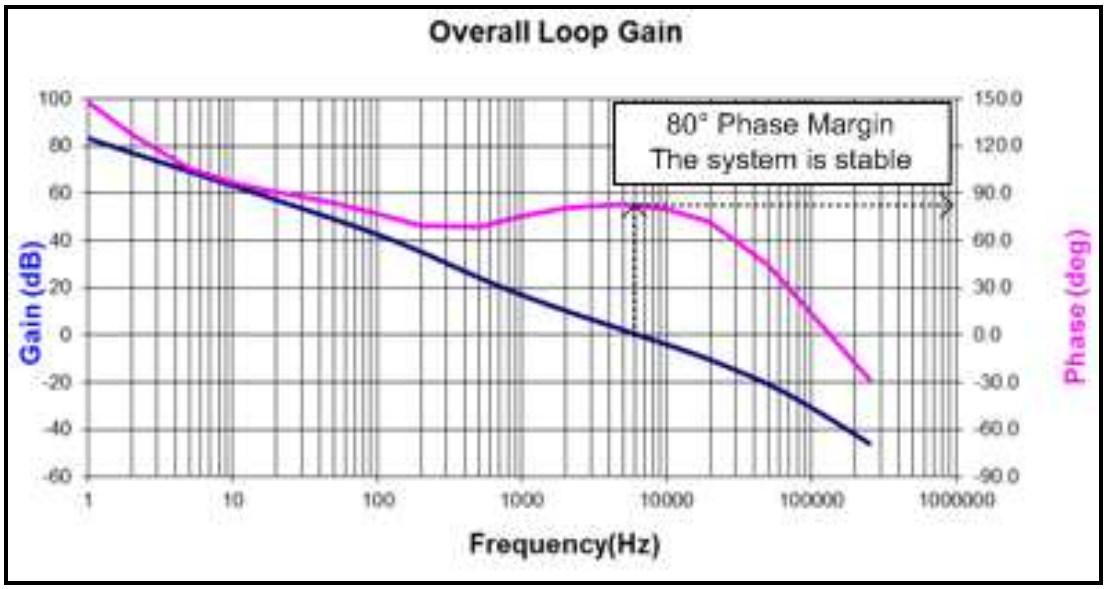



**Figure 41: Overall voltage loop gain and phase**

According to Dostal (2008:3) a minimum phase margin of 45° to 50° is necessary and more is better. In the case of this design, the maximum phase margin was found to be 80° which yields the conclusion that the designed system is stable.

The results of the step load transient tests will be presented in Chapter 4 in order to verify if the practical setup is really stable as found theoretically.

### 3.7.8 MOSFETs

As the input voltage for this design is limited to 46 V, the PSMN5R5 MOSFET is an appropriate choice for the reason that it has a maximum drain-source voltage of 60 V and a drain current of 100 A. This MOSFET has a low $R_{DS(ON)}$ (5.2 mΩ) and a total gate charge of 56 nC.

Switching devices used for multiphase buck converters have different criteria. For example the $R_{DS(ON)}$ of the synchronous rectifier should be as low as possible because it conducts current during most of the switching cycle. Another criterion is the switching speed so as to minimize the switching losses. The switching speed has a

direct relation with the gate charge because a low gate charge allows the gate driver to switch the MOSFET rapidly (Schuellein 2000).

## 3.8 Converter construction

To be able to meet the above requirements, the LM5119 evaluation board (see Annexure C) from Texas Instruments was used to implement the prototype. Figures 42 and 43 show the top and bottom views of the redesigned converter.

The construction of a multiphase synchronous buck converter requires a multilayer board on which careful layout considerations need to be taken into account. Some of these considerations are (Schuellein 2000):

- Output inductors and capacitors should be situated on wide planes connected to the load so as to minimize drops during heavy loads and transients.
- The area of the inductor switching node should be minimised by placing the inductor and the MOSFETs of each phase close to each other.
- High current traces such as those of the inductor switching node and gate drive should be as short and wide as possible to negate the effect of EMI.
- Input capacitors should be placed as close to the switching MOSFETs as possible and with the output capacitors closer to the load.

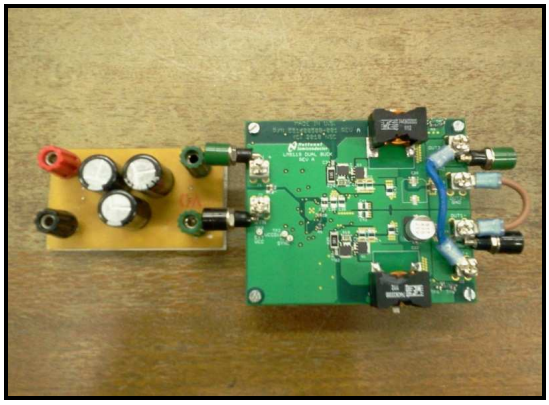


**Figure 42: Top view of the redesigned LM5119 evaluation board and input capacitors on the left-hand side**

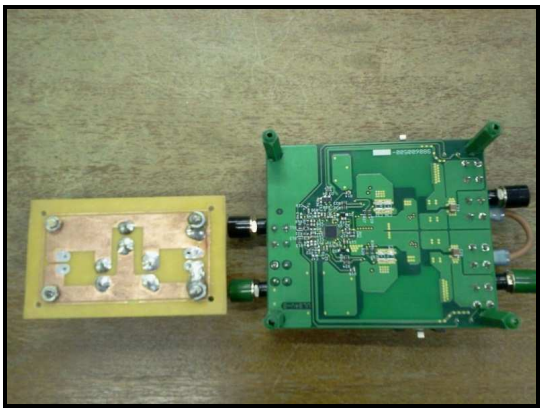


**Figure 43: Bottom view of the redesigned LM5119 evaluation board and input capacitors on the left-hand side**

The LM5119 evaluation board was redesigned according to the converter specifications because the board comes already populated with components. Hence, the components replaced include the input and output capacitors, inductors as well as some resistors and capacitors associated with the operation of the LM5119 controller.

## 3.9 Summary

A brief presentation of the topology used was presented. The design procedure and calculations regarding components as well as the construction of the converter were considered.

The next chapter will discuss the measurements and results.

# Chapter 4 Results

## 4.1 Introduction

Chapter 4 considers the simulation performed to obtain theoretical waveforms. The tests and measurements performed on the converter are also presented. A comparative analysis of some simulated and experimental results of the converter power stage is also presented. The converter has been mainly tested according to the problem statement set out in Chapter 1.

## 4.2 Simulation

The simulated results were obtained by means of Cadence OrCAD. This software package is widely used to simulate SMPS. It includes a schematic capture program called Capture and a SPICE simulator called PSpice. Owing to Cadence OrCAD's widespread use in industry most semiconductor manufacturers produce device models for both the PSpice and Capture.

After completion of the design phase, a simulation of a portion of the converter was implemented. The simulation model consists of a single phase synchronous buck converter. As the LM5119 PSpice model is not available, the LM5117 model was downloaded from the Texas Instruments website. The LM5117 is the one channel version of the LM5119. The reason behind this is that the designed converter consists of two identical synchronous buck converters. Hence, to simplify the analysis, a single channel synchronous buck was used. The desired frequency and the pulse width signals for the gates of the MOSFETs were obtained using the LM5117 controller. It is important to note that components used in the schematic were modeled to be similar to the components of the prototype.

Figure 44 shows the simulation circuit diagram. The input of the power supply is modeled by a constant voltage source *V1*. The circuit is simulated for a run time of at least 3.5 ms to ensure that the simulation reaches steady state. Each input and

output capacitor's ESR (Equivalent Series Resistance) along with inductor's DCR (Direct Current Resistance) are also modeled in this simulation in order to get a good representation of what is happening in each phase of the actual hardware circuit. The circuit's performance was then studied by obtaining plots of critical parameters such as the output voltage, the inductor current, etc. Figure 45 shows the output filter and load current waveforms during typical operation with a load of 2 Ω. This plot shows that the inductor ripple current is filtered out by the output capacitance. Hence the load sees the DC current.

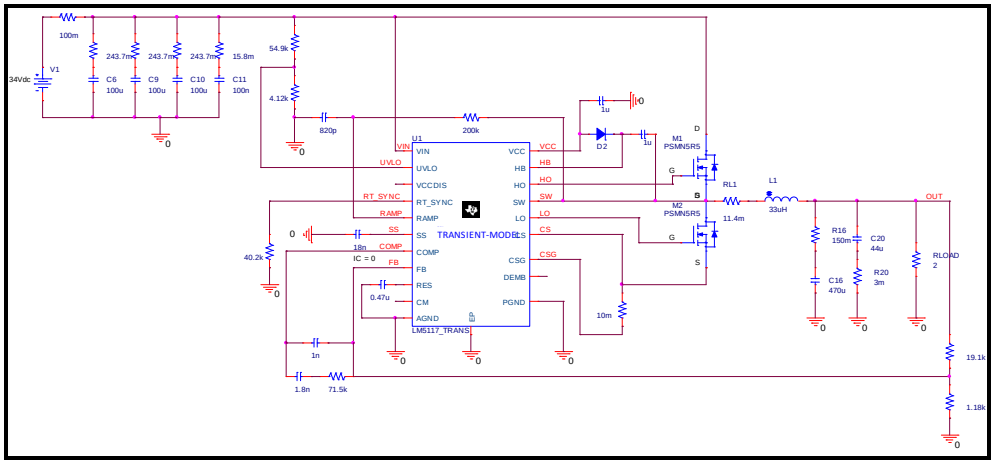



**Figure 44: Single channel synchronous buck circuit used to obtain simulation results**

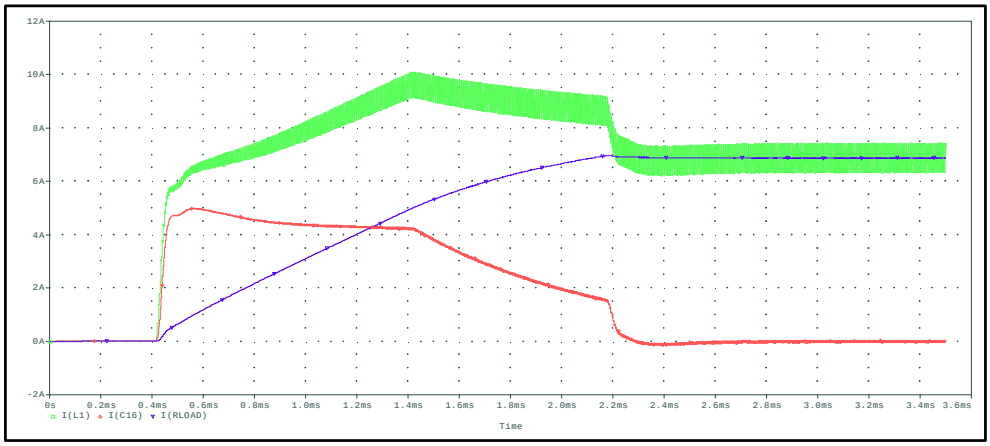



**Figure 45: Output inductor (green trace), output capacitor (red trace) and load (blue trace) current waveforms**

Figure 46 shows the simulation result for the output voltage.

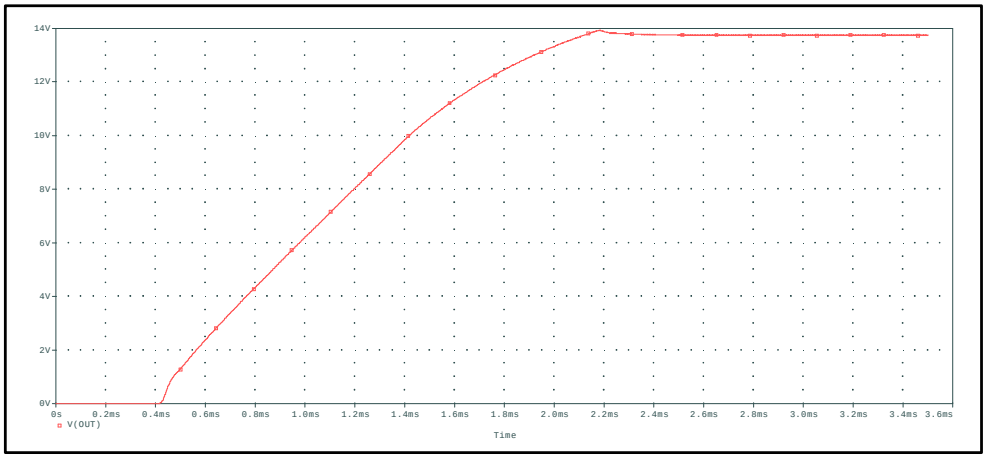



**Figure 46: Result of the simulated output voltage.**

## 4.3 Turn-on input voltage test

This test was performed to ascertain at what value of the input voltage the converter starts delivering the required output voltage. The waveforms were obtained using a Rigol DS2102 100 MHz digital oscilloscope. Figure 47 shows the recorded the input voltage while monitoring the output voltage coming into the specified regulation range.

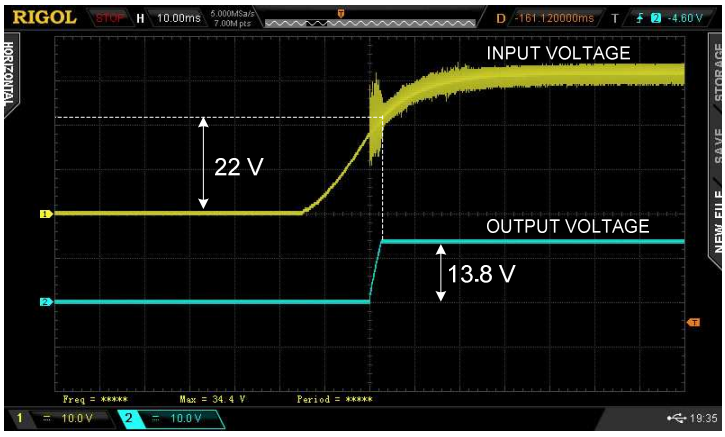



**Figure 47: Turn-on input voltage test result**

The measured input voltage was found to be 22 V, which is the lowest voltage within the specified range of input voltages.

## 4.4 Soft-start time test

The soft-start time is a small time duration needed for the output voltage to reach the specified accuracy when the output is loaded into a resistive load. A sequence of events occurs when power is applied to the converter. Soft-start capacitors and other components allow for a linear increase in output voltages (See Annexure C).

Figure 48 shows the soft-start waveform obtained while measuring the output voltage on the hardware (Input voltage: 34 V, 12 Ω load on 13.8 V output). The soft-start time of the converter is 1.28 ms.

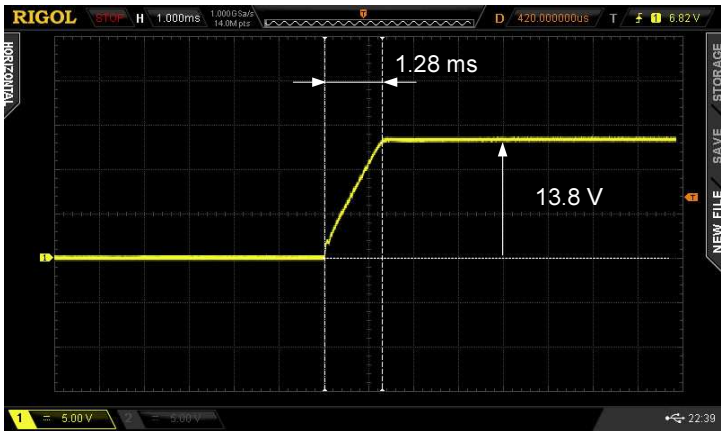



**Figure 48: Output voltage waveform and start-up time**

## 4.5 Load transient test

The load transient test is the simplest way to analyse the loop stability of a converter (Simpson 2007:2). This test gives a qualitative indication of the feedback loop circuitry performance. In case the results indicate potential instabilities, then stability margin measurements tests are usually appropriate if feasible (Leon 2010:7).

Figure 49 illustrates the block diagram of the test set-up diagram needed to evaluate the regulator's response to a transient load. The test was done at different resistance loads. The test set-up included a PIC microcontroller needed to generate a step voltage to switch ON a MOSFET. When the switching element is ON, the value of the load changes. The oscilloscope connected to the output shows a small voltage droop, which recovers to the steady state value after a short time. Figure 50 shows the practical setup used for the measurement.

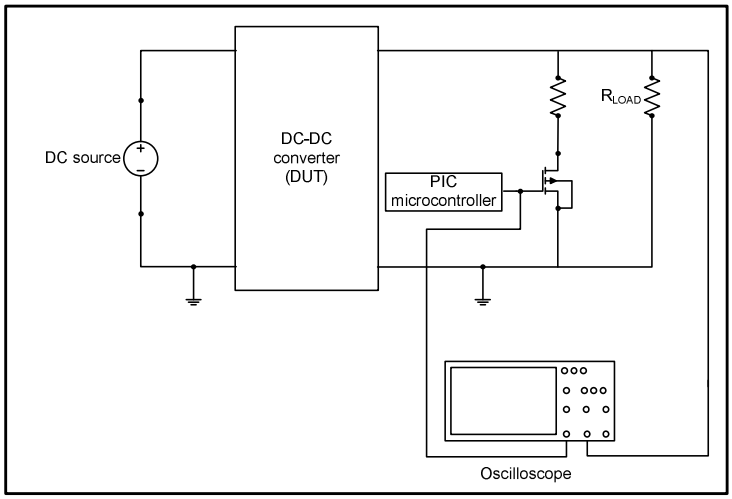



**Figure 49: Load transient test setup**

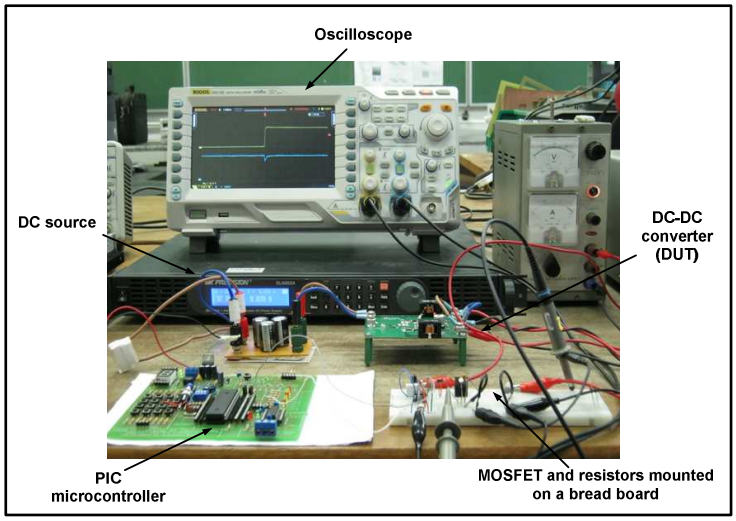



**Figure 50: Practical of the transient load test**

Figure 51 shows the step load response of the converter. The upper waveform shows the 12 V step voltage applied to the gate of the MOSFET. The lower waveform shows a voltage droop in the output voltage during the sudden change in the value of the load. The converter output current went from 0.8 A to 2 A in about 380 ns. This is called load transient recovery time or transient response time (Brown 2001:76). It represents how long it takes for the converter to return to its set voltage after an abrupt change in load current.

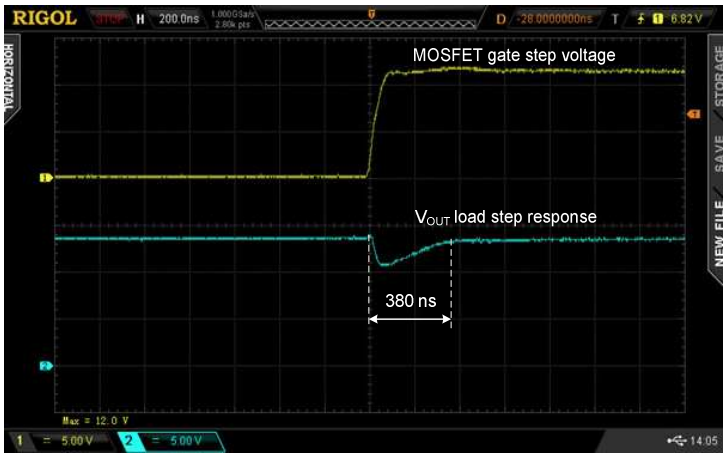



**Figure 51: Hardware step load response**

According to Simpson (2007:4) the appearance of the $V_{OUT}$ load step response should extinguish very cleanly and have the fastest possible settling time. Based on this criterion, the converter shows a very good stability which is in accord with the theoretical calculations presented in Chapter 3.

In a converter, the type 2 error amplifier compares the converter output voltage with a reference voltage to produce an error signal that is used to adjust the duty ratio of the switches. Compensation associated with the amplifier determines the control loop performance and provides for a stable control system (Hart 2011:308).

The converter prototype includes a type 2 amplifier which acts in keeping the output voltage constant under varying input current and load conditions. The measurement

shown in Figure 51 indicates how the controller brings the load voltage back to its set point in 380 ns. The two dashed lines highlight the area of interest.

## 4.6 Further measurement results

In Figure 52 the complete circuit diagram with the test points (TPs) is shown. The prototype consists of a power stage with two synchronous buck converters connected in an interleaved configuration. The controller stage is constituted by the LM5119 PWM controller.

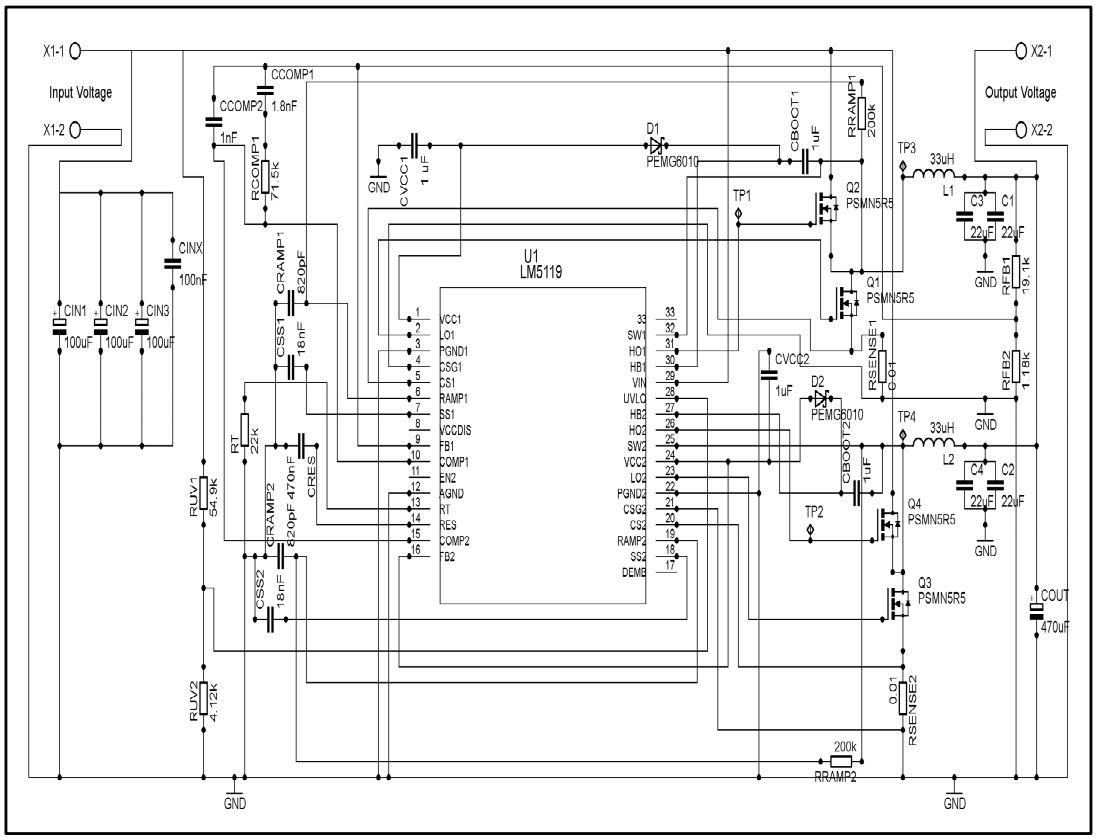



**Figure 52: Complete circuit diagram of the converter**

Figure 53 is obtained simultaneously from test points TP1 and TP2 of the experimental model. The trace on top is the high-side MOSFET gate pulses for *Q2*. It shows as well its period being 4.560 µs yielding a switching frequency of 219 kHz.

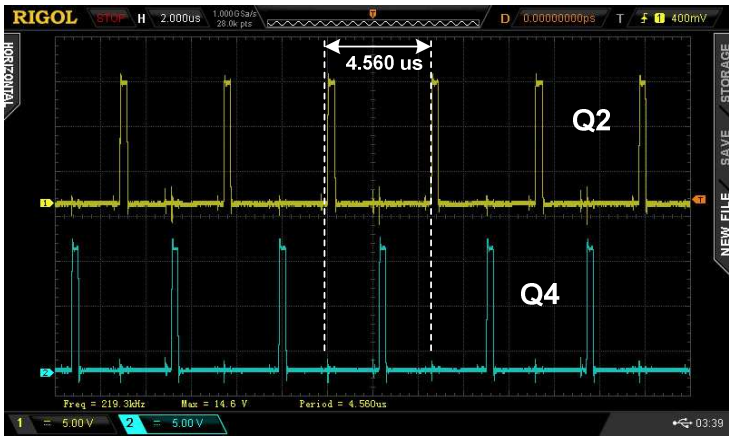



**Figure 53: *Q2* and *Q4* high-side MOSFET gate voltages waveforms obtained at TP1 and TP2**

This frequency approaches the 230 kHz set out in the requirements. The frequency is not accurate due to the tolerance in the value of the timing resistor $R_T$. The bottom trace is high-side MOSFET gate pulse for *Q4*. It can also be seen that there exists a 180° phase shift between *Q2* and *Q4* switching pulses.

Figure 54 shows the switch node voltages for each phase obtained simultaneously at TP3 and TP4. Figure 55 shows the simulated model's result for the switch node voltage.

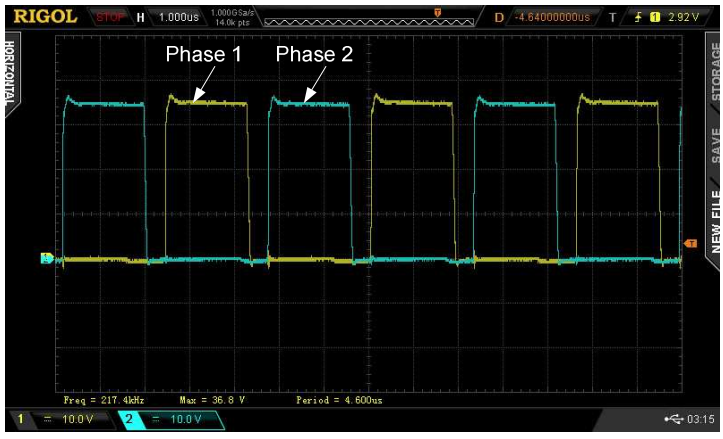



**Figure 54: Switch node 1 and 2 waveforms obtained at TP3 and TP4**

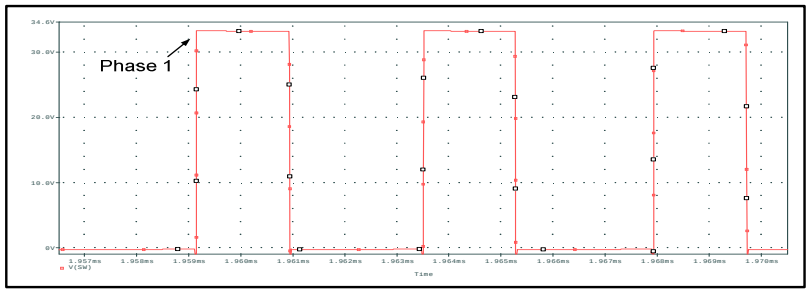



**Figure 55: Simulated voltage of the switch node voltage**

From the waveforms, shown in Figure 54, it is clear that the phases are interleaved because the waveform at the switch node 1 is the same as the one at switch node 2. According to Baba (2012) interleaving minimises ripple currents at the input and output.

## 4.7 Efficiency and wide input voltage experiments

A DC–DC converter test apparatus shown in Figure 56 was used in order to obtain the efficiency and wide input voltage measurements. The converter input power was supplied by a BK precision XLN6024 high power programmable DC power supply. Values of voltages and currents were obtained from digital multimeters. Finally, a TT*i* LD 300 DC electronic load was used as a load for the converter.

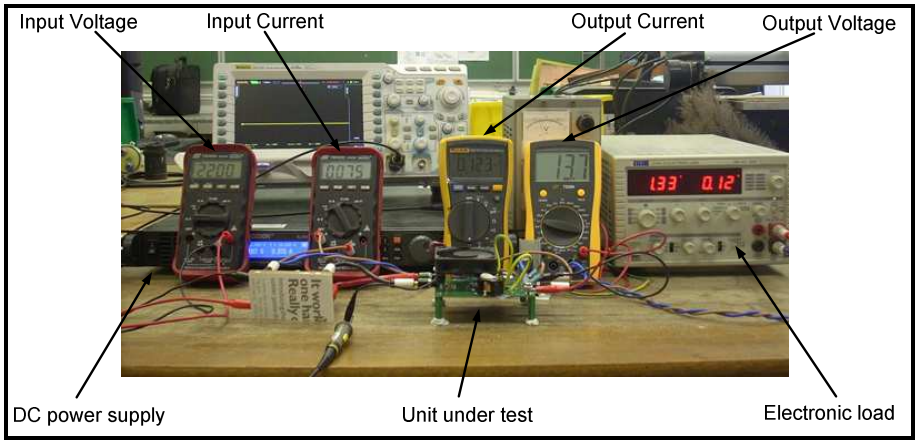



**Figure 56: Hardware setup for efficiency and wide input voltage measurements**

The testing of the redesigned LM5119 evaluation board yielded results shown in Table 3 and Figure 57. Table 3 and Figure 57 show the efficiency of the converter as the load was increased. The converter functioned efficiently with loading up to 7 A with an output voltage which varied slightly from 13.8 to 13.4 V.

**Table 3: Test of re-designed LM5119 evaluation board at a input voltage of 22 V**

| Input Voltage ($V_{in}$) | Input Current ($I_{in}$) | Input Power ($P_{in}$) | Output Voltage ($V_{out}$) | Output Current ($I_{out}$) | Output Power ($P_{out}$) | Efficiency (%) |
|---|---|---|---|---|---|---|
| 22 | 0.935 | 20.57 | 13.7 | 1.4 | 19.18 | 93 |
| 22 | 1.852 | 40.744 | 13.59 | 2.8 | 38.052 | 93 |
| 22 | 2.744 | 60.368 | 13.51 | 4.2 | 56.742 | 94 |
| 22 | 3.669 | 80.718 | 13.47 | 5.6 | 75.432 | 93 |
| 22 | 4.595 | 101.09 | 13.4 | 7 | 93.8 | 93 |

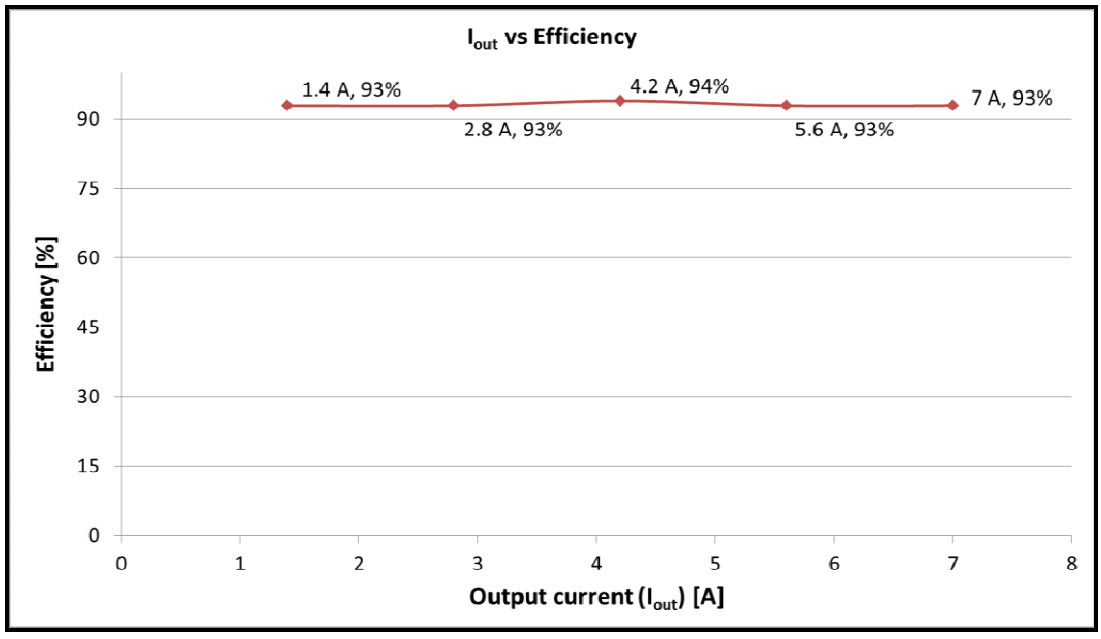



**Figure 57: Efficiency plot of the redesigned LM5119 evaluation board for an input voltage of 22 V**

The testing of the redesigned evaluation board at a maximum input voltage of 46 V yielded the results shown in Table 4 and Figure 58.

**Table 4: Test of re-designed LM5119 evaluation board at a input voltage of 46 V**

| Input Voltage ($V_{in}$) | Input Current ($I_{in}$) | Input Power ($P_{in}$) | Output Voltage ($V_{out}$) | Output Current ($I_{out}$) | Output Power ($P_{out}$) | Efficiency (%) |
|---|---|---|---|---|---|---|
| 46 | 0.46 | 21.16 | 13.7 | 1.4 | 19.18 | 91 |
| 46 | 0.89 | 40.94 | 13.65 | 2.8 | 38.22 | 93 |
| 46 | 1.35 | 62.1 | 13.6 | 4.2 | 57.12 | 92 |
| 46 | 1.78 | 81.702 | 13.5 | 5.6 | 75.6 | 93 |
| 46 | 2.2 | 100.98 | 13.48 | 7 | 94.36 | 93 |

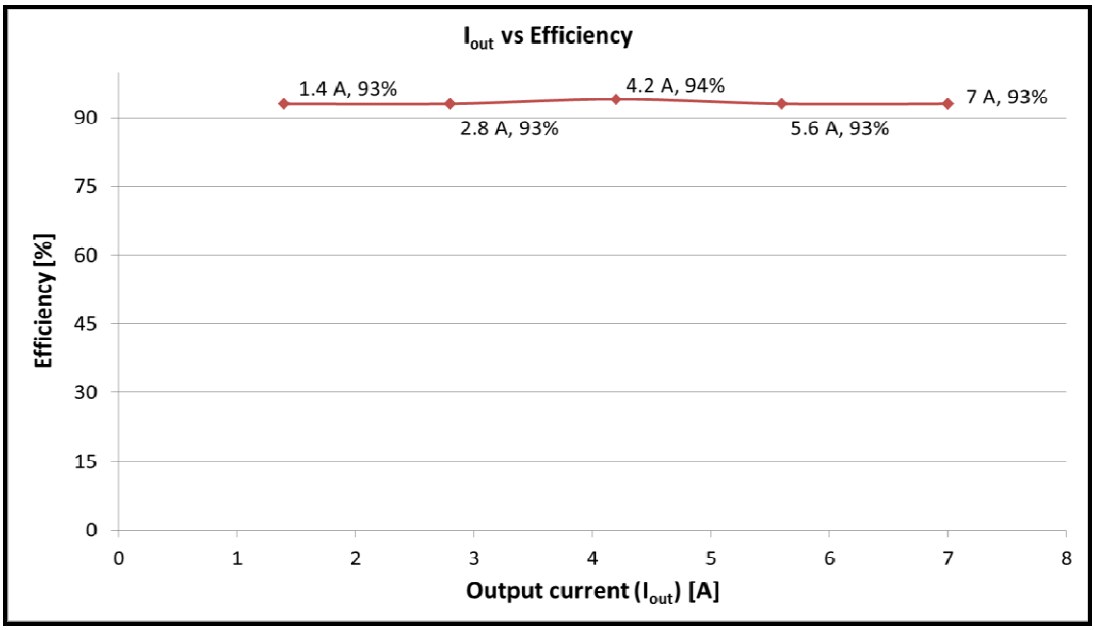



**Figure 58: Efficiency plot of the redesigned LM5119 evaluation board for an input voltage of 46 V**

These results showed that the converter is capable of handling a wide range of input voltages as set out in the specifications. The converter efficiency was above 90

percent. This indicates that the requirements set out in the problem statement were met successfully.

More importantly, it was found that the converter operated safely up to 7 A, instead of the 14 A, that was initially necessary to attain the required 200 W mark. In order to attain this wattage, the proposed solution is to connect two redesigned LM5119 evaluation boards in parallel. This will be discussed further in Chapter 5.

## 4.5 Calculations

The efficiency is defined as the ratio of total output power to total input power. It expressed as a percentage. It is normally specified at full load and nominal input voltage (Lenk 2005:179).

$$\eta = \frac{P_{out}}{P_{in}} \tag{22}$$

Calculating the efficiency of the system at full load and a nominal voltage of 34 V:

$$\eta = \frac{94.5\ \text{W}}{101.32\ \text{W}} = 93\%$$

The load regulation is defined as the change in output voltage over the specified change in output load. It usually specified in percentage (Maniktala 2006:5). Figure 59 shows the result of the experimental converter load regulation.

The load regulation is expressed as:

$$\%\ \text{Load Regulation} = \frac{V_{\text{loadmin}} - V_{\text{loadmax}}}{V_{\text{loadnom}}} \times 100 \tag{23}$$

where $V_{loadmin} \equiv$ output voltage at minimum load

$V_{loadmax}$ ≡ output voltage at maximum load

$V_{loadnom}$ ≡ specified output voltage

Calculating the overall percentage of load regulation of the converter:

$$\% \text{ Load Regulation} = \frac{13.7 - 13.4}{13.8} \times 100 = 2\ \%$$

The load regulation results as obtained, are presented. At this stage, no attempts were made to keep the voltage steady.

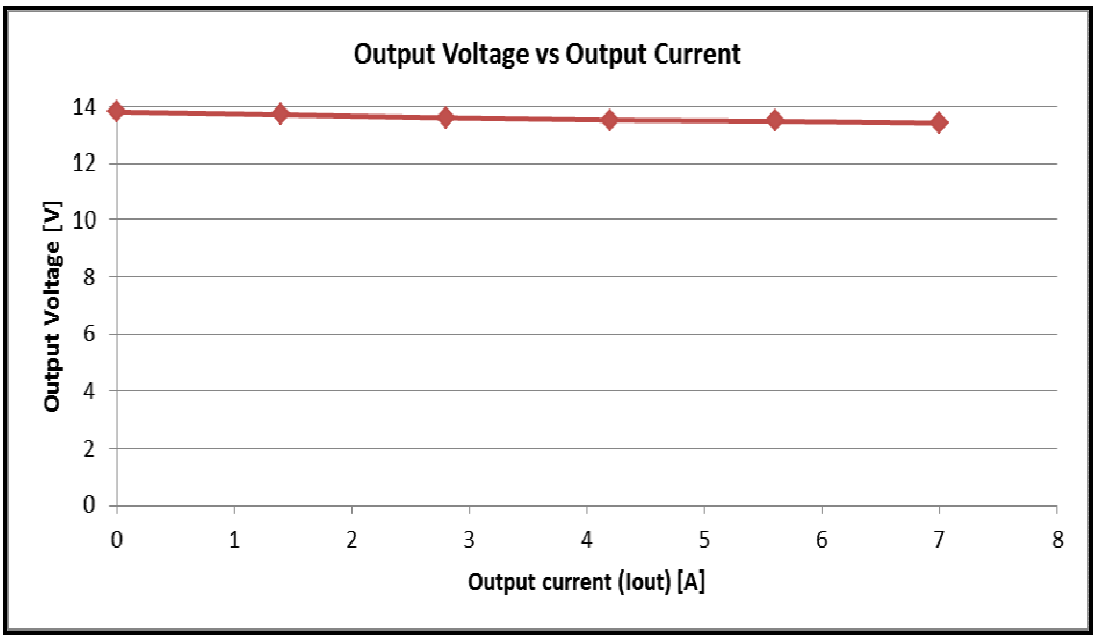



**Figure 59: Load regulation of the converter**

## 4.6 200 W PAFC Modelling

According to Pholo (2008:58) the output power of a single cell for a PAFC was found to be 3.3 W. The obtained converter measurement results have shown that its input voltage ranges between 22 and 46 V. In order to obtain a mathematical model for a 200 W stack, a value of $N_c$ (number of identical cells) is required. Therefore:

$$N_C = \frac{200\ \text{W}}{3.3\ \text{W}} = 60.6\ \text{Cells} \quad (24)$$

The rounded value of cells is thus 60 cells.

Furthermore, Table 5 gives the output voltage of the single cell PAFC at different currents (Pholo 2008:57). The performance of a FC is determined by the use of a polarisation curve. The polarisation curve in Figure 60 presents the performance of the PAFC designed in research at the Vaal University of Technology.

**Table 5: Measured data of a PAFC stack (Pholo 2008:57)**

| Stack voltage (V) | Current (A) | Current density (mA.cm$^{-2}$) |
|---|---|---|
| 0.73 | 0.03 | 1.2 |
| 0.64 | 0.04 | 1.6 |
| 0.63 | 0.05 | 2.0 |
| 0.62 | 0.06 | 2.4 |
| 0.60 | 0.08 | 3.2 |
| 0.59 | 0.1 | 4 |
| 0.57 | 0.2 | 8 |
| 0.56 | 0.3 | 12 |
| 0.55 | 0.4 | 16 |
| 0.54 | 0.5 | 20 |
| 0.53 | 0.6 | 24 |
| 0.52 | 0.7 | 28 |
| 0.51 | 0.8 | 32 |
| 0.50 | 1.0 | 40 |
| 0.49 | 1.5 | 60 |
| 0.48 | 2.0 | 80 |
| 0.47 | 2.5 | 100 |
| 0.46 | 3.0 | 120 |

**Table 5: Measured data of a PAFC stack (Pholo 2008:57) continued**

| Stack voltage (V) | Current (A) | Current density (mA.cm$^{-2}$) |
|---|---|---|
| 0.45 | 3.5 | 140 |
| 0.44 | 4.0 | 160 |
| 0.43 | 4.5 | 180 |
| 0.42 | 5.5 | 220 |

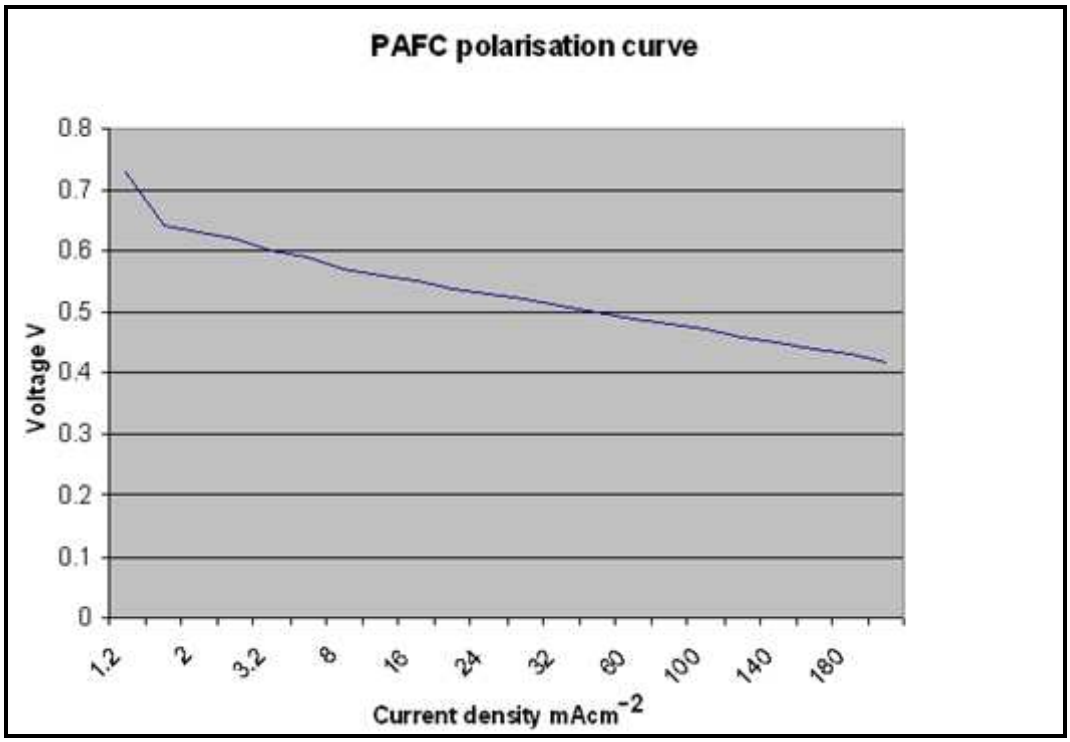



**Figure 60: Performance curve for a single cell PAFC. (Pholo 2008:76)**

The data in Table 5 can be used to predict the 60 cells stack PAFC model. By means of simulation, it can be verified that the stack will be compatible with the converter's wide input range of voltages. But this analysis goes beyond the scope of this study.

## 4.7 Summary

The experimental measurements and results of the converter module have been covered in this chapter. Some waveforms of the power and control sections have

also been presented. The results related to the original problem statement have been discussed. These facts indicate the successful power conversion of a wide range of input voltages to a stable voltage around 13.8 V with a current of 7 A.

Chapter 5 is the final chapter of this dissertation. It will consider the conclusions reached and recommendations for future research that evolved from the study of the design and development of a 200 W converter for PAFC.

# Chapter 5 Conclusions and recommendations

## 5.1 Introduction

The last chapter of this document presents the conclusions that have been reached based on the results obtained regarding the design and development of a 200 W converter for phosphoric acid FCs. As the study requirements for the converter pointed out in the original problem statement were achieved, the recommendations for future research will be considered.

## 5.2 Conclusions

At the outset of this study, the analysis of the literature available showed that the obstacles for integrating FCs with modern electronics are the low output voltage of the FC combined with its instability over the range of electrical loading. Thus, power conditioning circuitry to accommodate for the inconsistencies and load-driven output voltage variation is a critical component of any FC system. A DC–DC converter with a wide range of input voltages was therefore required to regulate the FC voltage.

Accordingly, it was found that one of the most outstanding conclusions that can be made regarding this project was that the decision regarding the choice of DC–DC converter topology is of paramount importance. The research showed that a change in topology means that the components used will change as well. Hence it was necessary to spend sufficient time to determine which topology will be suited for the application. Originally, three converter topologies have been investigated with regard to their wattage specifications. These included: a two-switch forward converter, a half-bridge converter and a push-pull converter. The latter was selected mainly because it is used in application where the wattage range varies from 200 W to 1 kW.

The push-pull topology uses magnetic components such as a centre tap transformer and inductors which have a tremendous impact on the overall efficiency of the converter. Several attempts were made to construct the transformer using a N87 Mn-Zn ferrite core material mounted on a EPCOS ETD 49 core shape. The transformer also comprised a primary as well as a secondary centre tap winding made with copper foils in order to achieve good layer coupling, minimise leakage inductance and skin effect. Inductors were constructed using toroid cores and copper wires. Besides the magnetic components, the semiconductor switches had to be chosen according to their voltage and current handling characteristics taking into account that the push-pull converter switches must handle twice the input voltage. Another time consuming task was to design the control section of the converter. The control scheme was built around a PWM IC UC3825 from Texas Instruments which drove the gates of the two MOSFET switches. The UC3825 chip's main role was to maintain the regulated output voltage. While the prototype did not meet expectations, it operated open-loop at a switching frequency of 50 kHz, whilst it delivered 13.8 V with a 40 W of output power and an efficiency of 63 percent.

Later, recent comprehensive studies highlighted the fact that the power electronic system interfacing directly to the FC stacks has a significant impact on the long-term durability and reliable energy efficiency of the FC. Energy conversion efficiency for the FC then came to the fore as of significant importance. Today, the efficiencies of power-electronics conversion technology have exceeded 90 percent. However, under severe cost constraints, most of these technologies are not economically viable. As such, achieving high power-conversion efficiency at a significantly low cost for the viability of FC power systems was a daunting challenge.

Taking these concerns into account, a new design consisting of an interleaved synchronous buck converter was implemented. The design was based on the National Semiconductor LM5119 IC using an LM5119 evaluation board. The evaluation board was redesigned to meet the requirements for the application. In total, three LM5119 evaluation boards were used. The first one worked well. However a short circuit led to it being damaged. A second board was purchased and

accordingly redesigned using a lower value for the current sense resistor $R_S$ (5 mΩ) in order to increase the power output. Unfortunately there was no change, the maximum current stayed at 7 A. A third evaluation board was offered free of charge, courtesy of Texas Instruments and the board was redesigned accordingly. The module worked well as the parameters used in the first place with the first LM5119 evaluation board were kept as they were.

The focus was directed on building a converter capable of handling a wide range of input voltages. This was made possible using the LM5119 controller. This IC is well suited for operation of the DC–DC regulator with a wide range of voltages (5.5 to 65 V). The efficiency was found to be greater than 90 percent. This result is well above the minimum efficiency that a FC's converter should have which is 85 percent according to the literature. Hence the objective pursued with regard to the design and development of a highly efficient and wide range input voltages converter was achieved.

## 5.3 Recommendations

As stated in Chapter 4, the converter module was designed to produce 14 A of output current. However, the experimental converter achieved 7 A. In order to reach 14 A, which will result in the targeted 200 W output power, two of the redesigned converters need to be connected in parallel in order to obtain 14 A.

However, studies have shown that connecting DC–DC converters in parallel has advantages and disadvantages. Besides, modules of the same kind can be connected directly in parallel. This method retains efficiency. But differences in current between modules can cause unequal heating and possible change in output voltage. This situation requires that the output voltages be kept equal.

When connecting converter outputs it should be remembered that the switching will not be synchronous, hence some form of coupling should be employed. One possible solution is to use a diode feed; this is suitable mainly for 12 to15 V output types only

where the diode voltage drop (typically 0.6 V) will not affect the circuit functionality. This method also has a beat frequency that will superimpose itself over the ripple of the two converters; this can be reduced by using an external capacitor at the paralleled output. The preferred method of connecting converters in parallel is via series inductors on the output. This configuration not only has a lower loss of voltage than the diode method, but by suitable choice of inductor and an additional external capacitor, the beat frequency can be significantly reduced, as will the ripple from each converter. This aspect remains to be investigated with regard to the connection of two DC–DC synchronous buck converters in parallel.

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## List of Annexures

Bill of materials ANNEXURE A

| Part | Value | Package |
|---|---|---|
| Cboot1 | 1 uF, 16 V | 0805 |
| Cboot2 | 1 uF, 16 V | 0805 |
| Ccomp1 | 1.8 nF, 25 V | 0805 |
| Ccomp2 | 1.8 nF, 25 V | 0805 |
| Cin | 3 x 100 uF, 200 V | CAPPR7.5-16X25 324 $mm^2$ |
| Cinx | 100 nF, 100 V | 0805 |
| Cout1 | 470 uF, 25 V | CAPSMT_62_JA0 151 $mm^2$ |
| Cramp1 | 820 pF, 50 V | 0805 |
| Cramp2 | 820 pF, 50 V | 0805 |
| Cres | 470 nF, 16 V | 0402 |
| Css1 | 18.0 nF, 50 V | 0805 |
| Css2 | 18.0 nF, 50 V | 0805 |
| Cvcc1 | 1 uF, 16 V | 0805 |
| Cvcc2 | 1 uF, 16 V | 0805 |
| D1 | 60 V, 1 A | SOD123F |
| D2 | 60 V, 1 A | SOD123F |
| L1 | 33 µH | IND_WE-HCF 540mm2 |
| L2 | 33 µH | IND_WE-HCF 540mm2 |
| Rcomp1 | 71.5 kΩ | 0805 |
| Rfb1 | 1.18 kΩ | 0805 |
| Rfb2 | 19.1 kΩ | 0805 |
| Rramp1 | 200 kΩ | 0805 |
| Rramp2 | 200 kΩ | 0805 |
| Rsense1 | 10 mΩ | 1206 |
| Rsense2 | 10 mΩ | 1206 |
| Rt | 40.2 kΩ | 0805 |
| Ruv1 | 54.9 kΩ | 0805 |
| Ruv2 | 4.12 kΩ | 0805 |
| U1 | LM5119PSQ | SQA32A 49$mm^2$ |
| LM5119 EVALUATION BOARD***** | | |

***** Arrow Altech Distribution (Pty) Ltd

LM5119EVAL/NOPB

Pricing for units

Break 1-9 units at R2065.80 ea

Break 10-99 units at R1968.12 ea

Lead time +- 2 weeks.

# LM5119

***LM5119 Wide Input Range Dual Synchronous Buck Controller***


Literature Number: SNVS676E

National Semiconductor

September 28, 2010

# LM5119

## Wide Input Range Dual Synchronous Buck Controller

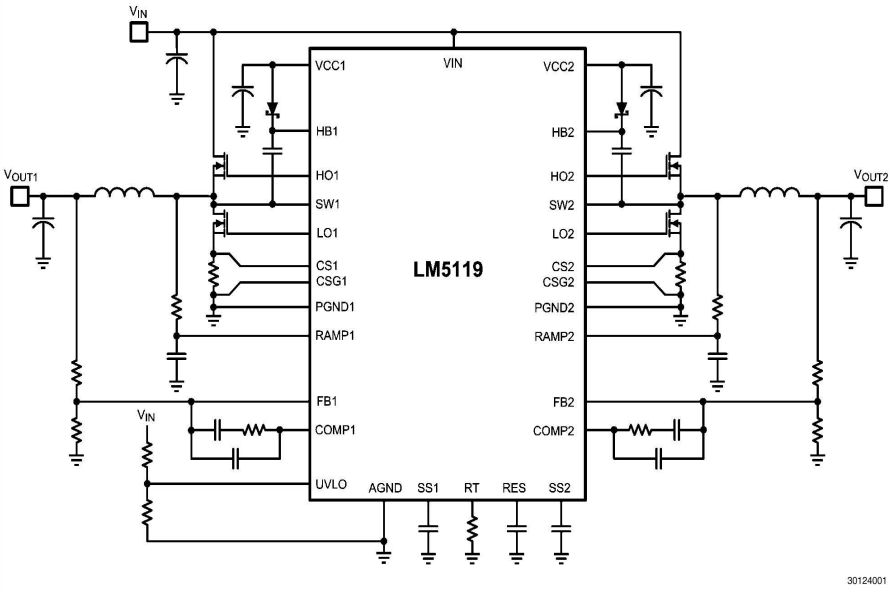
### General Description

The LM5119 is a dual synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications. The switching frequency is programmable from 50kHz to 750kHz. The LM5119 drives external high-side and low-side NMOS power switches with adaptive dead-time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions. A high voltage bias regulator with automatic switch-over to external bias further improves efficiency. Additional features include thermal shutdown, frequency synchronization, cycle-by-cycle and hiccup mode current limit and adjustable line under-voltage lockout. The device is available in a power enhanced leadless LLP-32 package featuring an exposed die attach pad to aid thermal dissipation.

### Features

- Emulated peak current mode control
- Wide operating range from 5.5V to 65V
- Easily configurable for dual outputs or interleaved single output
- Robust 3.3A peak gate drive
- Switching frequency programmable to 750kHz
- Optional diode emulation mode
- Programmable output from 0.8V
- Precision 1.5% voltage reference
- Programmable current limit
- Hiccup mode overload protection
- Programmable soft-start
- Programmable line under-voltage lockout
- Automatic switch-over to external bias supply
- Channel2 enable logic input
- Thermal Shutdown
- Leadless LLP32 (5mm x 5mm) package

### Typical Application

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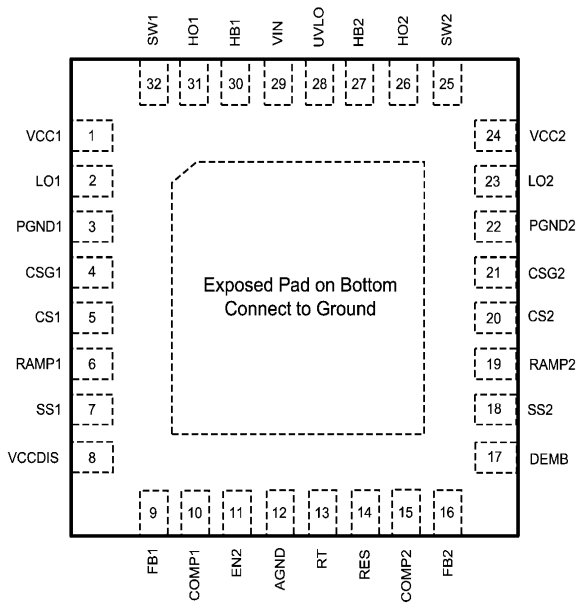
## Connection Diagram




**Top View**
**32–Lead LLP**

| Order Number | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|
| LM5119PSQ | LLP-32 | SQA32A | 1000 Units on Tape and Reel |
| LM5119PSQX | LLP-32 | SQA32A | 4500 Units on Tape and Reel |
| LM5119PSQE | LLP-32 | SQA32A | 250 Units on Tape and Reel |

## Pin Descriptions

| Pin | Name | Description |
|---|---|---|
| 1 | VCC1 | Bias supply pin. Locally decouple to PGND1 using a low ESR/ESL capacitor located as close to controller as possible. |
| 2 | LO1 | Low side MOSFET gate drive output. Connect to the gate of the channel1 low-side synchronous MOSFET through a short, low inductance path. |
| 3 | PGND1 | Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel1 current sense resistor. |
| 4 | CSG1 | Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel1 current sense resistor. |
| 5 | CS1 | Current sense amplifier input. Connect to the high side of the channel1 current sense resistor. |
| 6 | RAMP1 | PWM ramp signal. An external resistor and capacitor connected between the SW1 pin, the RAMP1 pin and the AGND pin sets the channel1 PWM ramp slope. Proper selection of component values produces a RAMP1 signal that emulates the current in the buck inductor. |
| 7 | SS1 | An external capacitor and an internal 10µA current source set the ramp rate of the channel1 error amp reference. The SS1 pin is held low when VCC1 or VCC2 < 4.9V, UVLO < 1.25V or during thermal shutdown. |
| 8 | VCCDIS | Optional input that disables the internal VCC regulators when external biasing is supplied. If VCCDIS >1.25V, the internal VCC regulators are disabled. The externally supplied bias should be coupled to the VCC pins through a diode. VCCDIS has a 500kΩ pull-down resistor to ground to enable the VCC regulators when the pin is left floating. The pull-down resistor can be overridden by pulling VCCDIS above 1.25V with a resistor divider connected to the external bias supply. |
| 9 | FB1 | Feedback input and inverting input of the channel1 internal error amplifier. A resistor divider from the channel1 output to this pin sets the output voltage level. The regulation threshold at the FB1 pin is 0.8V. |
| 10 | COMP1 | Output of the channel1 internal error amplifier. The loop compensation network should be connected between this pin and the FB1 pin. |
| 11 | EN2 | If the EN2 pin is low, channel2 will be disabled. Channel1 and all other functions remain active. The EN2 has a 50kΩ pull-up resistor to enable channel2 when the pin is left floating. |
| 12 | AGND | Analog ground. Return for the internal 0.8V voltage reference and analog circuits. |
| 13 | RT | The internal oscillator is set with a single resistor between RT and AGND. The recommended maximum oscillator frequency is 1.5MHz which corresponds to a maximum switching frequency of 750kHz for either channel. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into RT through a small coupling capacitor. |
| 14 | RES | The restart timer pin for an external capacitor that configures the hiccup mode current limiting. A capacitor on the RES pin determines the time the controller will remain off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel may operate in normal mode while the other is in hiccup mode overload protection. The hiccup mode commences when either channel experiences 256 consecutive PWM cycles with cycle-by-cycle current limiting. After this occurs, a 10µA current source charges the RES pin capacitor to the 1.25V threshold which restarts the overloaded channel. |
| 15 | COMP2 | Output of the channel2 internal error amplifier. The loop compensation network should be connected between this pin and the FB2 pin. |
| 16 | FB2 | Feedback input and inverting input of the channel2 internal error amplifier. A resistor divider from the channel2 output to this pin sets the output voltage level. The regulation threshold at the FB2 pin is 0.8V. |
| 17 | DEMB | Logic input that enables diode emulation when in the low state. In diode emulation mode, the low side MOSFET is latched off for the remainder of the PWM cycle when the buck inductor current reverses direction (current flow from output to ground). When DEMB is high, diode emulation is disabled allowing current to flow in either direction through the low side MOSFET. A 50kΩ pull-down resistor internal to the LM5119 holds DEMB pin low and enables diode emulation if the pin is left floating. |
| 18 | SS2 | An external capacitor and an internal 10µA current source set the ramp rate of the channel2 error amp reference. The SS2 pin is held low when VCC1 or VCC2 < 4.9V, UVLO < 1.25V or during thermal shutdown. |

| Pin | Name | Description |
|---|---|---|
| 19 | RAMP2 | PWM ramp signal. An external resistor and capacitor connected between the SW2 pin, the RAMP2 pin and the AGND pin sets the channel2 PWM ramp slope. Proper selection of component values produces a RAMP2 signal that emulates the current in the buck inductor. |
| 20 | CS2 | Current sense amplifier input. Connect to the high side of the channel2 current sense resistor. |
| 21 | CSG2 | Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel2 current sense resistor. |
| 22 | PGND2 | Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel2 current sense resistor. |
| 23 | LO2 | Low side MOSFET gate drive output. Connect to the gate of the channel2 low-side synchronous MOSFET through a short, low inductance path. |
| 24 | VCC2 | Bias supply pin. Locally decouple to PGND2 using a low ESR/ESL capacitor located as close to controller as possible. |
| 25 | SW2 | Switching node of the buck regulator. Connect to channel2 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. |
| 26 | HO2 | High side MOSFET gate drive output. Connect to the gate of the channel2 high-side MOSFET through a short, low inductance path. |
| 27 | HB2 | High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel2 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to the controller as possible. |
| 28 | UVLO | Under-voltage lockout programming pin. If the UVLO pin is below 0.4V, the regulator will be in the shutdown mode with all function disabled. If the UVLO pin is greater than 0.4V and below 1.25V, the regulator will be in standby mode with the VCC regulators operational, the SS pins grounded and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.25V, the SS pins are allowed to ramp and pulse width modulated gate drive signals are delivered at the LO and HO pins. A 20µA current source is enabled when UVLO exceeds 1.25V and flows through the external UVLO resistors to provide hysteresis. |
| 29 | VIN | Supply voltage input source for the VCC regulators. |
| 30 | HB1 | High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel1 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to controller as possible. |
| 31 | HO1 | High side MOSFET gate drive output. Connect to the gate of the channel1 high-side MOSFET through a short, low inductance path. |
| 32 | SW1 | Switching node of the buck regulator. Connect to channel1 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. |
| EP | EP | Exposed pad of LLP package. No internal electrical connections. Solder to the ground plane to reduce thermal resistance. |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| VIN to AGND | -0.3 to 75V |
| SW1, SW2 to AGND | -3.0 to 75V |
| HB1 to SW1, HB2 to SW2 | -0.3 to 15V |
| VCC1, VCC2 to AGND (Note 2) | -0.3 to 15V |
| FB1, FB2, DEMB, RES, VCCDIS, UVLO to AGND | -0.3 to 15V |
| HO1 to SW1, HO2 to SW2 | -0.3 to HB+0.3V |
| LO1, LO2 to AGND | -0.3 to VCC+0.3V |
| SS1, SS2 to AGND | -0.3 to 7V |
| EN2, RT to AGND | -0.3 to 7V |
| CS1, CS2, CSG1, CSG2 to AGND | -0.3V to 0.3V |
| PGND to AGND | -0.3V to 0.3V |
| ESD Rating HBM (Note 3) | 2kV |
| Storage Temperature | -55°C to +150°C |
| Junction Temperature | +150°C |

## Operating Ratings (Note 1)

| | |
|---|---|
| VIN | 5.5V to 65V |
| VCC | 5.5V to 14V |
| HB to SW | 5.5V to 14V |
| Junction Temperature | -40°C to +125°C |

Note: COMP1, COMP2, RAMP1, and RAMP2 are output pins. As such they are not specified to have an external voltage applied.

## Electrical Characteristics

Limits in standard type are for $T_J$ = 25°C only; limits in boldface type apply over the junction temperature range of -40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 36V, VCC = 8V, VCCDIS = 0V, EN2 = 5V, $R_T$ = 25kΩ, no load on LO and HO. Electrical characteristics are per channel where applicable. See (Note 4) and (Note 5).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VIN Supply** | | | | | | |
| $I_{BIAS}$ | VIN Operating Current | SS1 = SS2 = 0V | | 6 | **7.3** | mA |
| | | VCCDIS = 2V, SS1 = SS2 = 0V | | 400 | **550** | µA |
| $I_{VCC}$ | VCC1 Operating Current | VCCDIS = 2V, SS1 = SS2 = 0V | | 3.9 | **4.5** | mA |
| | VCC2 Operating Current | VCCDIS = 2V, SS1 = SS2 = 0V | | 1.4 | **2.0** | mA |
| $I_{SHUTDOWN}$ | VIN Shutdown Current | UVLO = 0V, SS1 = SS2 = 0V | | 18 | **50** | µA |
| **VCC Regulator** (Note 6) | | | | | | |
| $V_{CC(REG)}$ | VCC Regulation | | **6.77** | 7.6 | **8.34** | V |
| | VCC Regulation | VIN = 6V, No external load | **5.9** | 5.95 | | V |
| | VCC Sourcing Current Limit | VCC = 0V | **25** | 40 | | mA |
| | VCCDIS Switch Threshold | VCCDIS Rising | **1.19** | 1.25 | **1.29** | V |
| | VCCDIS Switch Hysteresis | | | 0.07 | | V |
| | VCCDIS Input Current | VCCDIS = 0V | | -20 | | nA |
| | VCC Under-voltage Threshold | Positive going VCC | **4.7** | 4.9 | **5.2** | V |
| | VCC Under-voltage Hysteresis | | | 0.2 | | V |
| **EN2 Input** | | | | | | |
| $V_{IL}$ | EN2 Input Low Threshold | | | 2.0 | **1.5** | V |
| $V_{IH}$ | EN2 Input High Threshold | | **2.9** | 2.5 | | V |
| | EN2 Input pull-up resistor | | | 50 | | kΩ |
| **UVLO** | | | | | | |
| | UVLO Threshold | UVLO Rising | **1.20** | 1.25 | **1.29** | V |
| | UVLO Hysterisis Current | UVLO = 1.4V | **15** | 20 | **25** | µA |
| | UVLO Shutdown Threshold | | | 0.4 | | V |
| | UVLO Shutdown Hysterisis Voltage | | | 0.1 | | V |
| **Soft Start** | | | | | | |
| | SS Current Source | SS = 0V | **7** | 10 | **13** | µA |
| | SS Pull Down $R_{DSON}$ | | | 10 | | Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Error Amplifier** | | | | | | |
| $V_{REF}$ | FB Reference Voltage | Measured at FB pin, FB = COMP | **0.788** | 0.8 | **0.812** | V |
| | FB Input Bias Current | FB = 0.8V | | 1 | | nA |
| | FB Disable Threshold | Interleaved Threshold | | 2.5 | | V |
| | COMP VOH | Isource = 3mA | **2.8** | | | V |
| | COMP VOL | Isink = 3mA | | | **0.31** | V |
| $A_{OL}$ | DC Gain | | | 80 | | dB |
| $f_{BW}$ | Unity Gain Bandwidth | | | 3 | | MHz |
| **PWM Comparators** | | | | | | |
| $t_{HO(OFF)}$ | Forced HO Off-time | | **220** | 320 | **430** | ns |
| $t_{ON(min)}$ | Minimum HO On-time | $C_{RAMP}$ = 50pF | | 100 | | ns |
| **Oscillator** | | | | | | |
| $f_{SW1}$ | Frequency 1 | $R_T$ = 25kΩ | **180** | 200 | **220** | kHz |
| $f_{SW2}$ | Frequency 2 | $R_T$ = 10kΩ | **430** | 480 | **530** | kHz |
| | RT Output Voltage | | | 1.25 | | V |
| | RT Sync Positive Threshold | | **2.5** | 3.2 | **4** | V |
| | Sync Pulse Minimum Width | | **100** | | | ns |
| **Current Limit** | | | | | | |
| $V_{CS(TH)}$ | Cycle-by-cycle Sense Voltage Threshold (CS - CSG) | RAMP = 0 | **106** | 120 | **134** | mV |
| | CS Bias Current | CS = 0V | | -70 | **-95** | µA |
| | Hiccup Mode Fault Timer | | | 256 | | Cycles |
| **RES** | | | | | | |
| $I_{RES}$ | RES current Source | | | 9.7 | | µA |
| $V_{RES}$ | RES threshold | $C_{RES}$ Charging | **1.20** | 1.25 | **1.30** | V |
| **Diode Emulation** | | | | | | |
| $V_{IL}$ | DEMB Input Low Threshold | | | 2.0 | **1.65** | V |
| $V_{IH}$ | DEMB Input High Threshold | | **2.9** | 2.6 | | V |
| | DEMB Input Pull-Down Resistance | | | 50 | | kΩ |
| | SW Zero Cross Threshold | | | -5 | | mV |
| **LO Gate Driver** | | | | | | |
| $V_{OLL}$ | LO Low-state Output Voltage | $I_{LO}$ = 100mA | | 0.1 | **0.18** | V |
| $V_{OHL}$ | LO High-state Output Voltage | $I_{LO}$ = -100mA, $V_{OHL}$ = VCC - $V_{LO}$ | | 0.17 | **0.26** | V |
| | LO Rise Time | C-load = 1000pF | | 6 | | ns |
| | LO Fall Time | C-load = 1000pF | | 5 | | ns |
| $I_{OHL}$ | Peak LO Source Current | $V_{LO}$ = 0V | | 2.5 | | A |
| $I_{OLL}$ | Peak LO Sink Current | $V_{LO}$ = VCC | | 3.3 | | A |
| **HO Gate Driver** | | | | | | |
| $V_{OLH}$ | HO Low-state Output Voltage | $I_{HO}$ = 100mA | | 0.11 | **0.19** | V |
| $V_{OHH}$ | HO High-state Output Voltage | $I_{HO}$ = -100mA, $V_{OHH}$ = $V_{HB}$ - $V_{HO}$ | | 0.18 | **0.27** | V |
| | HO Rise Time | C-load = 1000pF | | 6 | | ns |
| | HO Fall Time | C-load = 1000pF | | 5 | | ns |
| $I_{OHH}$ | Peak HO Source Current | $V_{HO}$ = 0V, SW = 0, HB = 8V | | 2.2 | | A |
| $I_{OLH}$ | Peak HO Sink Current | $V_{HO}$ = $V_{HB}$ = 8V | | 3.3 | | A |
| | HB to SW Under-voltage | | | 3 | | V |
| | HB DC Bias Current | HB - SW = 8V | | 70 | **100** | µA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | |
| | LO Fall to HO Rise Delay | No load | | 70 | | ns |
| | HO Fall to LO Rise Delay | No load | | 60 | | ns |
| **THERMAL** | | | | | | |
| $T_{SD}$ | Thermal Shutdown | Rising | | 165 | | °C |
| | Thermal Shutdown Hysteresis | | | 25 | | °C |
| $\theta_{JA}$ | Junction to Ambient | | | 40 | | °C/W |
| $\theta_{JC}$ | Junction to Case | | | 4 | | °C/W |

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics Table.

**Note 2:** These pins must not exceed VIN.

**Note 3:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

**Note 4:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production at $T_A$ = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

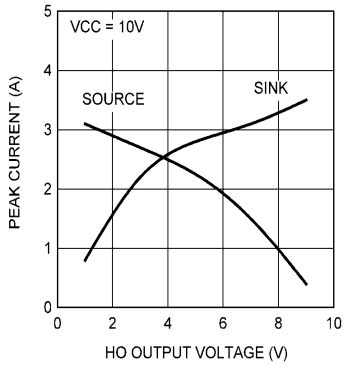
**Note 5:** Typical specifications represent the most likely parametric normal at 25°C operation.

**Note 6:** Per VCC Regulator

LM5119

## Typical Performance Characteristics

**HO Peak Driver Current vs Output Voltage**

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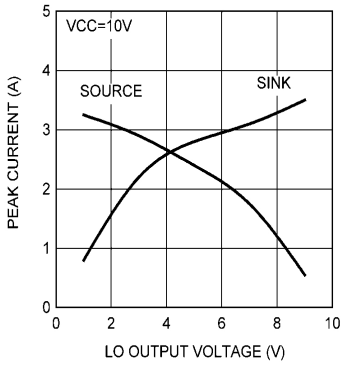
**LO Peak Driver Current vs Output Voltage**

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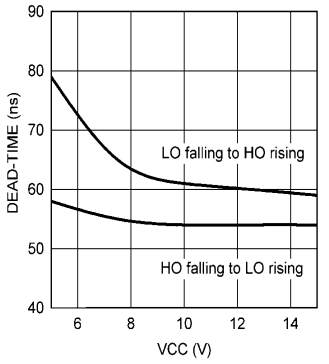
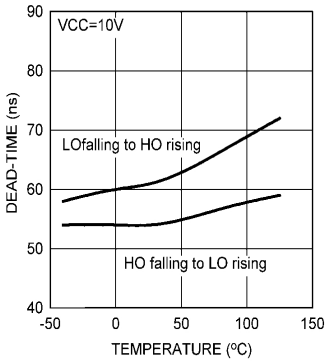
**Driver Dead Time vs VCC**




30124005

**Driver Dead Time vs Temperature**

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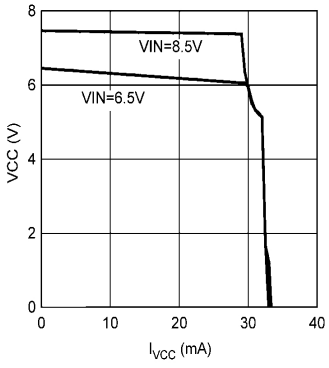
**VCC vs $I_{VCC}$**

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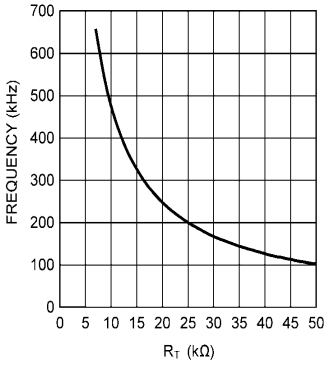
**Switching Frequency vs $R_T$**

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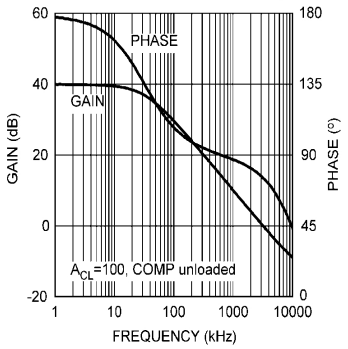
**Error Amp Gain and Phase vs Frequency**

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## Block Diagram

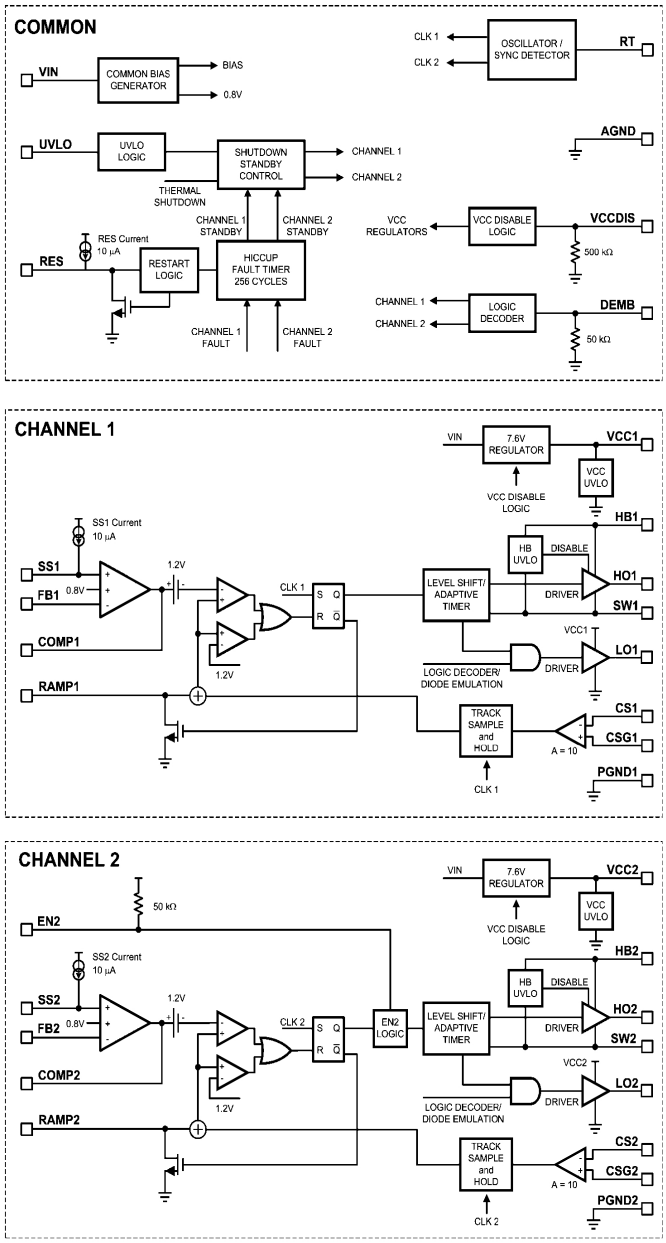



**FIGURE 1. Block Diagram**

## Detailed Operating Description

The LM5119 high voltage switching regulator features all of the functions necessary to implement an efficient dual channel buck regulator that operates over a very wide input voltage range. The LM5119 may be configured as two independent regulators or as a single high current regulator with two interleaved channels. This easy to use regulator integrates high-side and low-side MOSFET drivers capable of supplying peak currents of 2.5 Amps (VCC = 8V). The regulator control method is based on current mode control utilizing an emulated current ramp. Emulated peak current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of the very small duty cycles necessary in high input voltage applications. The switching frequency is user programmable from 50kHz to 750kHz. An oscillator/synchronization pin allows the operating frequency to be set by a single resistor or synchronized to an external clock. An under-voltage lockout and channel2 enable pin allows either both regulators to be disabled or channel2 to be disabled with full operation of channel1. Fault protection features include current limiting, thermal shutdown and remote shutdown capability. The under-voltage lockout input enables both channels when the input voltage reaches a user selected threshold and provides a very low quiescent shutdown current when pulled low. The LLP32 package features an exposed pad to aid in thermal dissipation.

## High Voltage Start-Up Regulator

The LM5119 contains two internal high voltage bias regulators, VCC1 and VCC2, that provide the bias supply for the PWM controllers and gate drive for the MOSFETs of each regulator channel. The input pin (VIN) can be connected directly to an input voltage source as high as 65 volts. The outputs of the VCC regulators are set to 7.6V. When the input voltage is below the VCC set-point level, the VCC output will track the VIN with a small dropout voltage. If VCC1 is in an under voltage condition, channel2 will be disabled. This interdependence is necessary to prevent channel2 from running open loop in the single output interleaved mode when the channel2 error amplifier is disabled (if either VCC is in UV, both channels are disabled).

The outputs of the VCC regulators are current limited at 25mA (minimum) output capability. Upon power-up, the regulators source current into the capacitors connected to the VCC pins. When the voltage at the VCC pins exceed 4.9V and the UVLO pin is greater than 1.25V, both channels are enabled and a soft-start sequence begins. Both channels remain enabled until either VCC pin falls below 4.7V, the UVLO pin falls below 1.25V or the die temperature exceeds the thermal limit threshold.

When operating at higher input voltages the bias power dissipation within the controller can be excessive. An output voltage derived bias supply can be applied to a VCC pins to reduce the IC power dissipation. The VCCDIS input can be used to disable the internal VCC regulators when external biasing is supplied. If VCCDIS >1.25V, the internal VCC regulators are disabled. The externally supplied bias should be coupled to the VCC pins through a diode, preferably a Schottky (low forward voltage). VCCDIS has a 500kΩ internal pull-down resistance to ground for normal operation with no external bias. The internal pull-down resistance can be overridden by pulling VCCDIS above 1.25V through a resistor divider connected to an external bias supply.

The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation.

If the external bias winding can supply VCC greater than VIN, an external blocking diode is required from the input power supply to the VIN pin to prevent the external bias supply from passing current to the input supply through the VCC pins. For VOUT between 6V and 14.5V, VOUT can be connected directly to VCC through a diode. For VOUT < 6V, a bias winding on the output inductor can be added as shown in *Figure 2*.

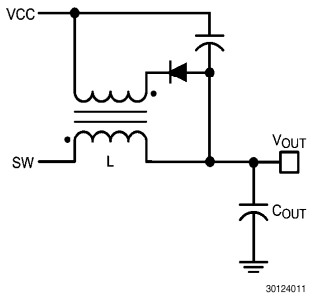



**FIGURE 2. VCC Bias Supply with Additional Inductor Winding**

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 75V. During line or load transients, voltage ringing on the VIN line that exceeds the Absolute Maximum Rating can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and AGND pins are essential.

## UVLO

The LM5119 contains a dual level under-voltage lockout (UVLO) circuit. When the UVLO pin is less than 0.4V, the LM5119 is in shutdown mode. The shutdown comparator provides 100mV of hysteresis to avoid chatter during transitions. When the UVLO pin voltage is greater than 0.4V but less than 1.25V, the controller is in standby mode. In the standby mode the VCC bias regulators are active but the controller outputs are disabled. This feature allows the UVLO pin to be used as a remote enable/disable function. When the VCC outputs exceed their respective under-voltage thresholds (4.9V) and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins.

An external set-point voltage divider from the VIN to GND is used to set the minimum VIN operating voltage of the regulator. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when the input voltage is in the desired operating range. UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 1.25V threshold, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is turned off causing the voltage at the UVLO pin to quickly fall. The UVLO pin should not be left floating.

## Enable 2

The LM5119 contains an enable function allowing shutdown control of channel2, independent of channel1. If the EN2 pin is pulled below 2.0V, channel2 enters shutdown mode. If the EN2 input is greater than 2.5V, channel2 returns to normal operation. An internal 50kΩ pull-up resistor on the EN2 pin allows this pin to be left floating for normal operation. The EN2 input can be used in conjunction with the UVLO pin to sequence the two regulator channels. If EN2 is held low as the UVLO pin increases to a voltage greater than the 1.25V UVLO threshold, channel1 will begin operation while channel2 remains off. Both channels become operational when the UVLO, EN2, VCC1, and VCC2 pins are above their respective operating thresholds. Either channel of the LM5119 can also be disabled independently by pulling the corresponding SS pin to AGND.

## Oscillator and Sync Capability

The LM5119 switching frequency is set by a single external resistor connected between the RT pin and the AGND pin ($R_T$). The resistor should be located very close to the device and connected directly to the pins of the IC (RT and AGND). To set a desired switching frequency ($f_{SW}$) of each channel, the resistor can be calculated from the following equation:

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948 \quad (1)$$

Where RT is in ohms and $f_{SW}$ is in Hertz. The frequency $f_{SW}$ is the output switching frequency of each channel. The internal oscillator runs at twice the switching frequency and an internal frequency divider interleaves the two channels with 180° phase shift between PWM pulses at the HO pins.

The RT pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the RT pin. The voltage at the RT pin is nominally 1.25V and the voltage at the RT pin must exceed 4V to trip the internal synchronization pulse detector. A 5V amplitude signal and 100pF coupling capacitor are recommended. Synchronizing at greater than twice the free-running frequency may result in abnormal behavior of the pulse width modulator. Also, note that the output switching frequency of each channel will be one-half the applied synchronization frequency.

## Error Amplifiers and PWM Comparators

Each of the two internal high-gain error amplifiers generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (0.8V). The output of each error amplifier is connected to the COMP pin allowing the user to provide loop compensation components. Generally a Type II network is recommended. This network creates a pole at 0Hz, a mid-band zero, and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin. Only one error amplifier is required when configuring the controller as a two channel, single output interleaved regulator. For these applications, the channel1 error amplifier (FB1, COMP1) is configured as the master error amplifier. The channel2 error amplifier must be disabled by connecting the FB2 pin to the VCC2 pin. When configured in this manner the output of the channel2 error amplifier (COMP2) will be disabled and have a high output impedance. To complete the interleaved configuration the COMP1 and the COMP2 pins should be connected together to facilitate PWM control of channel2 and current sharing between channels.

## Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulse width. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles are necessary for regulation. The LM5119 utilizes a unique ramp generator which does not actually measure the buck switch current but rather reconstructs the signal. Representing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample-and-hold DC level and the emulated inductor current ramp as shown in *Figure 3*.

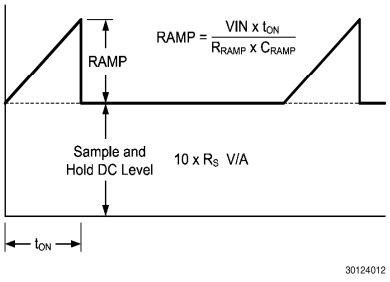



**FIGURE 3. Composition of Current Sense Signal**

The sample-and-hold DC level is derived from a measurement of the recirculating current flowing through the current sense resistor. The voltage across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The current sensing and sample-and-hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from RAMP pin to AGND and a series resistor connected between SW and RAMP. The ramp resistor should not be connected to VIN directly because the RAMP pin voltage rating could be exceeded under high VIN conditions. The ramp created by the external resistor and capacitor will have a slope proportional to the rising inductor current plus some additional slope required for slope compensation. Connecting the RAMP pin resistor to SW provides optimum slope compensation with a RAMP capacitor slope that is proportional to VIN. This "adaptive slope compensation" eliminates the requirement for additional slope compensation circuitry with high output voltage set points and frees the user from additional concerns in this area. The emulated ramp signal is approximately linear and the ramp slope is given by:

$$\frac{dV_{RAMP}}{dt} = \frac{10 \times K \times V_{IN} \times R_S}{L} \quad (2)$$

The factor of 10 in equation (2) corresponds to the internal current sense amplifier gain of the LM5119. The K factor is a constant which adds additional slope for robust pulse-width modulation control at lower input voltages. In practice this constant can be varied from 1 to 3. $R_S$ is the external sense resistor value.

The voltage on the ramp capacitor is given by:

$$V_{RAMP} = V_{IN} \times \left(1 - e^{\frac{t_{PERIOD}}{R_{RAMP} \times C_{RAMP}}}\right) \quad (3)$$

$$V_{RAMP} \approx \frac{V_{IN} \times t_{PERIOD}}{R_{RAMP} \times C_{RAMP}} \quad (4)$$

The approximation is the first order term in a Taylor Series expansion of the exponential and is valid since $t_{PERIOD}$ is small relative to the RAMP pin R-C time constant.

Multiplying (2) by $t_{PERIOD}$ to convert the slope to a peak voltage, and then equating (2) with (4) allows us to solve for $C_{RAMP}$:

$$C_{RAMP} = \frac{L}{10 \times R_S \times K \times R_{RAMP}} \quad (5)$$

Choose either $C_{RAMP}$ or $R_{RAMP}$ and use (5) to calculate the other component.

The difference between the average inductor current and the DC value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. Sub-harmonic oscillation is normally characterized by alternating wide and narrow pulses at the switch node. The ramp equation above contains the optimum amount of slope compensation, however extra slope compensation is easily added by selecting a lower value for $R_{RAMP}$ or $C_{RAMP}$.

## Current Limit

The LM5119 contains a current limit monitoring scheme to protect the regulator from possible over-current conditions. When set correctly, the emulated current signal is proportional to the buck switch current with a scale factor determined by the current limit sense resistor, $R_S$, and current sense amplifier gain. The emulated signal is applied to the current limit comparator. If the emulated ramp signal exceeds 1.2V, the present cycle is terminated (cycle-by-cycle current limiting). Shown in *Figure 4* is the current limit comparator and a simplified current measurement schematic. In applications with small output inductance and high input voltage, the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the sample-and-hold circuit will detect the excess recirculating current before the buck switch is turned on again. If the sample-and-hold DC level exceeds the internal current limit threshold, the buck switch will be disabled and skip pulses until the current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay to a controlled level following any current overshoot.

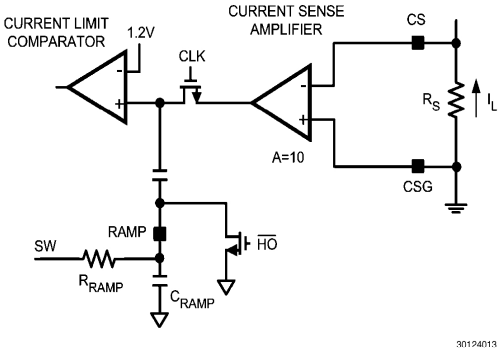



**FIGURE 4. Current Limit and Ramp Circuit**

## Hiccup Mode Current Limiting

To further protect the regulator during prolonged current limit conditions, an internal counter counts the PWM clock cycles during which cycle-by-cycle current limiting occurs. When the counter detects 256 consecutive cycles of current limiting, the regulator enters a low power dissipation hiccup mode with the HO and LO outputs disabled. The restart timer pin, RES, and an external capacitor configure the hiccup mode current limiting. A capacitor on the RES pin ($C_{RES}$) determines the time the controller will remain in low power standby mode before automatically restarting. A 10µA current source charges the RES pin capacitor to the 1.25V threshold which restarts the overloaded channel. The two regulator channels operate independently. One channel may operate normally while the other is in the hiccup mode overload protection. The hiccup mode commences when either channel experiences 256 consecutive PWM cycles with cycle-by-cycle current limiting. If that occurs, the overloaded channel will turn off and remain off for the duration of the RES pin timer.

The hiccup mode current limiting function can be disabled. The RES configuration is latched during initial power-up when UVLO is above 1.25V and VCC1 and VCC2 are above their UV thresholds, determining hiccup or non-hiccup current limiting. If the RES pin is tied to VCC at initial power-on, hiccup current limit is disabled.

## Soft-Start

The soft-start feature allows the regulator to gradually reach the steady state operating point, thus reducing start-up stresses and surges. The LM5119 will regulate the FB pin to the SS pin voltage or the internal 0.8V reference, whichever is lower. At the beginning of the soft-start sequence when SS = 0V, the internal 10µA soft-start current source gradually increases the voltage on an external soft-start capacitor ($C_{SS}$) connected to the SS pin resulting in a gradual rise of the FB and output voltages.

Either regulator channel of the LM5119 can be disabled by pulling the corresponding SS pin to AGND.

## Diode Emulation

A fully synchronous buck regulator implemented with a free-wheel MOSFET rather than a diode has the capability to sink current from the output in certain conditions such as light load, over-voltage or pre-bias startup. The LM5119 provides a diode emulation feature that can be enabled to prevent reverse (drain to source) current flow in the low side free-wheel MOSFET. When configured for diode emulation, the low side MOSFET is disabled when reverse current flow is detected. The benefit of this configuration is lower power loss at no load or light load conditions and the ability to turn on into a pre-biased output without discharging the output. The diode emulation mode allows for start-up into pre-biased loads, since it prevents reverse current flow as the soft-start capacitor charges to the regulation level during startup. The negative effect of diode emulation is degraded light load transient response times. Enabling the diode emulation feature is recommended and allows discontinuous conduction operation. The diode emulation feature is configured with the DEMB pin. To enable diode emulation, connect the DEMB pin to ground or leave the pin floating. If continuous conduction operation is desired, the DEMB pin should be tied to either VCC1 or VCC2.

## HO and LO Output Drivers

The LM5119 contains a high current, high-side driver and associated high voltage level shift to drive the buck switch of each regulator channel. This gate driver circuit works in conjunction with an external diode and bootstrap capacitor. A 0.1µF or larger ceramic capacitor, connected with short traces between the HB pin and SW pin, is recommended. During the off-time of the high-side MOSFET, the SW pin voltage is approximately 0V and the bootstrap capacitor charges from VCC through the external bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 320ns to ensure that the bootstrap capacitor is recharged.

The LO and HO outputs are controlled with an adaptive dead-time methodology which insures that both outputs are never enabled at the same time. When the controller commands HO to be enabled, the adaptive dead-time logic first disables LO and waits for the LO voltage to drop. HO is then enabled after a small delay. Similarly, the LO turn-on is disabled until the HO voltage has discharged. This methodology insures adequate dead-time for any size MOSFET.

Care should be exercised in selecting an output MOSFET with the appropriate threshold voltage, especially if VCC is supplied from the regulator output. During startup at low input voltages the MOSFET threshold should be lower than the 4.9V VCC under-voltage lockout threshold. Otherwise, there may be insufficient VCC voltage to completely turn on the MOSFET as VCC under-voltage lockout is released during startup. If the buck switch MOSFET gate drive is not sufficient, the regulator may not start or it may hang up momentarily in a high power dissipation state. This condition can be avoided by selecting a MOSFET with a lower threshold voltage or if VCC is supplied from an external source higher than the output voltage. If the minimum input voltage programmed by the UVLO pin resistor divider is above the VCC regulation level, this precaution is of no concern.

## Maximum Duty Cycle

When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 320ns to ensure the boot-strap capacitor is recharged and to allow time to sample and hold the current in the low side MOSFET. This forced off-time limits the maximum duty cycle of the controller. When designing a regulator with high switching frequency and high duty cycle requirements, a check should be made of the required maximum duty cycle (including losses) against the graph shown in *Figure 5*.

The actual maximum duty cycle will vary with the operating frequency as follows:

$$D_{MAX} = 1 - f_{SW} \times 320 \times 10^{-9} \quad (6)$$

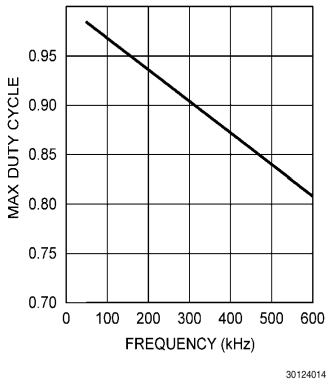



**FIGURE 5. Maximum Duty Cycle vs Switching Frequency**

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the VCC bias regulators. This feature is designed to prevent catastrophic failures from overheating and destroying the device.

## Application Information

### EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. Only the values for the 5V output are calculated since the procedure is the same for the 10V output. The circuit shown in *Figure 14* is configured for the following specifications:

- CH1 output voltage, $V_{OUT1}$ = 10.0V
- CH2 output voltage, $V_{OUT2}$ = 5.0V
- CH1 maximum load current, $I_{OUT1}$ = 4A
- CH2 maximum load current, $I_{OUT2}$ = 8A
- Minimum input voltage, $V_{IN(MIN)}$ = 14V
- Maximum input voltage, $V_{IN(MAX)}$ = 55V
- Switching frequency, $f_{SW}$ = 230kHz

Some component values were chosen as a compromise between the 10V and 5V outputs to allow identical components to be used on both outputs. This design can be reconfigured in a dual-channel interleaved configuration with a single 10V output which requires identical power channels.

### TIMING RESISTOR

$R_T$ sets the switching frequency of each regulator channel. Generally, higher frequency applications are smaller but have higher losses. Operation at 230kHz was selected for this example as a reasonable compromise between small size and high efficiency. The value of $R_T$ for 230kHz switching frequency can be calculated as follows:

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948 = 21.66\ k\Omega \quad (7)$$

A standard value or 22.1kΩ was chosen for $R_T$. The internal oscillator frequency is twice the switching frequency and is about 460kHz.

### OUTPUT INDUCTOR

The inductor value is determined based on the operating frequency, load current, ripple current and the input and output voltages.

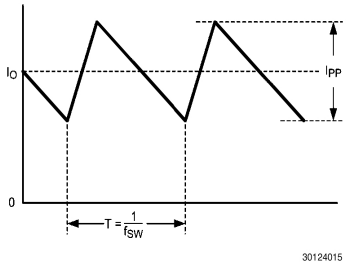



**FIGURE 6. Inductor Current**

Knowing the switching frequency, maximum ripple current ($I_{PP}$), maximum input voltage and the nominal output voltage ($V_{OUT}$), the inductor value can be calculated:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (8)$$

The maximum ripple current occurs at the maximum input voltage. Typically, $I_{PP}$ is 20% to 40% of the full load current. When operating in the diode emulation mode configuration, the maximum ripple current should be less than twice the minimum load current. For full synchronous operation, higher ripple current is acceptable. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple current. For this example, a ripple current of 15% of 8A was chosen as a compromise for the 10V output.

$$L = \frac{5V}{0.15 \times 8A \times 230\ kHz} \times \left(1 - \frac{5V}{55V}\right) = 16.5\ \mu H \quad (9)$$

The nearest standard value of 15µH was chosen for L. Using the value of 15µH for L, calculate $I_{PP}$ again. This step is necessary if the chosen value of L differs significantly from the calculated value.

$$I_{PP} = \frac{V_{OUT}}{L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (10)$$

$$I_{PP} = \frac{5V}{15\ \mu H \times 230\ kHz} \times \left(1 - \frac{5V}{55V}\right) = 1.32A \quad (11)$$

### CURRENT SENSE RESISTOR

Before determining the value of current sense resistor ($R_S$), it is valuable to understand the K factor, which is the ramp slope multiple chosen for slope compensation. The K factor can be varied from 1 to 3 in practice and is defined as:

$$K = \frac{L}{10 \times R_S \times R_{RAMP} \times C_{RAMP}} \quad (12)$$

The performance of the converter will vary depending on the selected K value (See *Table 1*). For this example, 2.5 was chosen as the K factor to minimize the power loss in sense resistor $R_S$ and the cross-talk between channels. Crosstalk between the two regulators under certain conditions may be observed on the output as switch jitter.

The maximum output current capability ($I_{OUT(MAX)}$) should be 20~50% higher than the required output current, (8A at $V_{OUT2}$) to account for tolerances and ripple current. For this example, 120% of 8A was chosen (9.6A). The current sense resistor value can be calculated as:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(MAX)} + \frac{V_{OUT} \times K}{f_{SW} \times L} - \frac{I_{PP}}{2}} \quad (13)$$

$$R_S = \frac{0.12}{9.6A + \frac{5V \times 2.5}{230\ kHz \times 15\ \mu H} - \frac{1.32A}{2}} = 0.0096 \quad (14)$$

Where $V_{CS(TH)}$ is the current limit threshold voltage (120mV). A value of 10mΩ was chosen for $R_S$. The sense resistor must be rated to handle the power dissipation at maximum input voltage when current flows through the free-wheel MOSFET for the majority of the PWM cycle. The maximum power dissipation of $R_S$ can be calculated:

$$P_{RS} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) I_{OUT}^2 R_S \quad (15)$$

$$P_{RS} = \left(1 - \frac{5V}{55V}\right) \times 8^2 \times 0.01 = 0.58W \quad (16)$$

During output short condition, the worst case peak inductor current is limited to:

$$I_{LIM\_PEAK} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(MAX)} t_{ON(MIN)}}{L} \quad (17)$$

$$I_{LIM\_PEAK} = \frac{0.12}{0.01\Omega} + \frac{55V \times 100\ ns}{15\ \mu H} = 12.37A \quad (18)$$

Where $t_{ON(MIN)}$ is the minimum HO on-time which is nominally 100ns. The chosen inductor must be evaluated for this condition, especially at elevated temperature where the saturation current rating of the inductor may drop significantly. At the maximum input voltage with a shorted output, the valley current must fall below $V_{CS(TH)} / R_S$ before the high-side MOSFET is allowed to turn on.

### RAMP RESISTOR AND RAMP CAPACITOR

The value of ramp capacitor ($C_{RAMP}$) should be less than 2nF to allow full discharge between cycles by the discharge switch internal to the LM5119. A good quality, thermally stable ceramic capacitor with 5% or less tolerance is recommended. For this design the value of $C_{RAMP}$ was set at the standard capacitor value of 820pF. With the inductor, sense resistor and the K factor selected, the value of the ramp resistor ($R_{RAMP}$) can be calculated as:

$$R_{RAMP} = \frac{L}{10 \times R_S \times K \times C_{RAMP}} \quad (19)$$

$$R_{RAMP} = \frac{15\ \mu H}{10 \times 0.01\Omega \times 2.5 \times 820\ pF} = 73.2\ k\Omega \quad (20)$$

The standard value of 73.2kΩ was selected.

### OUTPUT CAPACITORS

The output capacitors smooth the inductor ripple current and provide a source of charge during transient loading conditions. For this design example, a 470µF electrolytic capacitor with 10mΩ ESR was selected as the main output capacitor. The fundamental component of the output ripple voltage is approximated as:

$$\Delta V_{OUT} = I_{PP} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \quad (21)$$

$$\Delta V_{OUT} = 1.32A \times \sqrt{0.01\Omega^2 + \left(\frac{1}{8 \times 230\ kHz \times 470\ \mu F}\right)^2} \quad (22)$$

$$\Delta V_{OUT} = 13.3mV \quad (23)$$

Two 22µF low ERS / ESL ceramic capacitors are placed in parallel with the 470µF electrolytic capacitor, to further reduce the output voltage ripple and spikes.

**TABLE 1. Performance Variation by K Factor**

| | K < 1 | 1 <— K —> 3 | | K > 3 |
|---|---|---|---|---|
| **Cross Talk** | Sub-harmonic oscillation may occur | Higher | Lower | Introduces additional pole near cross-over frequency |
| **Peak Inductor Current with Short Output Condition** | | Lower | Higher | |
| **Inductor Size** | | Smaller | Larger | |
| **Power Dissipation of Rs** | | Higher | Lower | |
| **Efficiency** | | Lower | Higher | |

### INPUT CAPACITORS

The regulator input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the buck switch steps to the valley of the inductor current waveform, ramps up to the peak value, and then drops to the zero at turn-off. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$. Seven 2.2µF ceramic capacitors were used for each channel. With ceramic capacitors, the input ripple voltage will be triangular. The input ripple voltage with one channel operating is approximately:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} \quad (24)$$

$$\Delta V_{IN} = \frac{8A}{4 \times 230\ kHz \times 15.4\ \mu F} = 0.565V \quad (25)$$

The ripple voltage of the input capacitors will be reduced significantly with dual channel operation since each channel operates 180 degrees out of phase from the other. Capacitors connected in parallel should be evaluated for RMS current rating. The current will split between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

When the converter is connected to an input power source, a resonant circuit is formed by the line inductance and the input capacitors. To minimize overshoot make $C_{IN} > 10 \times L_{IN}$. The characteristic source impedance ($Z_S$) and resonant frequency ($f_S$) are:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (26)$$

$$f_S = \frac{1}{2\pi\sqrt{L_{IN} \times C_{IN}}} \quad (27)$$

Where $L_{IN}$ is the inductance of the input wire. The converter exhibits negative input impedance which is lowest at the minimum input voltage:

$$Z_{IN} = \frac{V_{IN}^2}{P_{OUT}} \quad (28)$$

The damping factor for the input filter is given by:

$$\delta = \frac{1}{2} \times \left( \frac{R_{IN} + ESR}{Z_S} + \frac{Z_S}{Z_{IN}} \right) \quad (29)$$

Where $R_{IN}$ is the input wiring resistance and ESR is the equivalent series resistance of the input capacitors. When $\delta = 1$, the input filter is critically damped. This may be difficult to achieve with practical component values. With $\delta < 0.2$, the input filter will exhibit significant ringing. If $\delta$ is zero or negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation. When operating near the minimum input voltage, a bulk aluminum electrolytic capacitor across $C_{IN}$ may be needed to damp the input for a typical bench test setup.

### VCC CAPACITOR

The primary purpose of the VCC capacitor ($C_{VCC}$) is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The recommended value of $C_{VCC}$ should be no smaller than 0.47µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 1µF was selected for this design.

### BOOTSTRAP CAPACITOR

The bootstrap capacitor between the HB and SW pins supplies the gate current to charge the high-side MOSFET gate at each cycle's turn-on and recovery charge for the bootstrap diode. These current peaks can be several amperes. The recommended value of the bootstrap capacitor is at least 0.1µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \quad (30)$$

$Q_g$ is the high-side MOSFET gate charge and $\Delta V_{HB}$ is the tolerable voltage droop on $C_{HB}$, which is typically less than 5% of VCC. A value of 0.47µF was selected for this design.

### SOFT START CAPACITOR

The capacitor at the SS pin ($C_{SS}$) determines the soft-start time ($t_{SS}$), which is the time for the output voltage to reach the final regulated value. The value of $C_{SS}$ for a given time is determined from:

$$C_{SS} = \frac{t_{SS} \times 10\ \mu A}{0.8V} \quad (31)$$

For this application, a value of 0.047µF was chosen for a soft-start time of 3.8ms.

### RESTART CAPACITOR

The restart pin sources 10µA into the external restart capacitor ($C_{RES}$). The value of the restart capacitor is given by:

$$C_{RES} = \frac{10\ \mu A \times t_{RES}}{1.25V} \quad (32)$$

Where $t_{RES}$ is the time the LM5119 remains off before a restart attempt in hiccup mode current limiting. For this application, a value of 0.47µF was chosen for a restart time of 59ms.

### OUTPUT VOLTAGE DIVIDER

$R_{FB1}$ and $R_{FB2}$ set the output voltage level, the ratio of these resistors is calculated from:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8V} - 1 \quad (33)$$

1.33kΩ was chosen for $R_{FB1}$ in this design which results in a $R_{FB2}$ value of 6.98kΩ for $V_{OUT2}$ of 5V. A reasonable guide is to select the value of $R_{FB1}$ in the range between 500Ω and 10kΩ. The value of $R_{FB1}$ should be large enough to keep the total divider power dissipation small.

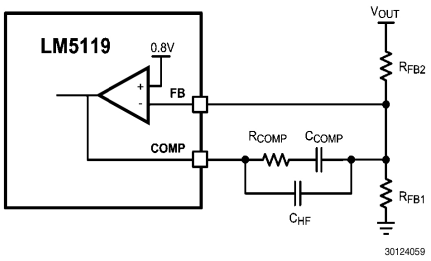



**FIGURE 7. Feedback Configuration**

## UVLO DIVIDER

The UVLO threshold is internally set to 1.25V at the UVLO pin. The LM5119 is enabled when the system input voltage VIN causes the UVLO pin to exceed the threshold voltage of 1.25V. When the UVLO pin voltage is below the threshold, the internal 20µA current source is disabled. When the UVLO pin voltage exceeds the 1.25V threshold, the 20µA current source is enabled causing the UVLO pin voltage to increase, providing hysteresis. The values of $R_{UV1}$ and $R_{UV2}$ can be determined from the following equation:

$$R_{UV2} = \frac{V_{HYS}}{20\ \mu A} \quad (34)$$

$$R_{UV1} = \frac{1.25V \times R_{UV2}}{VIN - 1.25} \quad (35)$$

$V_{HYS}$ is the desired UVLO hysteresis at VIN, and VIN in the second equation is the desired UVLO release (turn-on) voltage. For example, if it is desired for the LM5119 to be enabled when VIN reaches 13.5V, and the desired hysteresis is 1.2V, then $R_{UV2}$ should be set to 60kΩ and $R_{UV1}$ should be set to 6.12kΩ. For this application $R_{UV2}$ was selected to be 60.4kΩ, $R_{UV1}$ was selected to be 6.19kΩ. The LM5119 can be remotely shutdown by taking the UVLO pin below 0.4V with an external open collector or open drain device. The outputs and the VCC regulator are disabled in shutdown mode. Capacitor $C_{FT}$ provides filtering for the divider. A value of 100pF was chosen for $C_{FT}$. The voltage at the UVLO pin should never exceed 15V when using the external set-point divider. It may be necessary to clamp the UVLO pin at high input voltages.

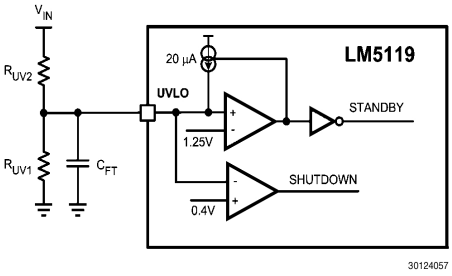



**FIGURE 8. UVLO Configuration**

## MOSFET SELECTION

Selection of the power MOSFETs is governed by the same tradeoffs as switching frequency. Breaking down the losses in the high-side and low-side MOSFETs is one way to compare the relative efficiencies of different devices. When using discrete SO-8 MOSFETs, generally the output current capability range is 2A to 10A. Losses in the power MOSFETs can be broken down into conduction loss, gate charging loss, and switching loss. Conduction loss $P_{DC}$ is approximately:

$$P_{DC\ (HO\text{-}MOSFET)} = D \times (I_O^2 \times R_{DS(ON)} \times 1.3) \quad (36)$$

$$P_{DC\ (LO\text{-}MOSFET)} = (1 - D) \times (I_O^2 \times R_{DS(ON)} \times 1.3) \quad (37)$$

Where, D is the duty cycle and the factor of 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet. Gate charging loss, $P_{GC}$, results from the current driving the gate capacitance of the power MOSFETs and is approximated as:

$$P_{GC} = n \times VCC \times Qg \times f_{SW} \quad (38)$$

Where $Q_g$ refers to the total gate charge of an individual MOSFET, and 'n' is the number of MOSFETs. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM5119 and not in the MOSFET itself. Further loss in the LM5119 is incurred if the gate driving current is supplied by the internal linear regulator. In this example, VCC is supplied from the 10V output through a diode to minimize the loss of the internal linear regulator.

Switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (39)$$

Where $t_R$ and $t_F$ are the rise and fall times of the MOSFET. The rise and fall times are usually mentioned in the MOSFET datasheet or can be empirically observed with an oscilloscope. Switching loss is calculated for the high-side MOSFET only. Switching loss in the low-side MOSFET is negligible because the body diode of the low-side MOSFET turns on before the MOSFET itself, minimizing the voltage from drain to source before turn-on. For this example, the maximum drain-to-source voltage applied to either MOSFET is 55V.The selected MOSFETs must be able to withstand 55V plus any ringing from drain to source, and be able to handle at least the VCC voltage plus any ringing from gate to source. A good choice of MOSFET for the 55V input design example is the PSMN5R5. It has an $R_{DS(ON)}$ of 5.2mΩ and total gate charge of 56nC. In applications where a high step-down ratio is maintained in normal operation, efficiency may be optimized by choosing a high-side MOSFET with lower $Q_g$, and low-side MOSFET with lower $R_{DS(ON)}$.

## MOSFET SNUBBER

A resistor-capacitor snubber network across the low-side MOSFET reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple noise to the output. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50Ω. Increasing the value of the snubber capacitor results in more

damping, but higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at high load. A snubber may not be necessary with an optimized layout.

## ERROR AMPLIFIER COMPENSATION

$R_{COMP}$, $C_{COMP}$ and $C_{HF}$ configure the error amplifier gain characteristics to accomplish a stable voltage loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, $R_{COMP}$ and $C_{COMP}$. The voltage loop gain is the product of the modulator gain and the error amplifier gain. For the 5V output design example, the modulator is treated as an ideal voltage-to-current converter. The DC modulator gain of the LM5119 can be modeled as:

$$DC\_GAIN_{(MOD)} = \frac{R_{LOAD}}{(A \times R_S)} \quad (40)$$

Note that A is the gain of the current sense amplifier which is 10 in the LM5119. The dominant low frequency pole of the modulator is determined by the load resistance ($R_{LOAD}$) and output capacitance ($C_{OUT}$). The corner frequency of this pole is:

$$f_{P(MOD)} = \frac{1}{(2\pi \times R_{LOAD} \times C_{OUT})} \quad (41)$$

For $R_{LOAD}$ = 5V / 8A = 0.625Ω and $C_{OUT}$ = 514µF (effective) then $f_{P(MOD)}$ = 496Hz

DC $Gain_{(MOD)}$ = 0.625Ω / (10 x 10mΩ) = 6.25 = 15.9dB

For the 5.0V design example, the modulator gain vs. frequency characteristic is shown in *Figure 9*.

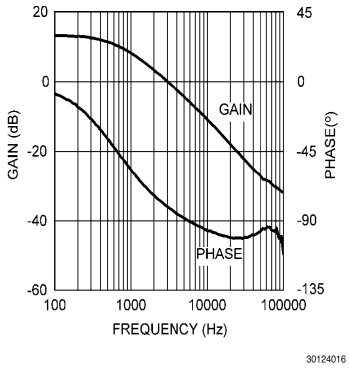



**FIGURE 9. Modulator Gain and Phase**

Components $R_{COMP}$ and $C_{COMP}$ configure the error amplifier as a Type II configuration. The DC gain of the amplifier is 80dB with a pole at 0Hz and a zero at $f_{ZEA}$ = 1 / (2π x $R_{COMP}$ x $C_{COMP}$). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the voltage loop. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin. For the design example, a conservative target loop bandwidth (crossover frequency) of 11kHz was selected. The compensation network zero ($f_{ZEA}$) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of $R_{COMP}$ and $C_{COMP}$ for a desired compensation network zero 1 / (2π x $R_{COMP}$ x $C_{COMP}$) to be about 1.1kHz. Increasing $R_{COMP}$, while proportionally decreasing $C_{COMP}$, increases the error amp gain. Conversely, decreasing $R_{COMP}$ while proportionally increasing $C_{COMP}$, decreases the error amp gain. For the design example $C_{COMP}$ was selected as 6800pF and $R_{COMP}$ was selected as 36.5kΩ. These values configure the compensation network zero at 640Hz. The error amp gain at frequencies greater than $f_{ZEA}$ is: $R_{COMP}$ / $R_{FB2}$, which is approximately 5.22 (14.3dB).

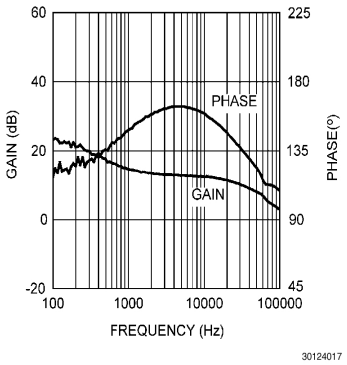



**FIGURE 10. Error Amplifier Gain and Phase**

The overall voltage loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

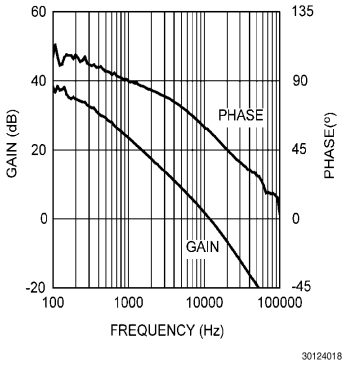



**FIGURE 11. Overall Voltage Loop Gain and Phase**

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If the K factor is between 2 and 3, the stability should be checked with the network analyzer. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. $C_{HF}$ can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of $C_{HF}$ must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well be-

yond the loop crossover frequency. A good approximation of the location of the pole added by $C_{HF}$ is: $f_{P2} = f_{ZEA} \times C_{COMP} / C_{HF}$. The value of $C_{HF}$ was selected as 100pF for the design example.

### MISCELLANEOUS FUNCTIONS

EN2 is left floating which allows channel2 to always remain enabled. If EN2 is pulled below 2V, channel2 is disabled.

The DEMB pin is left floating since this design uses diode emulation. For fully synchronous (continuous conduction) operation, connect the DEMB to a voltage greater than 2.6V.

VCCDIS is left floating to enable the internal VCC regulators. To disable the internal VCC regulators, connect this pin to a voltage greater than 1.25V.

### INTERLEAVED OPERATION

Interleaved operation can offer many advantages in single output, high current applications. The output power path is split between two identical channels reducing the current in each channel by one-half. Ripple current reduction in the output capacitors is reduced significantly since each channel operates 180 degrees out of phase from the other. Ripple reduction is greatest at 50% duty cycle and decreases as the duty cycle varies away from 50%.

Refer to *Figure 12* to estimate the ripple current reduction. Also, the effective ripple in the input and output capacitors occurs at twice the frequency of a single channel design due to the combining of the two channels. All of these factors are advantageous in managing the higher currents and their effects in a high power design.

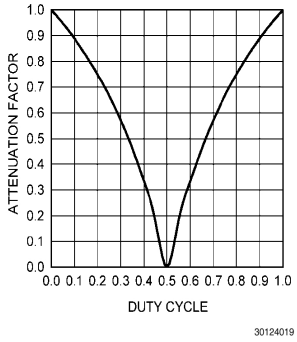



**FIGURE 12. Cancellation Factor vs. Duty Cycle for Output Capacitor**

To begin an interleaved design, use the previous equations in this datasheet to first calculate the required value of components using one-half the current in the output power path. The Attenuation Factor in *Figure 12* is the ratio of the output capacitor ripple to the inductor ripple vs. duty cycle. The inductor ripple used in this calculation is the ripple in either inductor in a two phase design, not the ripple calculated for a single phase design of the same output power. It can be observed that operation around 50% duty cycle results in almost complete ripple attenuation in the output capacitor. *Figure 12* can be used to calculate the amount of ripple attenuation in the output capacitors.

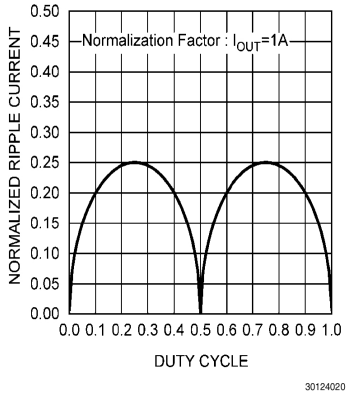
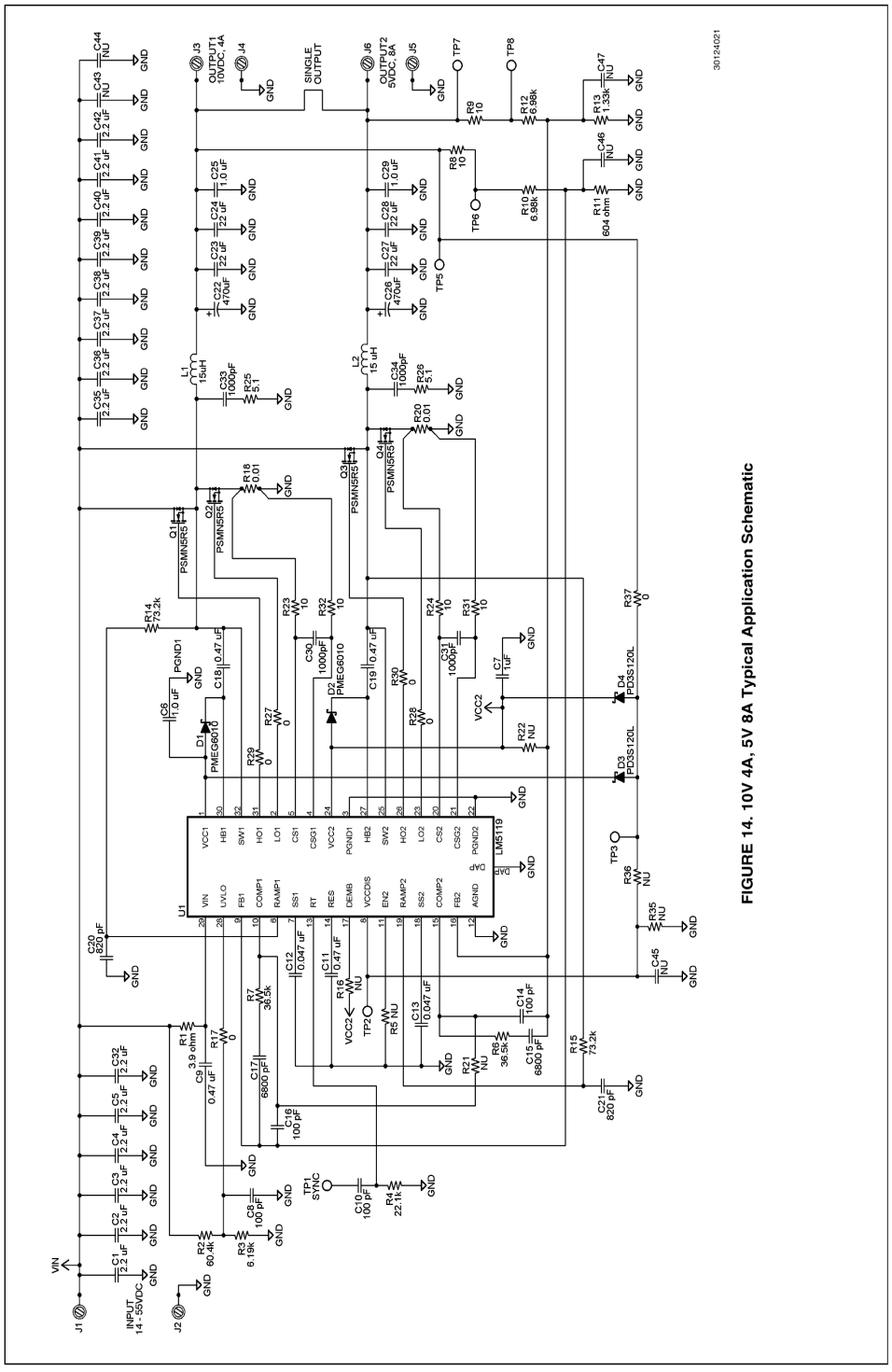



**FIGURE 13. Normalized Input Capacitor RMS Ripple Current vs. Duty Cycle**

*Figure 13* illustrates the ripple current reduction in the input capacitors due to interleaving. As with the output capacitors, there is near perfect ripple reduction near 50% duty cycle. This plot can be used to calculate the ripple in the input capacitors at any duty cycle. In designs with large duty cycle swings, use the worst case ripple reduction for the design.

To configure the LM5119 for interleaved operation, connect COMP1 and COMP2 pins together at the IC. Connecting the FB2 pin to VCC2 pin will disable the channel2 error amplifier with a high output impedance at COMP2. Connect the compensation network between FB1 and the common COMP pins. Connect the two power stages together at the output capacitors. Finally use the plots in *Figure 12* and *Figure 13* along with the duty cycle range to determine the amount of output and input capacitor ripple reduction. Frequently more capacitance than necessary is used in a design just to meet ESR requirements. Reducing the capacitance based solely on ripple reduction graphs alone may violate this requirement.

In the LM5119 evaluation board (schematic shown in *Figure 14*) interleaved operation can be enabled by shorting both outputs together (with identical components in the power train), and using zero ohm resistors for R22 and R21. This shorts VCC2 to FB2 and COMP2 to COMP1 respectively. Also the channel2 feedback network C14, R6, and C15 should be removed. The easy re-configuration between two channel and single channel operation will allow insight into the benefits of interleaved operation.


LM5119
30124021
FIGURE 14. 10V 4A, 5V 8A Typical Application Schematic
21
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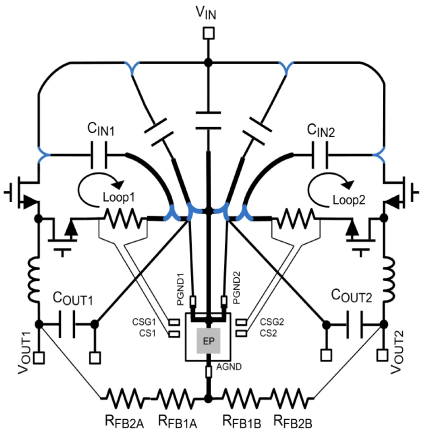
## PCB Board Layout Recommendations

The LM5119 consists of two integrated regulators operating almost independently. Crosstalk between the two regulators under certain conditions may be observed as switch jitter. This effect is common for any dual channel regulator. Crosstalk effects are usually most severe when one channel is operating around 50% duty cycle. Careful layout practices help to minimize this effect. The following board layout guidelines apply specifically to the LM5119 and should be followed for best performance.

1. Keep the Loop1 and Loop2, shown in *Figure 15*, as small as possible
2. Keep the signal and power grounds separate
3. Place VCC capacitors (C6, C7) and VIN capacitor (C9) as closes as possible to the LM5119
4. Route CS and CSG traces together with Kelvin connection to the sense resistor
5. Connect AGND and PGND directly to the underside exposed pad
6. Ensure there are no high current paths beneath the underside exposed pad

**Switching Jitter Root Causes and Solutions**

1. Noise coupling of the high frequency switching between two channels through the input power rail
   - A. Keep the high current path as short as possible
   - B. Choose a FET with minimum lead inductance
   - C. Place local bypass capacitors ($C_{IN1}$, $C_{IN2}$) as close as possible to the high-side FETs to isolate one channel from the high frequency noise of the other channel
   - D. Slow down the SW switching speed by increasing gate resistors R29 and R30
   - E. Minimize the effective ESR/ESL of the input capacitor by paralleling input capacitors
2. High frequency AC noise on FB, CS, CSG and COMP
   - A. Use the star ground PCB layout technique and minimize the length of the high current path
   - B. Keep the signal traces away from the SW, HO, HB traces and the inductor
   - C. Add an R-C filter between the CS and CSG pins
   - D. Place CS filter capacitor (C30, C31) next to the LM5119 and on the same PCB layer as the LM5119
3. Ground offset at the switching frequency
   - A. Use the star ground PCB layout technique and minimize the length between the grounds of $C_{IN1}$and $C_{IN2}$




The bold lines indicate a solid ground plane. Make the traces to the widest and the shortest and use the star ground technique.

These lines indicate the high current paths. Make the traces as wide and short as possible

These lines indicate the small signal paths. The traces can be narrow but keep them away from any radiated noise and away from traces that may couple noise capacitively

These points require the maximum bypassing of the high frequency switching noise. Isolate each channel from the high frequency switching noise of the other channel.

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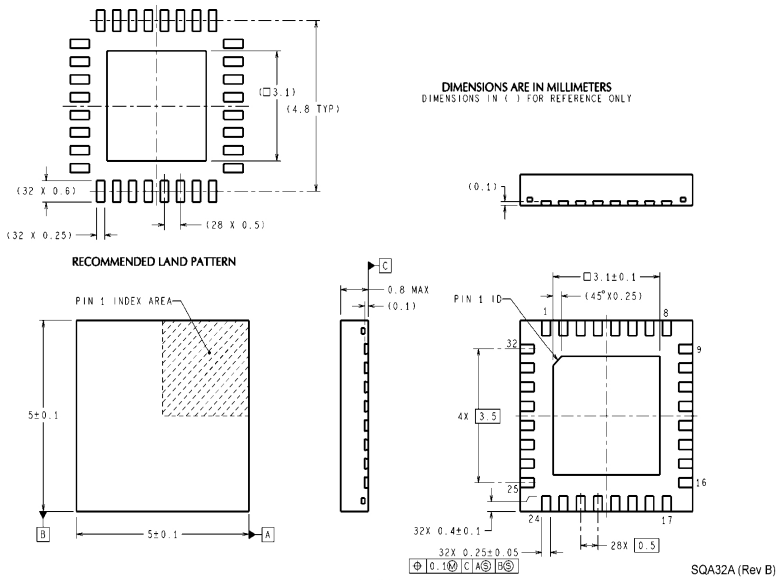
**FIGURE 15. Recommended PCB Layout**

## Physical Dimensions inches (millimeters) unless otherwise noted

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# LM5119 Evaluation Board

National Semiconductor
Application Note 2065
Eric Lee
September 28, 2010

## Introduction

The LM5119EVAL evaluation board provides the design engineer with a fully functional dual output buck converter, employing the LM5119 Dual Emulated Current Mode Synchronous Buck Controller. The evaluation board is designed to provide both 10V and 5V outputs over an input range of 14V to 55V. Also the evaluation board can be easily configured for a single 10V, 8A regulator.

## Performance of the Evaluation Board

- Input Voltage Range: 14V to 55V
- Output Voltage: 10V (CH1), 5V (CH2)
- Output Current: 4A (CH1), 8A (CH2)
- Nominal Switching Frequency: 230 KHz
- Synchronous Buck Operation: Yes
- Diode Emulation Mode: Yes
- Hiccup Mode Overload Protection: Yes
- External VCC Sourcing: Yes

## Powering and Loading Consideration

When applying power to the LM5119 evaluation board, certain precautions need to be followed. A misconnection can damage the assembly.

### PROPER BOARD CONNECTION

The input connections are made to the J1 (VIN) and J2 (RTN/GND) connectors. The CH1 load is connected to the J3 (OUT1+) and J4 (OUT1-/GND) and the CH2 load is connected to the J6 (OUT2+) and J5 (OUT2-/GND). Be sure to choose the correct connector and wire size when attaching the source power supply and the load.

### SOURCE POWER

The power supply and cabling must present low impedance to the evaluation board. Insufficient cabling or a high impedance power supply will droop during power supply application with the evaluation board inrush current. If large enough, this droop will cause a chattering condition during power up. During power down, insufficient cabling or a high impedance power supply will overshoot. This overshoot will cause a non-monotonic decay on the output.

An additional external bulk input capacitor may be required unless the output voltage droop/overshoot of the source power is less than 0.7V. In this board design, UVLO setting is conservative while UVLO hysteresis setting is aggressive. Minimum input voltage can goes down with an aggressive design. Minimum operating input voltage depends on the output voltage droop/overshoot of the source power supply and the forced off-time of the LM5119. Refer to the LM5119 datasheet for complete design information.

### LOADING

When using an electronic load, it is strongly recommended to power up the evaluation board at light load and then slowly increase the load. If it is desired to power up the evaluation board at maximum load, resistor banks must be used. In general, electronic loads are best suited for monitoring steady state waveforms.

### AIR FLOW

Prolonged operation with high input voltage at full power will cause the MOSFETs to overheat. A fan with a minimum of 200LFM should be always provided.

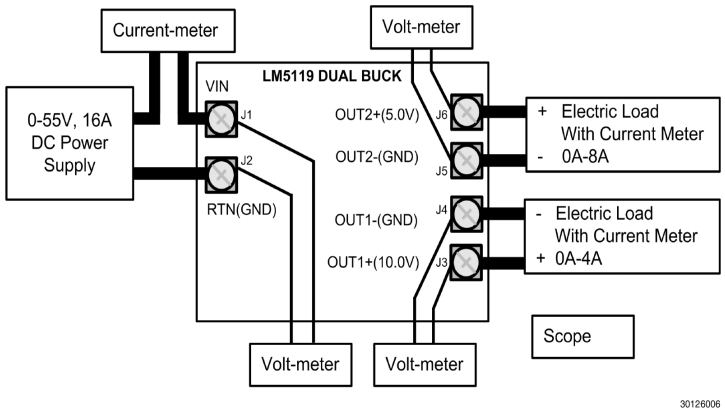


**FIGURE 1. Typical Evaluation Setup**

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### QUICK START-UP PROCEDURE

**STEP 1:** Set the power supply current limit to at least 16A. Connect the power supply to J1 and J2.

**STEP 2:** Connect one load with a 4A capacity between J3 and J4. Connect another load with an 8A capacity between J6 and J5.

**STEP 3:** Set input voltage to 24V and turn it on.

**STEP 4:** Measure the output voltages. CH1 should regulate at 10V and CH2 should regulate at 5V.

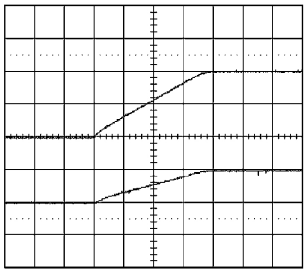
**STEP 5:** Slowly increase the load current while monitoring the output voltages. The outputs should remain in regulation up to full load current.

**STEP 6:** Slowly sweep the input voltage from 14V to 55V while monitoring the output voltages. The outputs should remain in regulation.

## Waveforms

### SOFT START

When applying power to the LM5119 evaluation board a certain sequence of events occurs. Soft-start capacitors and other components allow for a linear increase in output voltages. The soft-start time of each output can be controlled independently. *Figure 2* shows the output voltage during a typical start-up with a load of 3Ω on the 10V output, and 1Ω on the 5V output, respectively.



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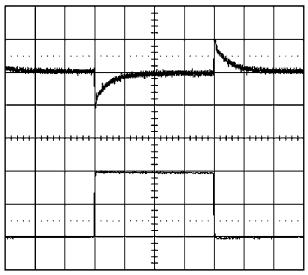
**Conditions:**
Input Voltage = 24VDC
3Ω Load on 10V output
1Ω Load on 5V output
**Traces:**
Top Trace: 10V Output Voltage, Volt/div = 5V
Bottom Trace: 5V Output Voltage, Volt/div = 5V
Horizontal Resolution = 1 ms/div

**FIGURE 2. Start-Up with Resistive Load**

### LOAD TRANSIENT

*Figure 3* shows the transient response for a load of change from 2A to 6A on 5V output. The upper waveform shows output voltage droop and overshoot during the sudden change in output current shown by the lower waveform.



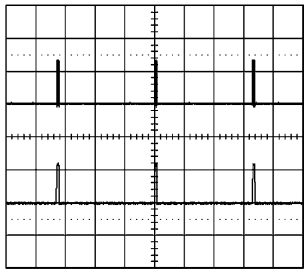
30126008

**Conditions:**
Input Voltage = 24VDC
Output Current 2A to 6A
**Traces:**
Top Trace: 5V Output Voltage, Volt/div = 100mV, AC coupled
Bottom Trace: Output Current, Amp/div = 2A
Horizontal Resolution = 0.5 ms/div

**FIGURE 3. Load Transient Response**

### OVERLOAD PROTECTION

The evaluation board is configured with hiccup mode overload protection. The restart time can be programmed by C11. *Figure 4* shows hiccup mode operation in the event of an output short on CH2 output. One channel may operate in the normal mode while the other is in hiccup mode overload protection.



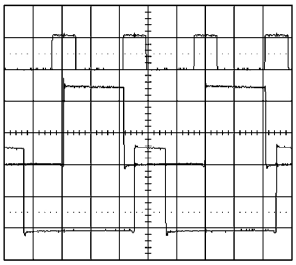
30126009

**Conditions:**
Input Voltage = 24VDC
Output Short on 5V
**Traces:**
Top Trace: SW Voltage on CH2, Volt/div = 20V
Bottom Trace: Inductor Current, Amp/div = 10A
Horizontal Resolution = 20 ms/div

**FIGURE 4. Short Circuit**

### EXTERNAL CLOCK SYNCHRONIZATION

A TP1 (SYNC) test point has been provided on the evaluation board in order to synchronize the internal oscillator to an external clock. *Figure 5* shows the synchronized switching operation. Each channel operates 180 degrees out of phase from the other.



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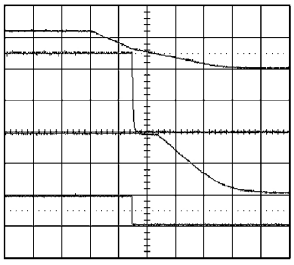
**Conditions:**
Input Voltage = 24VDC
4A on 10V Output
8A on 5V Output
**Traces:**
Top Trace: SYNC pulse, Volt/div = 5V
Middle Trace: SW voltage on CH1, Volt/div = 10V
Bottom Trace: SW voltage on CH2, Volt/div = 10V
Horizontal Resolution = 1 µs/div

**FIGURE 5. Clock Synchronization**

### SHUTDOWN

*Figure 6* shows the shutdown procedure by powering off the source power. When UVLO pin voltage is less than 1.26V, the switching stops and soft-start capacitors are discharged by internal switches.



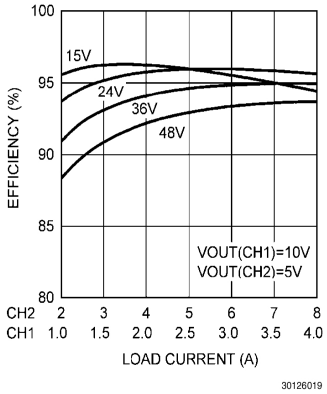
30126018

**Conditions:**
Input Voltage = 24VDC
1Ω Load on 5V Output
**Traces:**
Top Trace: Input Voltage, Volt/div = 20V
Middle Trace1: 5V Output, Volt/div = 2V
Middle Trace2: VCC, Volt/div = 5V
Bottom Trace: SS Voltage, Volt/div = 5V
Horizontal Resolution = 20 ms/div

**FIGURE 6. Shutdown**

## Performance Characteristics

*Figure 7* shows the efficiency curves. The efficiency of the power converter is 96% at 24V with full load current. Monitor the current into and out of the evaluation board. Monitor the voltage directly at the input and output terminals of the evaluation board.




30126019

**FIGURE 7. Typical Efficiency vs Load Current**

## Board Configuration

### INTERLEAVED BUCK OPERATION FOR SINGLE 10V 8A OUTPUT

The evaluation board is designed to be easily converted to a 10V, 8A single output regulator with the interleaved operation. Proper electronic load connection is shown in *Figure 8*. Connecting the electronic load at the center of shorting bar is recommended to prevent a voltage difference between CH1 and CH2 output. In order to produce a single 10V output with 8A maximum output current, populate R21 and R22 with 0Ω resistor and open R6, C15 and C14. The electronic load should have over 8A capability to test the interleaved operation.

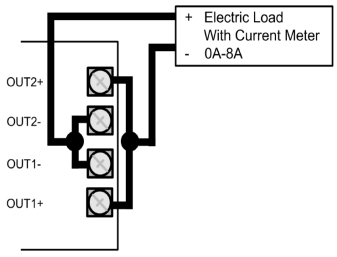



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**FIGURE 8. Load Connection for Single Output**

### EXTERNAL VCC SUPPLY & VCC DISABLE

External VCC supply helps to reduce the temperature and the power loss of the LM5119 at high input voltage. By populating D3 and D4, VCC can be supplied from an external power supply. Use TP3 as an input of the external VCC supply with 0.1A current limit. R36, R35 and C45 should be populated with proper value when the voltage of the external VCC is smaller than 7V. The voltage at the VCCDIS pin can be monitored at TP2. To prevent a reverse current flow from VCC to VIN through the internal diode, the external VCC voltage should always be lower than VIN. In this LM5119 evaluation board, VCC1 and VCC2 are supplied from the 10V output to achieve high efficiency.

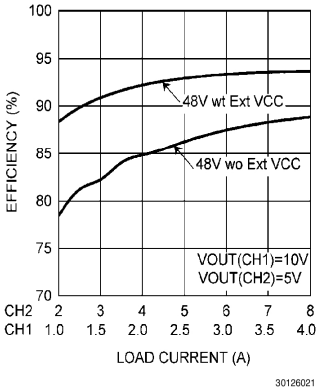



**FIGURE 9. Efficiency Comparison at 48V with External VCC vs Without External VCC**

### LOOP RESPONSE

TP5 and TP6 (TP7 and TP8) have been provided in order to measure the loop transfer function of CH1 (CH2). Refer to AN-1889 for detail information about the loop transfer function measurement.

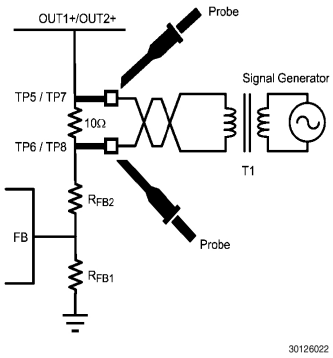
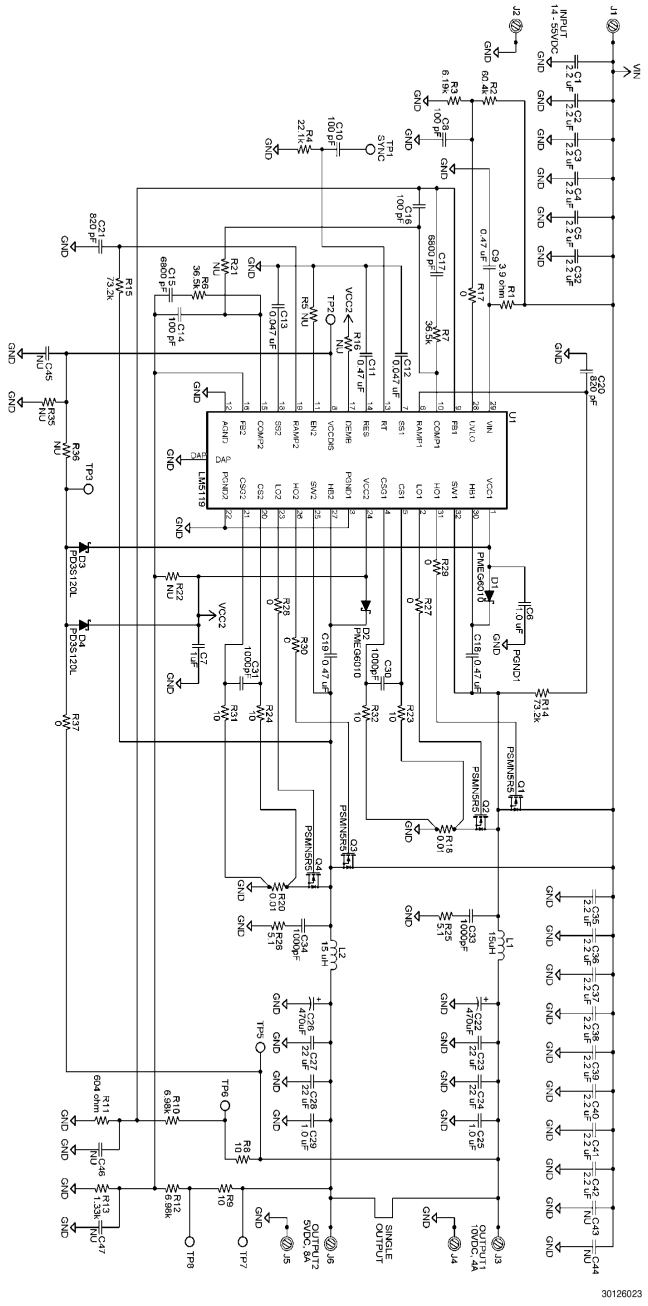



**FIGURE 10. Loop Response Measurement Setup**

## Evaluation Board Schematic



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## Bill of Materials

| Part | Value | Package | Part Number | Manufacturer |
|---|---|---|---|---|
| C1, C2, C3, C4,C5, C32, C35,C36, C37, C38, C39, C40, C41, C42 | 2.2µF, 100V, X7R | 1210 | C3225X7R2A225K | TDK |
| C6, C7, C25,C29 | 1µF, 16V, X7R | 0603 | C1608X7R1C105K | TDK |
| C8, C10, C14, C16 | 100pF, 50V, C0G | 0603 | C1608C0G1H101J | TDK |
| C9 | 0.47µF, 100V, X7R | 0805 | GRM21BR72A474KA73 | Murata |
| C11, C18, C19 | 0.47µF, 25V, X7R | 0603 | GRM188R71E474KA12 | Murata |
| C12,C13 | 0.047µF, 16V, X7R | 0603 | C1608X7R1C473K | TDK |
| C15,C17 | 6800pF, 25V, C0G | 0603 | C1608C0G1E682J | TDK |
| C20,C21 | 820pF, 50V, C0G | 0603 | C1608C0G1H821J | TDK |
| C22,C26 | 470µF, 16V | Φ10 | PCG1C471MCL1GS | Nichicon |
| C23,C24,C27,C28 | 22µF,16V, X7R | 1210 | C3225X7R1C226K | TDK |
| C30,C31 | 1000pF, 50V, X7R | 0603 | C1608X7R1H102K | TDK |
| C33,C34 | 1000pF,100V, C0G | 0805 | C2012C0G2A102J | TDK |
| C43,C44,C45,C46,C47 | NU | | | |
| R1 | 3.9 ohm, 5% | 0805 | CRCW08053R90JNEA | Vishay |
| R2 | 60.4k, 1% | 0805 | CRCW080560K4FKEA | Vishay |
| R3 | 6.19k, 1% | 0603 | CRCW06036K19FKEA | Vishay |
| R4 | 22.1k, 1% | 0603 | CRCW060322K1FKEA | Vishay |
| R5,R16,R21,R22,R35, R36 | NU | | | |
| R6,R7 | 36.5k, 1% | 0603 | CRCW060336K5FKEA | Vishay |
| R8,R9,R23,R24,R31, R32 | 10 ohm, 5% | 0805 | CRCW080510R0JNEA | Vishay |
| R10,R12 | 6.98k, 1% | 0805 | CRCW08056K98FKEA | Vishay |
| R11 | 604 ohm, 1% | 0805 | MCR10EZHF6040 | Rohm |
| R13 | 1.33k, 1% | 0805 | MCR10EZHF1331 | Rohm |
| R14,R15 | 73.2k, 1% | 0603 | CRCW060373K2FKEA | Vishay |
| R17,R37 | 0 ohm | 0603 | MCR03EZPJ000 | Rohm |
| R18,R20 | 0.01 ohm, 1W, 1% | 0815 | RL3720WT-R010-F | Susumu |
| R25,R26 | 5.1 ohm, 1W, 1% | 2512 | ERJ-1TRQF5R1U | Panasonic — ECG |
| R27,R28,R29,R30 | 0 ohm | 0805 | MCR10EZPJ000 | Rohm |
| D1,D2 | 60V, 1A | SOD123F | PMEG6010CEH | NXP |
| D3,D4 | 20V, 1A | PowerDI323 | PD3S120L | Diodes |
| L1,L2 | 15µH, 14A | 18.2x18.3 | 74435571500 | WE |
| Q1,Q3, Q2,Q4 | 60V, 100A | LFPAK SO-8 | PSMN5R5-60YS | NXP |
| U1 | | LLP32 | LM5119 | NSC |
| J1,J2,J3,J4,J5,J6 | 15A | | 7693 | Keystone |
| TP1,TP2,TP3 | | Φ0.1 | 5002 | Keystone |
| TP5,TP6,TP7,TP8 | | | 1040 | Keystone |

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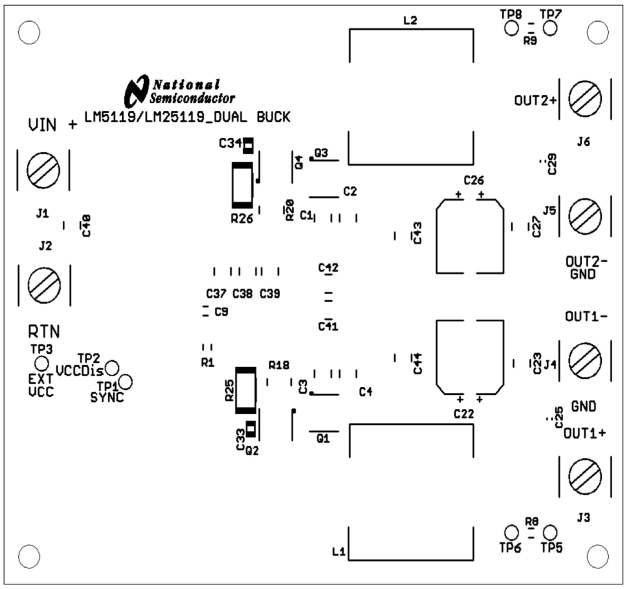
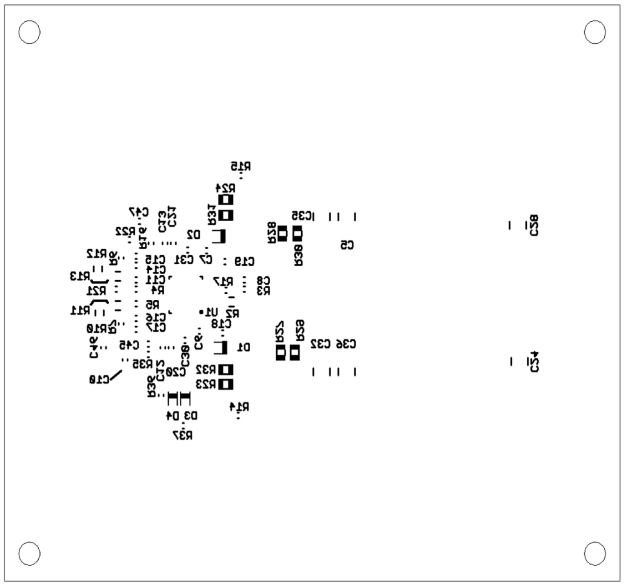
## PCB Layout



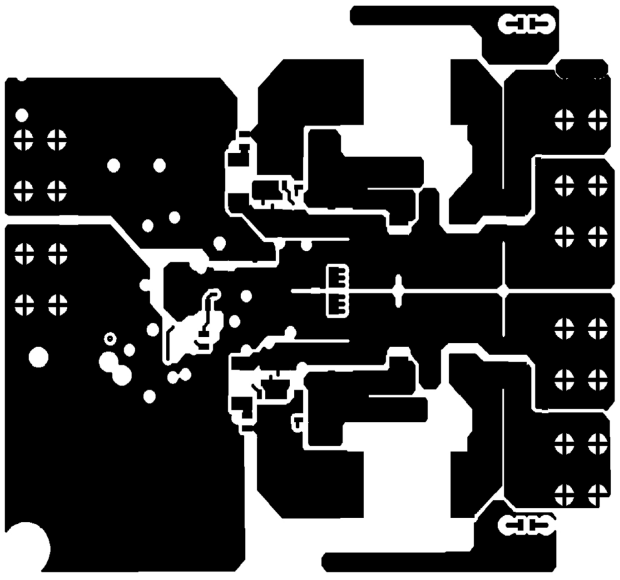

TOP SILKSCREEN (.PLC) AS VIEWED FROM TOP

30126011



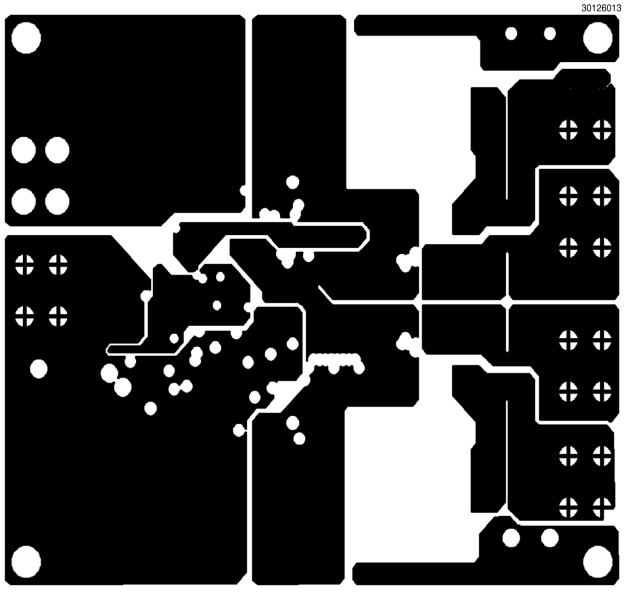
BOTTOM SILKSCREEN (.PLS) AS VIEWED FROM TOP

30126012



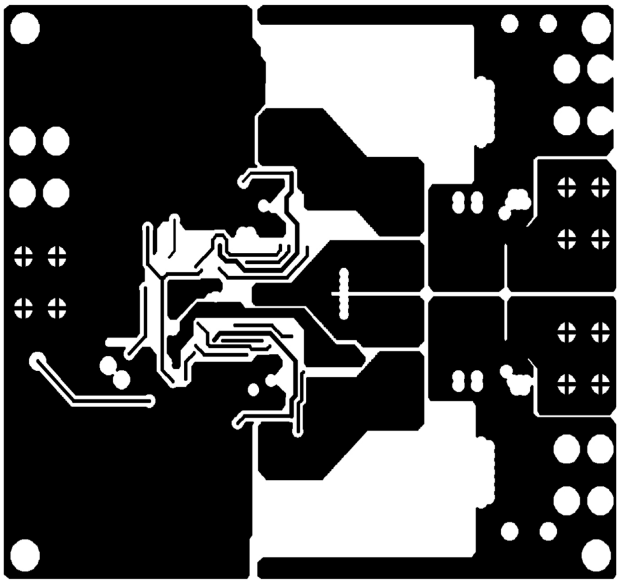
TOP COMPONENT LAYER (.CMP) AS VIEWED FROM TOP

30126013



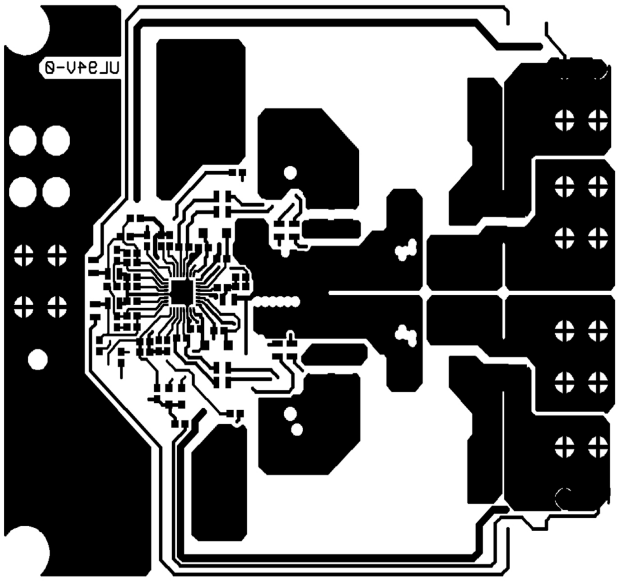
LAYER 2 (.LY2) AS VIEWED FROM TOP

30126014



LAYER 3 (.LY3) AS VIEWED FROM TOP

30126015



BOTTOM SOLDER LAYER (.SOL) AS VIEWED FROM TOP

30126016

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LM5119 Evaluation Board

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| LED Lighting | www.national.com/led | Feedback/Support | www.national.com/feedback |
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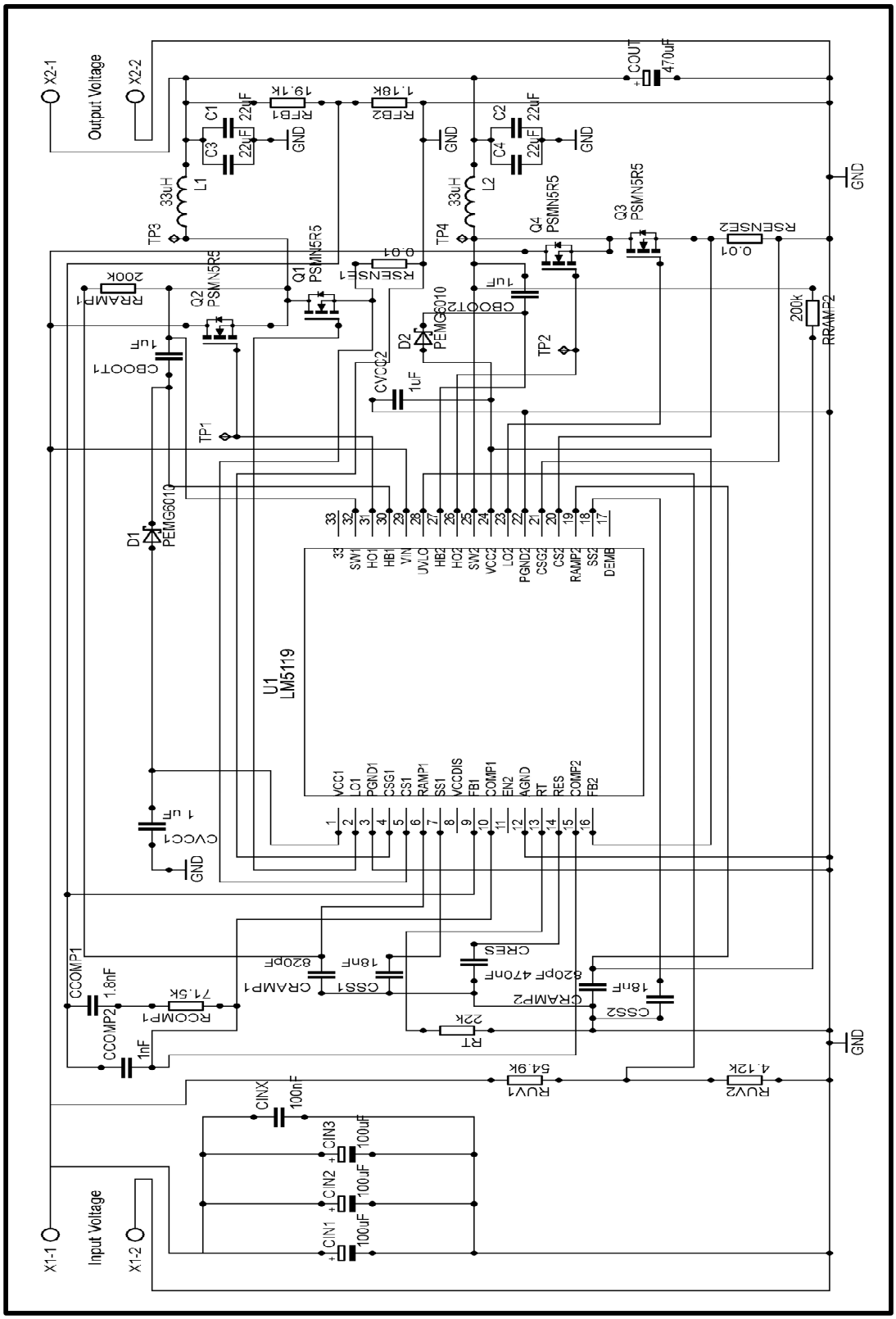
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Output Voltage
X2-2
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470uF
C1
22uF
C3
22uF
RFB1
19.1K
RFB2
1.18K
GND
C2
22uF
C4
22uF
L1
33uH
L2
33uH
TP3
TP4
Q4
PSMN5R5
Q3
PSMN5R5
RSENSE2
0.01
RSENSE1
0.01
Q1
PSMN5R5
Q2
PSMN5R5
RRAMP1
200K
CBOOT2
1uF
D2
PEMG3010
TP2
CBOOT1
1uF
CVCC2
1uF
TP1
RRAMP2
200k
D1
PEMG6010
U1
LM5119
SW1
HO1
HB1
VIN
UVLO
HB2
HO2
SW2
VCC2
LO2
PGND2
CSG2
CS2
RAMP2
SS2
DEMB
VCC1
LO1
PGND1
CSG1
CS1
RAMP1
SS1
VCCDIS
FB1
COMP1
EN2
AGND
RT
RES
COMP2
FB2
CVCC1
1 uF
CCOMP1
1.8nF
RCOMP1
71.5K
CCOMP2
1nF
CRAMP1
820pF
CSS1
18nF
CRES
820pF 470nF
CRAMP2
CSS2
18nF
RT
22k
RUV1
54.9K
RUV2
4.12K
CINX
100nF
CIN3
100uF
CIN2
100uF
CIN1
100uF
X1-1
Input Voltage
X1-2