Development of a universal bidirectional galvanic isolated switch module for power converter applications

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A dissertation submitted in fulfilment of the requirements for the Magister Technologiae: Engineering: Electrical

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Date: June 2013

Declaration

I, Kopano Mokhalodi, hereby declare that the following research information is solely my own work. This is submitted for the requirements of the Magister Technologiae: Engineering: Electrical to the Department of Electronics and Engineering at the Vaal University of Technology, Vanderbijlpark. This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

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Mokhalodi Kopano

Date: ……..

Acknowledgements

I hereby wish to express my gratitude to:

- Prof H C vZ Pienaar for his continued encouragement and guidance.

- Dr JF Janse van Rensburg for his wisdom and contribution that helped me.

- Personnel of the Department of Applied Electronics and Electronic Communication Telkom Centre of Excellence and my fellow colleagues for their support and encouragement.

- Telkom South Africa Ltd, TFMC Pty Ltd, M-TEC and THRIP for the financial assistance towards the research projects.

- My whole family for always being there for me.

Dedication

This project is dedicated to my whole family which has always been my pillar of strength.

Abstract

The global trends towards energy efficiency have facilitated the need for technological advancements in the design and control of power electronic converters for energy processing. The proposed design is intended to make the practical implementation of converters easier.

The development of a universal bidirectional galvanic isolated switch module will be used to drive any MOSFET or IGBT in any position in any topology whether the load is AC or DC. Semiconductor switches are required and are also integrated for fast switching times in power converter applications.

The structure of the power switch module consists of an opto-coupler which will provide an isolation barrier for maximum galvanic isolation between the control circuitry and power stage. It also consists of a high performance gate drive circuit for high speed switching applications with a floating supply.

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Glossary of abbreviations and symbols

A

A - Amperes

AC - Alternating current

B

BJT - Bipolar junction transistor

C

° C - Degrees Celsius

D

DC - Direct current

E

ESR- Equivalent series resistance

EMI - Electromagnetic interference

F

F - Farad

FC - Fuel cell

H

H - Henry

I

I_O - Output current

IGBT – Insulated-gate bipolar transistor

J

J - Joule

K

kW - Kilowatts

M

μ - Micro, 10^{-6}

mA - Milliamps

MOSFET - Metal-oxide semiconductor field effect transistor

N

η - Efficiency

O

Ω - Ohm

P

PWM - Pulse-width modulation

Q

q - Charge of an electron, 1.062×10^{-19}

R

R - Resistance

S

s - Second

T

t_{OFF} - OFF-time of a switch

t_{ON} - ON-time of a switch

V

V - Volts

V_D - Voltage across a diode

V_{DC} - Direct current voltage

V_{IN} - Input voltage

V_O - Output voltage

W

W – Watts

Definition of terms

Algorithm: An ambiguous description of a finite set of operations for solving a computational problem in a finite amount of time.

Bidirectional: Capability to block the voltage and to conduct current in both directions.

Chopping: A technique of rapidly switching ON and OFF a source of voltage.

Fuel cell: A device that produces electricity through an electrochemical process, usually from hydrogen and oxygen.

Galvanic isolation: The principle of isolating functional sections of electrical systems to prevent current flow, no metallic conduction path is permitted.

Nomograph: Alignment chart or abaque, which can be used for graphically calculating the resistance or used to estimate resistance or capacitance points at various frequencies.

Pulse width modulation: A powerful technique for controlling analog circuits with a microprocessor's digital outputs, employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

Renewable energy: A form of energy which is never exhausted because it is renewed by nature.

Uninteruptable power supply: An electrical apparatus that provides emergency power to a load when the input power source typically mains power, fails.

Chapter 1 Introduction

1.1 Background

It is clear that rapid technology evolution coupled with the population explosion has resulted in an increase in average electrical power use (Kularatna 1998:2). This magnitude of growth increases the global energy demand for electricity and with the limited sources of fossil fuels (oil, gas, coal) which have traditionally provided this energy, depleting, the world has turned to the use of renewable energy as the targeted energy market, example being Fuel Cells (FC) (Archer & Hill 2001:16).

These global trends towards energy efficiency have forced researchers to come up with technological advancements in the design and control of power electronic converters for energy processing (Khan 2007:543). According to Khan (2007:543) these power electronic converters can be used in a variety of applications such as:

- Consumer electronics

  Telecommunications equipment, cellular, telephones, cameras charging and computer power supplies,
- Automobile industries

  Electronic ignitions and lighting,
- Commercial sectors

  Variable speed motor drives for conveyor belt systems, heating, installations for metals processing, uninterruptible power supplies (UPS) and industrial welding,
- Domestic electronics

  Fluorescent, compact fluorescent and incandescent lighting, washing machines, cooking appliances, and dishwashers,
- Utility applications

  DC transmission lines for electrification purposes.

According to (Rashid 2001:xi) all these applications utilise similar power converter

topologies which allow for controlled and efficient power conversion from one form of energy to another, utilising semiconductor technologies such as BJT transistors, SCRs (thyristors), IGBTs and power MOSFETs. Kularatna (1998:2) as quoted by Rashid (2004:1) described these power conversion electronics "as a group of electrical and electronic components arranged to form an electric circuit or group of circuits for the purpose of modifying or controlling electric power from one form to another."

Khan (2007:543) refers to Pirelli Tyres who coined the phrase "Power is nothing without control." Khan (2007:549) also stresses the point that this gate drive circuitry of a power converter should be considered as an important enabling interface between the power electronics and the control stage. It is therefore of utmost importance that researchers and engineers pay much attention in the design of this interface between the control and power electronics, since it can have a substantial impact on the performance and reliability of a power electronic system (Khan 2007:549).

As Kularatna (1998:1) states "the core of most power electronic apparatus consists of a converter using power semiconductor switching devices that work under the guidance of control electronics." From the electrical point of view, these power converters can be classified as rectifiers (AC-DC converters), inverters (DC-AC converters), DC-DC converters or an AC power controllers running at the same frequency (Mohan, Undeland & Robbins 2003:703).

The motivation for using switching devices in a converter is to increase the conversion efficiency to a high value. Power electronics can be described as an area where anything from few watts to over several hundred megawatts order powers are controlled by semiconductor controlled elements (Mohan *et al* 2003:703). These semiconductor devices are close to ideal switching, i.e. they must either be completely ON or completely OFF. In the ON-state the voltage across the switch should ideally be zero, independent of the current. In the OFF-state the opposite must hold true, with zero current independent of the voltage (Grant & Gower 1989:17).

According to Rashid (2004:777) a semiconductor switch is sometimes used where no terminal is connected to the ground potential and it is thus said to be floating. This floating gate drive supply is used to ensure full gate control for indefinite periods of time. A level shifter must also be provided that can sustain full voltage with minimal propagation delays and lower power consumption (Janse van Rensburg 2012:282). The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency (International rectifier 2009). The control circuit supplies a logic signal (0 to 5 V) that indicates when the semiconductor switches must be ON and when they must be OFF. However, most semiconductor switches usually do not accept logic level signals therefore a drive circuit is needed to convert the logic signals to appropriate electrical signal levels (Khan 2007:546).

If the switch is used in a completely different electrical circuit where high voltages and currents are the norm, these high voltage levels may be disastrous to the control circuit and therefore there must be galvanic isolation between the control circuit and the power circuit. This electrical isolation between the control and the drive circuits can be provided by making use of an opto-coupler (Mohan *et al.* 2003:703). Also when switches are used in circuits where they are complementary they may not be ON simultaneously or else they will be destroyed (Mohan *et al* 2003:706).

1.2 Problem statement

Researchers and designers of solid state power converters all encounter the same problem, i.e. the gate drive circuitry between the control circuit and each semiconductor power device has to be custom designed for the application and the position of the device in the topology. This leads to many hours being spent on optimizing a gate drive for the specific device instead of solving the control algorithms required.

1.3 Objectives of the research

The main objective of this research is the development of a universal bidirectional

galvanic isolated switch module which can be used to drive any MOSFET or IGBT in any position in any topology whether the load is AC or DC. This switch module will be used as an interface between the control circuitry and the conversion topology to solve the interface problems. It will provide a galvanic isolated power source for the gate drive circuitry with sufficient drive power for the MOSFETs or IGBTs.

1.4 Research outcomes

The research is expected to deliver a suitable switch module that can be used in any AC or DC converter circuit with no interface problems between it and the control.

A poster presentation was presented at the SATNAC 2010 conference in Cape Town.

An article will also be submitted to an accredited journal.

1.5 Research methodology

The research commenced with acquisition and study of literature related to the fundamentals of semiconductor switches and their switching speeds. This information, all obtainable from previous scholarly research work, formed a basis for an in-depth analysis of both theoretical and practical concepts on the design of a switch module. The key element in the process was the evaluation of different gate drive techniques, switching devices and level shifting circuits.

A universal bidirectional isolated switch module for power converters was then constructed. Experiments were performed to establish the electrical characteristics of the switch module. The switch was then evaluated in an AC control application as well as in DC applications. Compilation of the research documentation and the dissertation constituted the final phase of the research.

1.6 Delimitations

Design and development of a universal bidirectional galvanic isolated switch module for power converter applications focused only on MOSFETs and IGBTs and their gate drive circuits since both are voltage-controlled devices.

Gate drive for current controlled devices like BJTs is not dealt with in this regard because it is outside the scope of this research.

1.7 Value of the research

Researchers in the fuel cell laboratory at VUT will be able to use the proposed circuit module to implement control algorithms in experimental set-ups without having any interface problems between the control circuit and the conversion topology.

This will shorten the research time by enabling the researchers to focus on their own objectives and not on peripheral issues. This should lead to more research output in a shorter time.

1.8 Overview of the report

This research report consists of five chapters relating to the design and development of the switch module.

Chapter 1 entails an introduction, the background and study of power electronics, the need for the research, as well as the aims and values of the research. The methodology of the research is outlined and the delimitations are presented. It also states the importance of it for other researchers at the institution.

Chapter 2 starts with the introduction and discussion on the history of power electronics. This is followed by the discussion on power processing and the need for switching power electronics circuits. This chapter is devoted to the literature related

to the development of the universal bidirectional galvanic isolated power switch module for power converter applications. It also contains a brief review on power MOSFETs and their characteristics. The drive circuits and techniques currently employed to successfully drive the high-frequency high power MOSFETs are also discussed.

Level-shifting circuits are also addressed. The final complementary totem-pole gate drive circuit is also discussed. This chapter also discusses the control circuitry and the converter topologies that will validate the application of this module.

Chapter 3 deals with the actual design of the switch module and certain converter topologies. The design parameters of the switch and converter are dealt with mathematically and systematically. Computer simulation results are presented, confirming the theoretical predictions that the proposed system can work as predicted.

Chapter 4 is devoted to the explanation of the whole set-up of the experiment. All the experimental work, analysis and measurements performed on the switch module and components are presented. The interaction between the various components and the stages are explained.

In Chapter 5, conclusions and recommendations are drawn, suggestions for further improvements are also presented and hence recommendations are made regarding the design.

1.9 Summary

This chapter presented the underlying factors and reasons that necessitated the undertaking of the research as well as its importance and relevance. The background and research methodology used in the research has been provided as well as an overview of the dissertation.

The theoretical study of power electronics components, their characteristics, operation and application are discussed in the next chapter.

Chapter 2 Theoretical considerations

The previous chapter covered the background, the problem statement and the primary objectives of this study as well as the need for this research. The methodology of the research study, the delimitations and approach were presented as well as the value the research has for the institution as a whole.

This chapter is devoted to the literature related to the development of the universal bidirectional galvanic isolated power switch module for power converter applications. Relative properties of controllable switches were compared and contrasted. Drive circuits techniques and requirements were also discussed and compared. Lastly the components that make up the module were also discussed together with the converter topologies that validate it.

2.1 Introduction

The history of power electronics began with the introduction of the mercury-arc rectifier in 1900 (Rashid 2004:2). Then, the metal tank rectifier, grid-controlled vacuum-tube rectifier, ignitron, phanotron and thyratron were introduced gradually and were applied for power control until the 1950s (Moorthi 2005:1).

Rashid (2001:ix) further states that the first electronics revolution began in 1948 with the invention of the silicon transistor by Bardeen, Bratain and Schockley at Bell Telephone Laboratories. Most of today's advanced electronic technologies are traceable to that invention and modern micro-electronics evolved over the years from these silicon semiconductors (Rashid 2001:xi).

According to Moorthi (2005:1) the second electronics revolution began with the development of a commercial thyristor by the General Electric Company in 1958. That was the beginning of a new era of power electronics. Since then, many

different types of power semiconductor devices and conversion techniques have been introduced (Rashid 2001:xi).

The demand for energy, particularly in electrical form, is ever-increasing in order to improve the standard of living (Rashid 2001:xi). Power electronics helps with the efficient use of electricity, thereby reducing power consumption. Semiconductor devices used as switches for power conversion or processing are solid state electronic devices employed for the efficient control of the amount of power and energy flow. Higher efficiency and lower losses are sought for devices for a range of applications, from microwave ovens to high-voltage DC transmission. New devices and power electronic systems have evolved for even more effective control of power and energy (Rashid 2001:xi).

As Rashid (2001:xi) states: "power electronics has already found an important place in modern technology and has revolutionised control of power and energy. And as the voltage and current ratings and switching characteristics of power semiconductor devices keep improving, the range of applications continues to expand in areas such as lamp controls, power supplies to motion control, factory automation, transportation, energy storage, multi-megawatt industrial drives and electric power transmission and distribution."

Rashid (2004:2) further describes that the greater efficiency and higher control features of power electronics are becoming attractive for application in motion control by replacing the earlier electro-mechanical and electronic systems. Application in power transmission includes high voltage DC [HVDC] conversion stations, flexible AC transmission system [FACTS] and static-var control (Mohan *et al*. 2003:8). In power distribution these include DC-AC conversion, dynamic filters, frequency conversion and custom power systems (Moorthi 2005:2).

According to Moorthi (2005:2) it is important to note that all the devices employed for power electronic applications are used in the 'switch' mode. The moments of switching ON or OFF are controlled to fulfill the requirements of the circuit under

consideration. In broad terms, the task of power electronics is to process and control the flow of electric energy by supplying voltages and currents in a form that are optimally suited for user loads (Mohan *et al*. 2003:8-9).

2.2 Power processing

Considering the nature of flow of the electric energy which will suit the load, Mohan *et al*. (2003:3) suggested a model shown in Figure 1 that describes the process and control of electric energy. This model shows a power electronic system in a block diagram form.

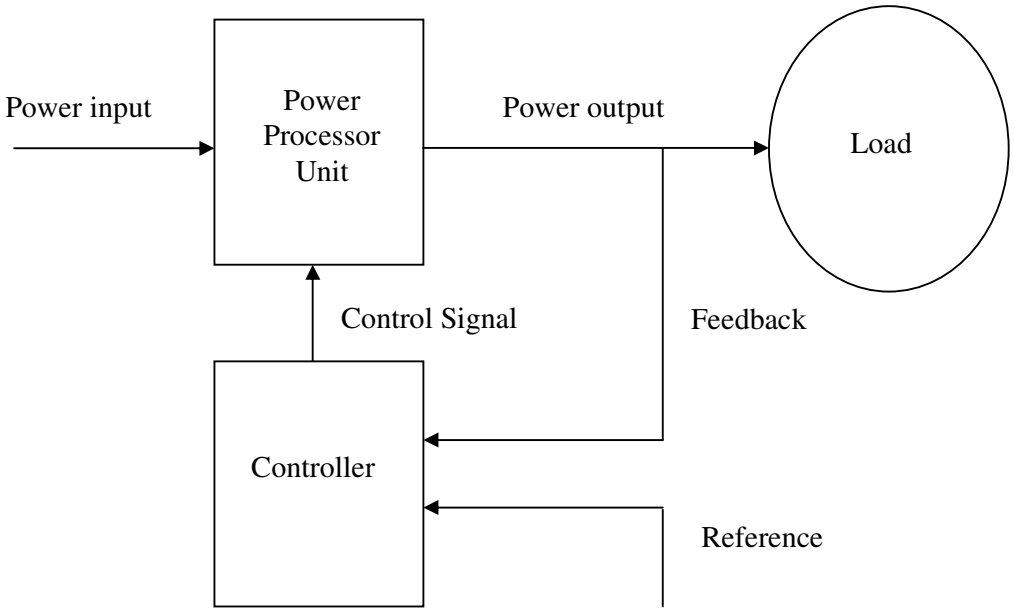

Figure 1: Block diagram of a power electronic system (Mohan *et al.* 2003:3)

According to Erickson & Maksimovic (2001:1) the power input is usually (but not always) from the electric utility at a certain frequency, being single or three-phase. The phase angle between the input voltage and the current depends on the topology and the control of the power processor. The processed output (voltage, current, frequency and the number of phases) is as desired by the load (Mohan *et al*. 2003:3).

If the power processor's output can be regarded as a voltage source, the output current and the phase angle relationship between the output voltage and the current depend on the load characteristic (Mohan *et al*. 2003:3). The feedback controller compares the output of the power processor unit with a desired (or a reference) value and adjust to the required value and by so doing the error between the two is minimized by the controller (Prodic, Maksimovic & Erickson 2001:893). The power flow through such systems may be reversible, thus interchanging the roles of the input and the output (Mohan *et al*. 2003:3).

The controller in the block diagram of Figure 1 consists of linear integrated circuits or digital signal processors (DSP) (Mohan *et al*. 2003:3). Revolutionary advances in microelectronics have led to the development of such controllers. Moreover, these advances in semiconductor fabrication technology have made it possible to significantly improve the voltage and current handling capabilities and the switching speeds of power semiconductor devices, which make up the power processor unit (Rashid 2004:26).

2.2.1 Interdisciplinary nature of power electronics

Mohan *et al*. (2003:14) also came up with a diagram showing the interdisciplinary nature of power electronics which encompasses many fields within electrical engineering as shown in Figure 2. These include power systems, solid-state electronics, electrical machines, analogue and digital control, signal processing, electromagnetic field calculations and so on (Rashid 2001:2).

Combining the knowledge and study of these diverse fields makes the study of power electronics more challenging as well as more interesting (Rashid 2001:2). There are many potential advances in all these fields that can improve the prospects for applying power electronics to new applications (Mohan *et al*. 2003:14). Any useful circuit design for the control of power must address issues of both devices and control as well as of the energy itself. Among the unique aspects of power electronics are its emphasis on large semiconductor devices, the application of

magnetic devices for energy storage and special control methods that must be applied to nonlinear systems (Rashid 2001:2).

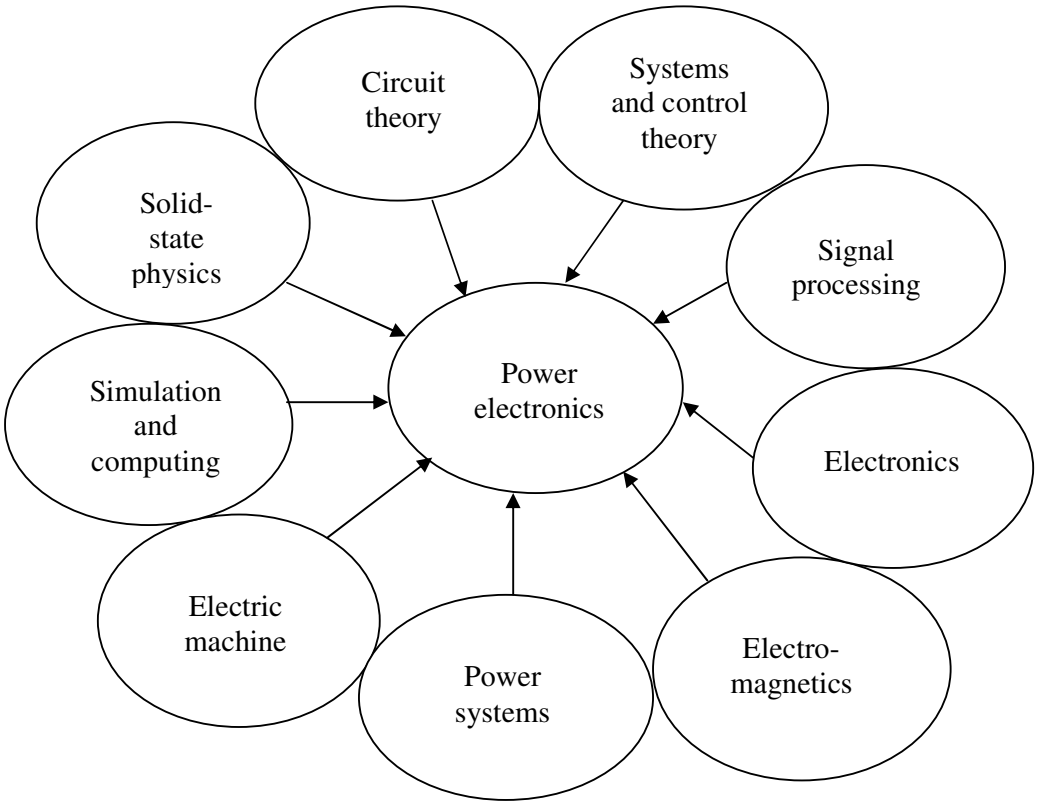

Figure 2: Interdisciplinary nature of power electronics (Mohan *et al*. 2003:14)

2.2.2 The need for switching in power electronic circuits

The need to use semiconductor devices to perform conversion functions is very much related to converter efficiency. In power electronic circuits, the semiconductor devices are generally used as switches, that is, either in the ON-state or the OFF-state (Rashid 2001:76).

This is unlike the case for power amplifiers and linear regulators where semiconductor devices operate in their linear mode and as a result a very large amount of energy is lost within the power circuit before the processed energy reaches

the output (Rashid 2001:76). Semiconductor switching devices are used in power electronic circuits because of their ability to control and manipulate very large amounts of power from the input to the output with relatively very low power dissipation in the switching devices. Their use helps to create highly efficient power electronic systems (Rashid 2001:76).

As efficiency is considered an important figure of merit, it does have a significant implication for overall system performance. In low efficiency power systems, large amounts of power are dissipated in the form of heat, which results in one or more of the following (Mohan *et al*. 2003:4):

- Cost of energy increase due to increased consumption,
- Additional design complications might be imposed, especially regarding the design of device heat sinks,
- Additional components such as heat sinks increase the cost, size and weight of the system resulting in a low-power density,
- High-power dissipation, forces the switch to operate at a low switching frequency resulting in a limited band-width, slow response and most importantly, the size and weight of components are large and
- Reduced system reliability.

According to Rashid (2001:76) switching by mechanical or electrical means, is the best possible way to achieve high efficiency. However, unlike mechanical switches, electronic switches are more superior by far because of their speed and power-handling capabilities as well as reliability. The advantages of using switches do not come without a cost. Because of the nature of switch currents and voltages (square waveforms), high order harmonics are normally generated in the system. To reduce these harmonics, additional input and output filters are normally added to the system (Baliga 2008:822). According to Rashid (2001:77) if the switch is assumed to be ideal and is periodically turned ON and OFF, then a typical output voltage V_o waveform can be seen as in Figure 3 and its average value given by:

$$V_o = \frac{1}{T}\int_0^T V_{in}\,dt = V_{in}D \qquad \text{(Volts)} \qquad (1)$$

Where:

$D \equiv$ duty cycle

$T \equiv$ period of the waveform in s

$V_{in} \equiv$ input voltage in V.

Moreover, depending on the device type and power electronic circuit topology used, the device driver circuit and the circuit protection (snubbers) can significantly increase both the complexity of the system and its cost (Erickson & Maksimovic 2001:14).

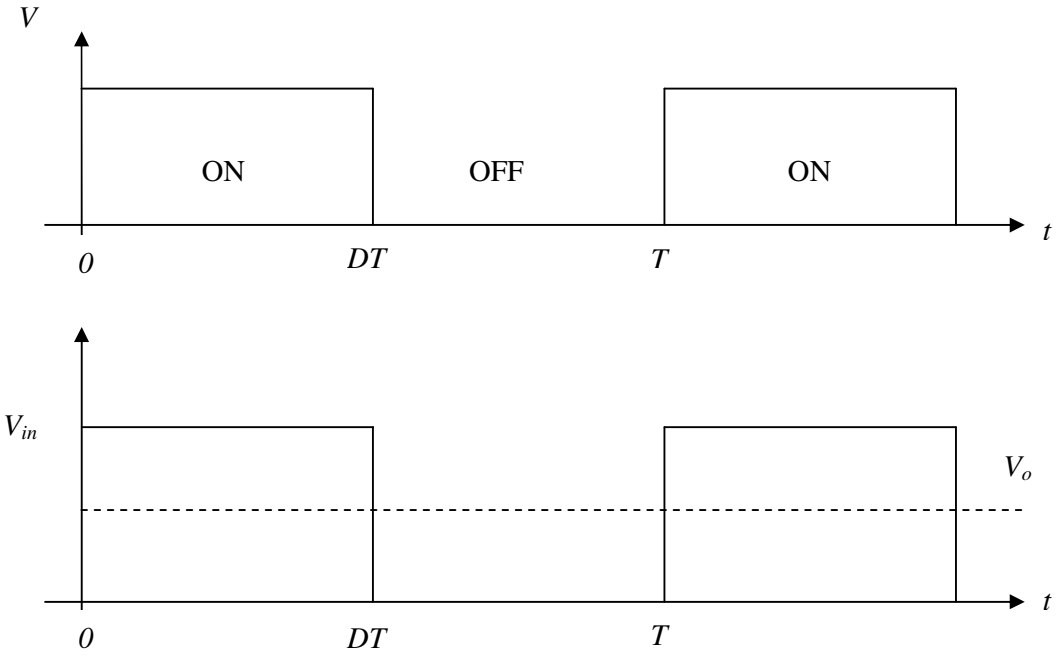

Figure 3: Switching and output waveforms (Rashid 2001:77)

2.3 Comparison of controllable switches

Mohan *et al*. (2003:29) points out that only a few definite statements can be made in comparing these devices because a number of properties must be considered

simultaneously and the devices are still evolving at a rapid pace. However, the qualitative observations given in Table 1 can be made. From this table, although the MOSFET has a low power capability when it comes to switching speed it is the fastest (Mohan *et al*. 2003:29). Again, a summary of power devices capabilities is shown in Figure 4 (Rashid 2001:64).

Table 1: Relative properties of controllable switches (Mohan *et al*. 2003:29)

Device	*Power Capability*	*Switching Speed*
BJT	Medium	Medium
MOSFET	Low	Fast
GTO	High	Slow
IGBT	Medium	Medium
MCT	Medium	Medium

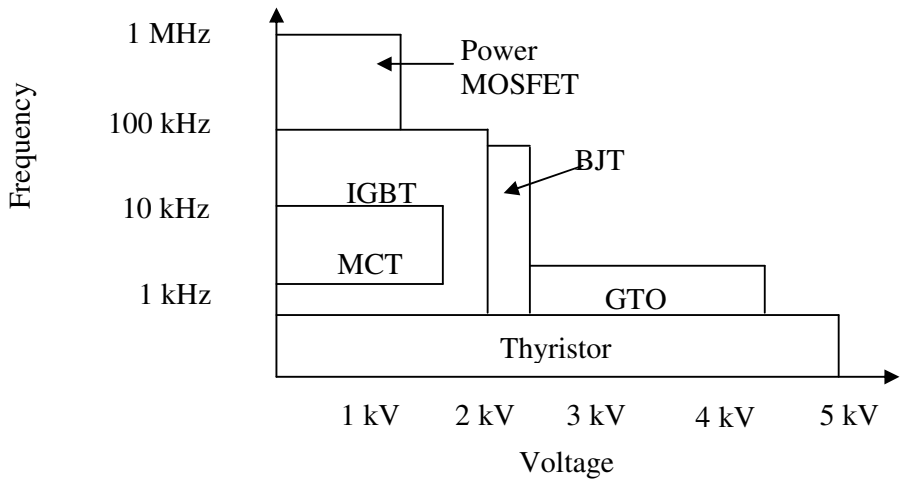

Figure 4: Device operating regions: Voltage vs Frequency (Rashid 2001:64)

This figure indicates that a categorization based on voltage and switching frequency provides two key parameters for determining whether a BJT, a MOSFET or an IGBT is the better device in an application (Rashid 2001:64). In addition to improvements in these devices, the progress in semiconductor technology will undoubtedly lead to

higher power ratings (Rashid 2001:64). Figure 5 is the categorization based on current and switching frequency for determining the device application. However, there are still difficulties in selecting a component for use in the crossover region, which includes voltages of 250 V to 1000 V and frequencies of 20 kHz to 100 kHz. At voltages < 1000 V, the BJT has been entirely replaced by the MOSFET and at higher voltages new designs use IGBTs (Rashid 2001:64).

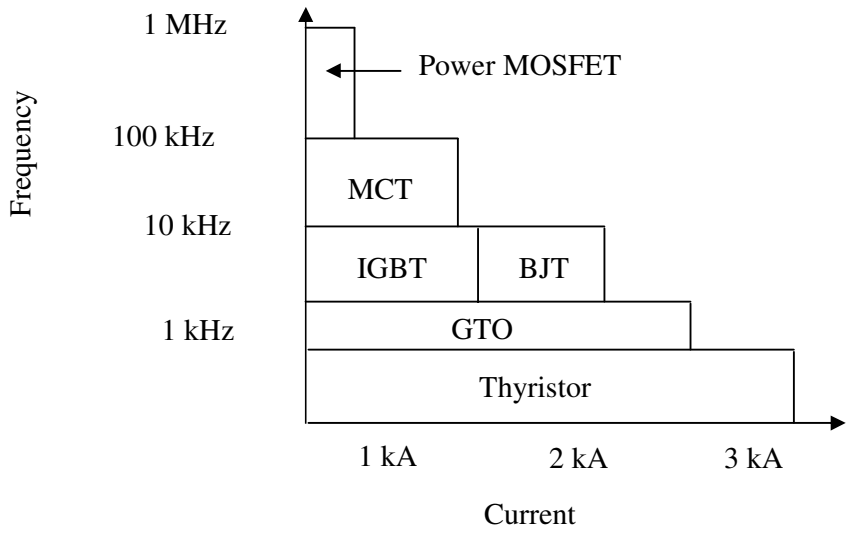

Figure 5: Device operating regions: Current vs Frequency (Rashid 2001:64)

On the other hand, the forced-commutated thyristor, which was once widely used in circuits for controllable switch applications, is no longer being used in new converter designs with the possible exception of power converters in multi-MVA ratings. This is just a pertinent example of how the advances in semiconductor power devices have modified converter design (Mohan *et al*. 2003:29).

2.4 Power Modules

The demand to control the electric power in electric motor drive systems and industrial controls existed for many years. This led to the early development of the Ward-Leonard system to obtain a variable DC voltage for the control of DC motor

drives. Power electronics have revolutionized the concept of power control for power conversion and for control of electrical motor drives (Rashid 2004:1).

According to Rashid (2004:26) power devices are available as a single unit or in a module. A power converter often requires two, four or six devices, depending on its topology. Power modules with dual (half-bridge configuration) or quad (full-bridge) or six (for three-phase) devices are available for almost all types of power devices (Galvez, Jorda, Vellvehi, Millan, Jose-Prieto & Martin 2007:1).

Mohan *et al*. (2003:656) classifies this as an intelligent module or also known as smart power. According to Gadi (1995:33) these modules are being used in power electronics technology and can be viewed as a box that interfaces a power source to any load as shown in Figure 6.

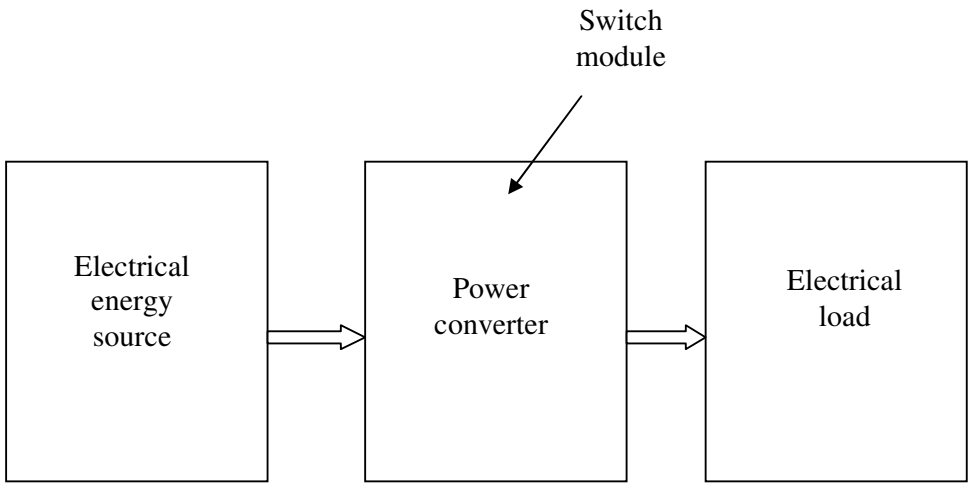

Figure 6: Generalized power converter system (Gadi 1995:33)

The modules offer the advantages of lower ON-state losses, high voltage and current switching characteristics and higher speeds than that of conventional or discrete devices. Some modules even include transient protection and gate drive circuitry (Rashid 2004:26).

2.4.1 Structure of the bidirectional switch power module

The universal bidirectional galvanic isolated switch module basically consists of power switches in a bidirectional switch function (bidirectional in current and voltage) and these power devices are connected in common emitter configuration (Galvez *et al*. 2007:3). It includes the power transistors gate drivers in a totem-pole configuration for driving MOSFETs, galvanic isolation between control and power stages, over-voltage protection devices and floating voltage power supply (Wheeler, Clare, Empringham, Bland & Apap 2002:384).

Gate drive circuits are commercially available to drive individual devices or modules (Rashid 2004:26). Intelligent modules can be classified as state-of-the-art power electronics, which integrate the power module and the peripheral circuit as shown in Figure 7 (Galvez *et al*. 2007:3). The user needs only to connect external power supplies (Kularatna 2008:129-132).

According to Rashid (2004:27) analogue circuits are used for creating the sensors necessary for self-protection and for providing a rapid feedback loop, which can terminate chip operation harmlessly when the system conditions exceed the normal operation conditions. For example, smart power or power module chips must be designed to shutdown without damage when a short circuit occurs across a load such as a motor winding (Romero, Fusaro & Martinez 1995:918).

Baliga (1996:35) states that in smart power technology, the load current is monitored and whenever this current exceeds a preset limit, the drive voltage to the power switches is shut OFF. In addition to this, features such as over-current protection, overvoltage and over-temperature protection are commonly included to prevent destructive failures (Rashid 2004:27). Power modules allow the control of output voltages and also allow obtaining better quality of the output current waveforms because the required commutation times between the power switches can be minimized (Rashid 2004:27). These classical circuits do not show natural free-wheeling paths for the inductive load currents.

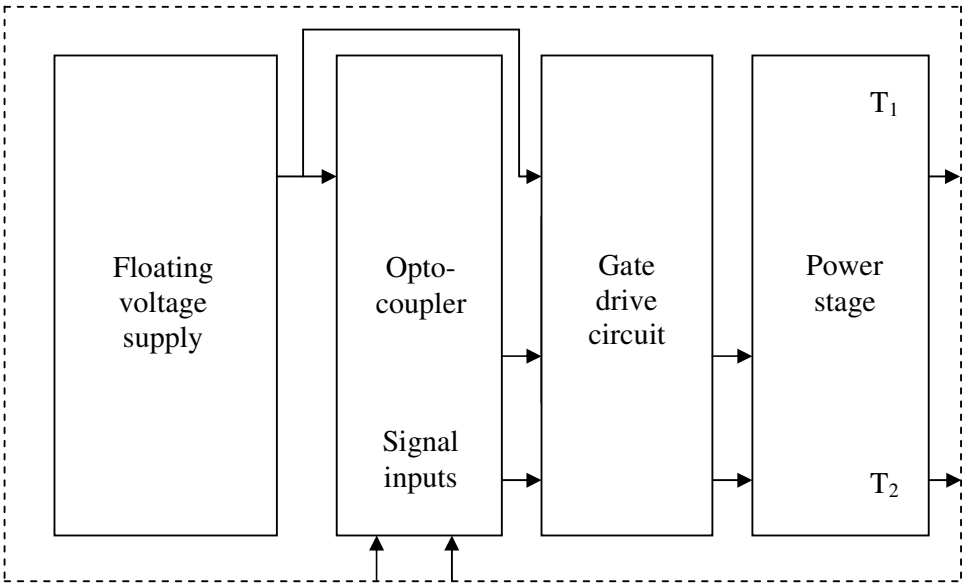

Figure 7: Power switch module shown in block diagram (Galvez *et al.* 2007:3)

Thus, current commutation strategy between power switches is of main importance in order to ensure correct performances and high reliability (Mulvey, Salim & Carr 1998:57). These algorithms determine the right switching sequence of the different transistors and their delay times. And these delays are mainly related to the characteristic switching times of the power devices (Galvez *et al*. 2007:1).

2.4.2 Operation of the switch module

The control circuitry determines the turn-ON and turn-OFF instants of the bidirectional switches using relatively complex modulation algorithms to fix the current and voltage target values in the load. The processed high-level logic control signals are galvanically isolated using opto-couplers before application to the power transistors' gate-drivers. The floating voltage supply of these drivers is supplied by an integrated DC-DC converter. The gate control signals are finally sent to the power devices and other protection devices such as over-voltage transient suppressors and gate resistors (Galvez *et al*. 2007:1).

2.4.3 Bidirectional switches

According to Casadei, Serra, Tani & Zarri (2005:83) several studies were conducted to come up with the necessary bidirectional switches for the power modules. The bidirectional switches were initially obtained by combining discrete components. Then, as the interest towards modules increased, some manufacturers produced power modules specifically designed for the application (Casadei Serra, Tani & Zarri 2002(a):371). The switches are usually traditional silicon IGBTs, but may also have device types such as MCTs and MOSFETs with SiC diodes (Wheeler, Clare & Empringham 1998(b):708).

Casadei *et al.* (2002(b):1110) also point out that power modules require bidirectional switches with the capability to block the voltage and to conduct current in both directions. There are two main topologies for bidirectional switches, namely the common-emitter anti-parallel configuration and the common-collector anti-parallel configuration (Casadei *et al.* 2005:86). The common-emitter configuration is represented in Figure 8 . As shown, two IGBTs are connected with two diodes in an anti-parallel configuration. The diodes provide the reverse blocking capability.

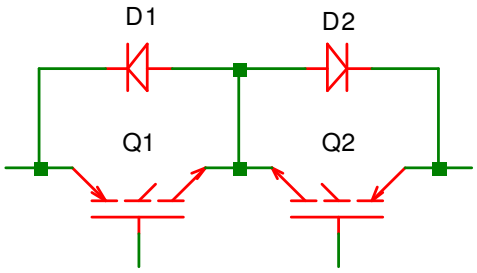

Figure 8: Bidirectional switches in common-emitter configuration (Casadei *et al.* 2005:1-86)

The main advantage of this solution is that the two IGBTs can be driven with respect to the same point, i.e. the same common emitter, that can be considered as a local

ground for the bidirectional switch (Wheeler, Clare & Empringham 1998(a):627). The common-collector arrangement is presented in Figure 9, where two IGBTs are now arranged in a common-collector configuration and their collector terminals are at common point which can be considered as the ground point (Casadei *et* al. 2005:86).

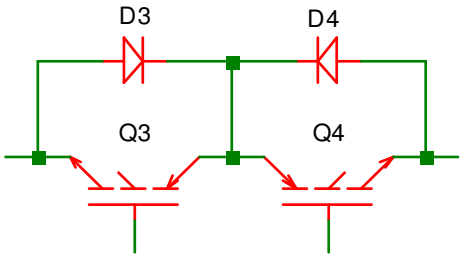

Figure 9: Bidirectional switches in common-collector configuration (Casadei *et al*. 2005:1-86)

Wheeler and Grant (1997:54) point out that the two diodes used with IGBTs in common emitter configuration provide the reverse-voltage blocking capability; whereas MOSFETs have the internal body diodes that provide the reverse-voltage blocking capability. This facility can then be used to reduce the switching losses during commutation of the load current (Casadei *et al.* 2002(a):371).

2.5 Power semiconductor devices

Rashid (2004:9) categorizes power transistors as four types; the BJT, IGBTs, SITs and power MOSFETs. One of the main important performance features of any semiconductor switching device is its switching characteristics. Understanding the device switching characteristics greatly improves its utilisation in the various applications. Power semiconductor devices have three operating states commonly known as the cut-OFF mode, the active mode and the saturation mode (Mohan *et al.* 2003:20). Where power electronic converters utilise switch-mode operation devices

are operated in either the cut-OFF region or the saturation region, whilst making the transition through the active or linear region as short as possible in order to facilitate maximum power conversion efficiency (Khan 2007:544).

According to Rashid (2001:83) in order to achieve these fast transition times, a suitable gate-driver circuit is required. This gate-driver has to be able to supply the necessary charge to the power semiconductor device gate junction in order to achieve turn-ON and turn-OFF as fast as possible. Power semiconductors can be classified into two categories with respect to drive requirements, namely:

- current-driven devices and
- voltage-driven devices.

Only voltage-driven devices will be looked at in this regard owing to BJTs being replaced by MOSFETs and IGBTs which are both voltage-driven devices.

2.5.1 Voltage-controlled devices

These devices are semiconductors which require a constant voltage drive on the gate control terminal in order to remain in conduction. The input drive requirements of these devices are substantially lower than their current-driven counter parts and are the preferred choice in modern power electronics. Two such devices are the MOSFET and the IGBT which are forced commutated switching devices being fully controlled at the gate terminal under normal operating conditions (Khan 2007:544).

The gate input junction of the MOSFET and IGBT is purely capacitive, so no gate drive current is needed in the steady state, unlike other transistors. A minimum gate drive voltage however must be maintained (above the gate threshold voltage) at the device gate in order for it to remain in conduction (Khan 2007:544). For the MOSFET to carry drain current, a channel between the drain and the source must be created. This can only occur when the continuous application of a gate-to-source voltage exceeds the device threshold voltage V_{Th} (Whittington, Flynn & Macpherson 1997:120). The device can then be either in the triode region, which is also called

'constant resistance region', or in the saturation region depending on the value of V_{DS} (Rashid 2001: 83). A high current low impedance drive circuit is needed to inject or remove current, from the gate with high slew rates in order to switch the device rapidly. The gate drain capacitance, although small, can also require significant charge at high drain voltage slew rates (Khan 2007:544).

2.6 Theoretical overview of MOSFETs

Because of their high efficiency, power MOSFETs and IGBTs are considered ideal as semiconductor switches and are ranked as one of the most significant developments in power electronics (Swart 2004(a):40). According to Rashid (2001:80) the ability of high power MOSFETs to act as switches make them the ideal switching devices and they are one of the fastest power switching devices with voltage power ratings up to 1500 V and current rating as high as 100 A.

This statement is largely attributed to the numerous advantages that the MOSFET holds over other semiconductor devices. Some noteworthy advantages are (Swart 2004(a):40):

- High switching speeds and
- Their ability to maintain gain up to much higher frequencies.

In the ON-state the voltage across the switch should ideally be zero, independent of the current. In the OFF-state the opposite must hold true with zero current flowing independent of the voltage (Swart 2004(a):40). Modern power MOSFETs also have an internal body diode connected between the source and the drain as shown in Figure 10, which provides a reverse direction for the drain current allowing a bidirectional switch implementation (Rashid 2001:82). Even though they do have adequate current and switching speed ratings, in some applications that require the use of ultra-fast diodes, an external fast recovery diode is added in anti-parallel fashion after blocking the body diode by a slow recovery as shown in Figure 11 (Rashid 2001:82).

According to (Agrawal 2001:116) another important parameter that affects the MOSFET switching behavior is the parasitic capacitances between the device's three terminals, namely, gate-to-source (C_{GS}), gate-to-drain (C_{GD}) and drain-to-source (C_{DS}) capacitances.

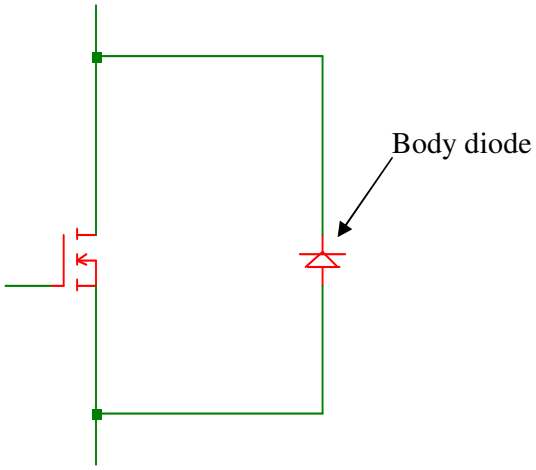

Figure 10: MOSFET internal body diode (Rashid 2001:82)

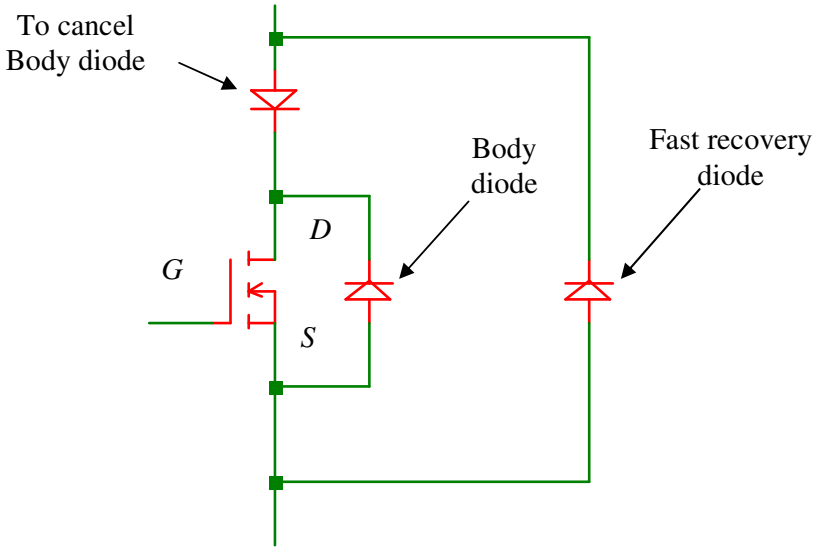

Figure 11: Implementation of a fast recovery body diode (Rashid 2001:82)

Normally, manufacturer's data sheets do not specify these device capacitances rather they quote input, output and reverse common source capacitances (C_{ISS}, C_{OSS}, and C_{RSS} respectively) as shown in Figure 12.

All these capacitances are related according to the following:

$$C_{GD} = C_{RSS} \tag{2}$$
$$C_{GS} = C_{ISS} - C_{RSS}$$
$$C_{DS} = C_{OSS} - C_{RSS}$$

Where:

C_{RSS} ≡ small-signal reverse transfer capacitance in pF

C_{ISS} ≡ small-signal input capacitance with the drain and source terminals shorted in pF

C_{OSS} ≡ small-signal output capacitance with the gate and source terminals shorted in pF (Rashid 2001:83).

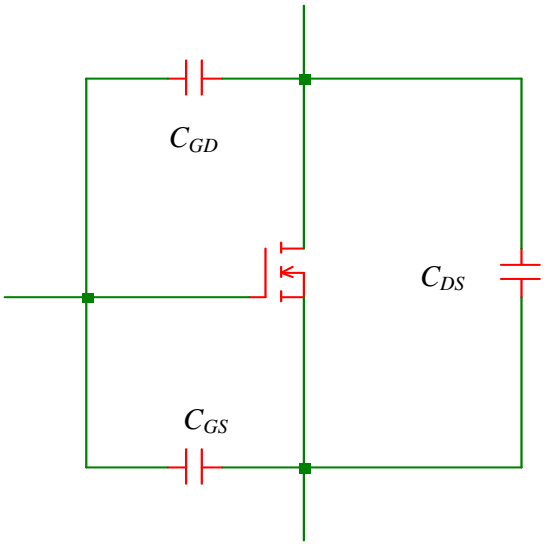

Figure 12: Equivalent MOSFET representation including junction capacitances (Rashid 2001:83)

2.6.1 Safe Operation Area

According to Mohan *et al.* (2003:591) MOSFETs have a safe operation area (SOA) that provides the current and voltage limits which the device is able to handle without destructive failure. A typical SOA graph for a MOSFET device is shown in Figure 13. As the drain-source voltage starts increasing, the device starts leaving the ON-state and enters the saturation region. During the transition time the device exhibits a large voltage and current simultaneously. The maximum current limit while the device is ON is determined by the maximum power dissipation (P_{dis}) equation (3) (Kazimierczuk 2008:685).

$$P_{dis} = I^2_D \times R_{DS(ON)} \quad \text{W} \tag{3}$$

Where:

$R_{(DS)ON}$ ≡ ON-resistance of the MOSFET in Ω

I_D ≡ forward current in A

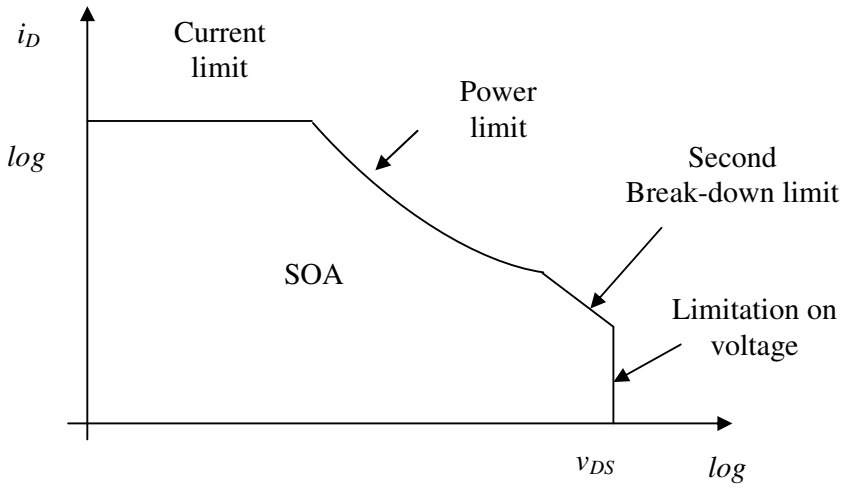

Figure 13: A typical graph for safe operation areas (SOA) (Mohan *et al.* 2003:591)

Mohan *et al* (2003:591) further states that at higher drain-source voltage values that approach the avalanche breakdown, it is observed that a power MOSFET suffers from a second breakdown phenomenon. The second breakdown occurs when the MOSFET is in the blocking state (OFF) and further increase in V_{DS} will cause a sudden drop in the blocking voltage (Whittington *et al*. 1997:125). According to Rashid (2001:91) the source of this phenomenon in a MOSFET is caused by the presence of a parasitic n-type bipolar transistor. Furthermore commercial MOSFETs and IGBTs have excellent high operating temperatures and the effect of temperature is more prominent on the ON-state resistance as shown in Figure 14 (Rashid 2001:91).

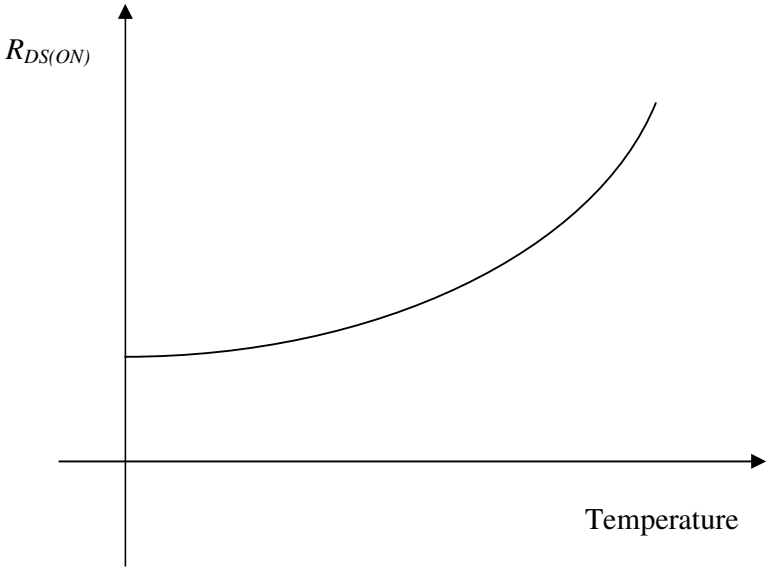

Figure 14: On-state resistance against temperature (Rashid 2001: 92)

As the ON-state resistance increases, the conduction losses also increase. This large V_{DS} limits the use of MOSFETs in high-voltage applications. Maximum drain current, the breakdown voltage and the internal junction temperature governed by the power dissipation in the device are the factors that determine the safe operating area of the devices (Mohan *et al* 2003:591). The use of silicon carbide instead of silicon has reduced the effect of this drain-to-source voltage (V_{DS}) many fold (Culurciello, Pouliquen, Andreou, Strohbehn & Jaskulek 2005:138).

2.6.2 Gate voltage limitations

The silicon oxide layer between the gate and the source regions can be punctured by exceeding its dielectric strength (Whittington *et al*. 1997:125). From the data sheet the gate-to-source voltage is between 10 V and 30 V for most devices (Philips Semiconductor Devices 2004:7). Care should be exercised not to exceed the gate-to-source maximum voltage rating. Even if the applied gate voltage is kept below the maximum rated gate voltage, the stray inductance of the gate connection coupled with the gate capacitance may generate ringing voltages that could lead to the destruction of the oxide layer. Over-voltages can also be coupled through the drain-gate self-capacitance owing to transients in the drain circuit. A gate drive circuit with very low impedance insures that the gate voltage is not exceeded in normal operation (Whittington *et al*. 1997:125).

The speed limitations of MOS circuits are due entirely to stray circuit capacitance and the inability of the MOSFET to charge and discharge this capacitance (Swart 2004(a):40). According to Balogh (2001:4) the practical switching times of MOSFETs are at least two to three orders of magnitude longer than the theoretical switching time. Therefore in high-speed applications, the most important parameters are the parasitic capacitances of the MOSFET device.

Zener diodes are frequently used to protect the gate from transients. Unfortunately they also contribute to oscillations and have been known to cause device failures. A transient can get to the gate from the drive side or from the drain side. In either case, it would be an indication of a more fundamental problem of a high impedance drive circuit. If this is necessary, it is advisable to insert a small series resistor between the zener diode and the gate to prevent these oscillations (Vishay Siliconix Semiconductor Devices 2010).

The intrinsic cut-off frequencies of MOS devices themselves are in the order of 1GHz. It is therefore valid to say MOSFETs are not really inherently bound to frequency limitations within the high-frequency range. This is because of the

absence of minority carrier transport (Baliga 1996:125) as quoted by (Swart 2004(a):43). Limits to high-frequency operation are set by:

- The transient time across the drift region and
- The rate of charging of the input gate capacitance.

The transit-time limited frequency response (f_t) is a function of the breakdown voltage (Baliga 2008:281):

$$f_t = \frac{\left(6.11\times10^{11}\right)}{\left(1+\frac{L}{d}\right)\times\left(BV_{PP}\right)^{7/6}} \quad \text{Hz} \tag{4}$$

Where:

L ≡ MOSFET channel length in μm

d ≡ MOSFET drift region thickness in μm

BV_{PP} ≡ MOSFET breakdown voltage in V

Taylor (1993:3) examined the gate control of a MOSFET when it is switched ON and found out that the gate control charge (Q_{gate}) may be expressed as

$$Q_{gate} = C_{ISS}\times V_{GS} \quad \text{C} \tag{5}$$

Where:

C_{ISS} ≡ input gate capacitance of the MOSFET in pF

V_{GS} ≡ gate-to-source voltage in V

C_{ISS} is the sum of the real capacitance between the gate and the source C_{GS} and the voltage dependant capacitance between the drain and the gate C_{DG}. The value of V_{GS} is a function of the device and the voltage required to achieve full enhancement. The energy expended in accumulating this gate charge (E_{gate}) can be expressed as (Taylor 1993:3):

$$E_{gate} = 0.5 \times C_{ISS} \times V_{GS}^{\,2} \quad \text{J} \tag{6}$$

According to Swart, Pienaar & Case (2004(b):544) the overall drive efficiency of the MOSFET is determined by the power consumed in the gate (P_{gate}). This power in the gate will only be dissipated within the gate structure if the gate structure's resistance happens to be significantly higher than the drive circuit impedance. According to Whittington *et al*. (1997:125) the amount of power that will be dissipated in the gate of an IRF530N MOSFET when the gate to source voltage is 12 V and the frequency of operation is 100 kHz is given by:

$$P_{gate} = 0.5 \times C_{ISS} \times V_{GS}^{\,2} \times f \quad \text{W} \tag{7}$$

Where:

f ≡ input gate frequency in Hz

V_{GS} ≡ gate-to-source voltage in V

From Taylor's (1993:3) findings it can be seen that driving high power MOSFETs at low frequencies requires only a small amount of power and thus a small amount of gate current. The gate charge may also be expressed with regard to current and time (Swart *et al*. 2004(b):544), as in equation (8)

$$Q_{gate} = I \times t \quad \text{C} \tag{8}$$

Where:

I ≡ input gate current in A

t ≡ time period to charge the gate in s

2.7 Ground referenced gate drive with PWM direct drive

According to Balogh (2001:11) the simplest way of driving the gate of the main

switching transistor in power supply applications, is to utilise the gate drive output of the PWM controller as shown in Figure 15.

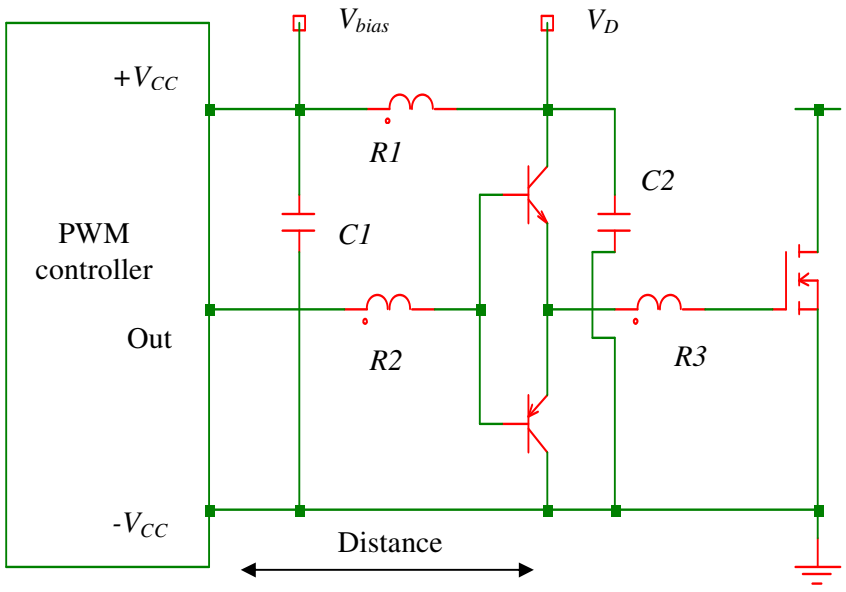

Figure 15: Bipolar totem-pole MOSFET driver (Balogh 2001:11)

As Balogh (2001:11) indicated the most difficult task is to optimise the circuit layout. Even with the ground plane, the inductance cannot be completely eliminated since the ground plane provides a low inductance path for the ground return current only. To reduce the inductance linked to the gate drive connection, a wider PCB trace is desirable (Jacobs 2002:96).

2.8 Gate drive requirements

The gating circuit is an integral part of a power converter that consists of power semiconductor devices (Rashid 2001:761). The output of a converter that depends on how the gating circuit drives the switching devices is a direct function of the switching. Therefore, the characteristics of the gating circuit are key elements in achieving the desired output and the control requirements of any power converter.

The design of a gating circuit requires knowledge of the gate characteristics and needs of devices such as gate-turn-off thyristors (GTOs), bipolar junction transistors (BJTs), metal oxide semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) (Rashid 2001:407).

According to Khan (2007:545) the gate drive requirements for power MOSFETs or IGBTs utilised as a switch are:

- The gate voltage must be 10 V to 15 V higher than the source voltage. Such a gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.
- The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the power device, which in most applications swings between the two rails.
- The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

Schoeman, Van Wyk, Blajszcak, & Case (1994:1303) also point out that the gate drive must also be capable of supplying a continuous (DC) output of either polarity for PWM applications.

2.8.1 The impedance of the gate circuit

The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. Once again, the lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance and the faster will be the rise time of the drain voltage (Maurice & Wuidart 1994:1). According to Kularatna (2008:131) low gate drive impedance is important to achieve high switching performance. Even when switching performance is of no great concern, it is important to minimise the impedance in the gate-drive circuit to clamp unwanted voltage transients on the gate.

Kularatna (2008:131) also states that the essential idea of a gate-drive circuit is to achieve two important design requirements:

- To provide correct voltage levels required by the MOSFET or IGBT gate and
- To provide fast charge or discharge of the gate capacitances for MOSFETs or IGBTs.

According to Balogh (2001:14) the primary function of a drive circuit is to switch a power semiconductor device from the-OFF state to the ON-state and vice versa. The designer seeks a low cost drive circuit that minimises the turn-ON and turn-OFF times so that the power device spends little time in traversing the active region where the instantaneous power dissipation is large. In the ON-state, the drive circuit must provide adequate drive power (e.g., base current to a BJT or gate-source voltage to a MOSFET) to keep the power switch in the ON-state where the conduction losses are low (Mohan *et al*. 2003:697). MOSFETs respond instantaneously to changes in gate voltage and will begin to conduct when the threshold is exceeded (Whittington *et al.* 1997:125). This drive current determines both the rise and fall times for the drain current. The drive current can be estimated as follows:

$$I_m = C_{DG}\frac{dV}{dt} \tag{9}$$

$$I_G = C_{GS}\frac{dv}{dt} \tag{10}$$

Where:

$I_m \equiv$ current required by the Miller effect to charge the drain-to-gate capacitance at the rate it is desired to move the drain voltage and

$I_G \equiv$ current required charging the gate-to-source capacitances through the linear region

As Swart (2004(a):44) stated there is a variation of the gate voltage V_{GS} with gate charge time when considering the drain-source voltage and this is shown in Figure

16. The gate waveforms show a step at a point just above the threshold voltage which varies in duration depending on the amount of drive current available (Whittington *et al*. 1997:125).

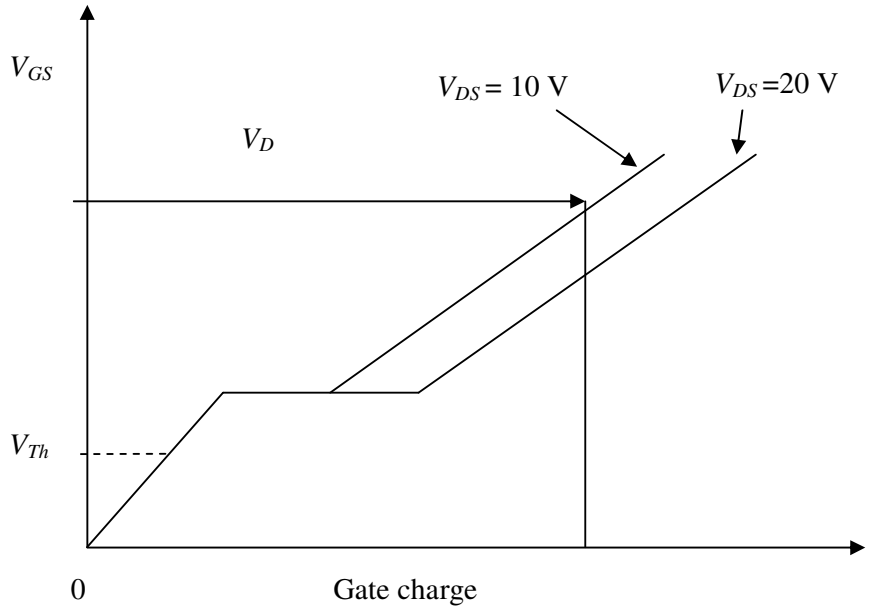

Figure 16: Typical gate charge to gate-to-source voltage (Swart 2004(a):44)

The value of capacitances may be found from the manufacturers' datasheet. Rashid (2001:422) describes that, for the first two periods, C_{ISS} and C_{RSS} values may be assumed to be dependent on

$$V_{DS} = \frac{1}{2}V_{DD} \tag{11}$$

For the third period, C_{ISS} is dependent on:

$$V_{DS} = V_{DD(ON)} \tag{12}$$

Since the source resistance (R_g) is in series with C_{GS} and C_G, the turn-ON time and the

turn-OFF time are affected by this resistance. Therefore, both periods can be controlled independently. Similarly, a bipolar gate drive signal allows rapid turn-ON and turn-OFF (Rashid 2001:422).

2.8.2 Design consideration of gate resistor

A small valued gate resistor of considerable power rating (5 to 20 W range) is used in high-speed switching circuits (Rashid 2001:426). This resistor will damp out oscillations caused by inductance of the device assembly connecting the driver circuit or chip on printed circuit board to the gate of MOSFET. It behaves as an under-damped series *RLC* circuit. If there is no gate resistance in the gate driving circuit, then under-damped oscillations will cause a gate voltage (V_{GS}) twice the size of V_D which is the gate drive supply voltage. When the driver chip or circuit operates at about 12 V, then V_{GS} would be 24 V. This could be destructive as the maximum V_{GS} is normally 20 V (Rashid 2001:426).

The damping ratio is given by:

$$\zeta = \frac{R}{2\sqrt{\frac{L_p}{C_g}}} \tag{13}$$

Where:

$L_p \equiv$ gate inductance in nH

$C_g \equiv$ gate capacitance in nF

$R \equiv$ gate resistance in Ω

For a total gate input capacitance of 1 nF and a gate inductance of 40 nH, the fastest response of the circuit without over-shoot will be for critical damping ($\zeta = 1$). Then the gate resistor can be calculated as

$$R = 2\zeta\sqrt{\frac{L_p}{C_g}}$$

$$R = (2)\times(1)\sqrt{\frac{40\times10^{-9}}{1\times\ 10^{-9}}}$$

$$R = 12.6\ \Omega$$

Taking (ζ= 0.6)

$$R = (2)\times(0.6)\sqrt{\frac{40\times10^{-9}}{1\times\ 10^{-9}}}$$

$$R = 7.56\ \Omega \qquad (14)$$

A higher-value gate resistor may effectively damp out the oscillations, but simultaneously it slows down the switching speed of the MOSFET. Because most of the driver chips operate from a 12 V source, they supply or demand about 1 A or more during the switching transitions. Therefore, a 10 Ω resistor is a suitable upper value for the gate resistance to damp out oscillations (Rashid 2001:426).

2.8.3 Bipolar totem-pole drive circuit

According to Balogh (2001:12) one of the most popular and cost effective drive circuits for driving MOSFETs is a bipolar, non-inverting totem-pole driver shown in Figure 17. This circuit handles the current spikes and power losses making the operating conditions for the PWM controller more favorable. If the circuit is placed right next to the power MOSFET, the high current transients of driving the gate are localized in a very small loop area, reducing the value of parasitic inductances (Balogh 2001:12).

According to Khan (2007:546) even though the driver is built from discrete components, it needs its own bypass capacitor *C1* placed across the collectors of the upper npn and the lower pnp transitors as shown in Figure 17. Another interesting property of the bipolar totem-pole driver is that the two base-emitter junctions protect each other against reverse breakdown.

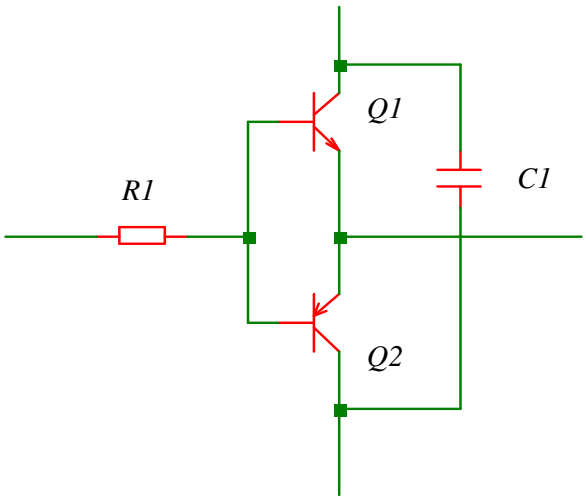

Figure 17: A bipolar totem-pole drive circuit (Balogh 2001:12)

2.9 Gate drive techniques and ICs

According to Rashid (2004:779) power electronics is increasingly used in applications that require gate drive circuits with advance control, high speed, high efficiency and compactness therefore, gate drive integrated circuits (ICs) that can perform this, are commercially available.

There are several techniques listed below that can be used to meet the gate drive requirements (Khan 2007:546). Each basic circuit can be implemented in a wide variety of configurations and can also come in a form of an IC package (Rashid 2004:779). Figures 18, 19, 20, 21 and 22 illustrate these techniques and their key features.

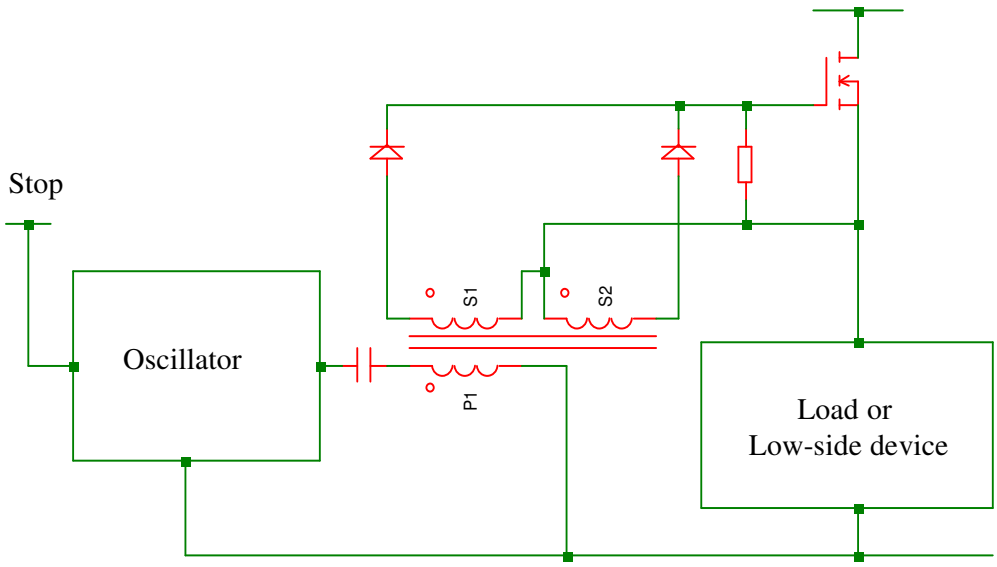

Figure 18: Basic block diagram of a carrier driver technique (Rashid 2004:780)

The key feature for the carrier gate-drive technique is that it gives full gate control for indefinite periods of time but is somewhat limited in switching performance; this can be improved with added complexity.

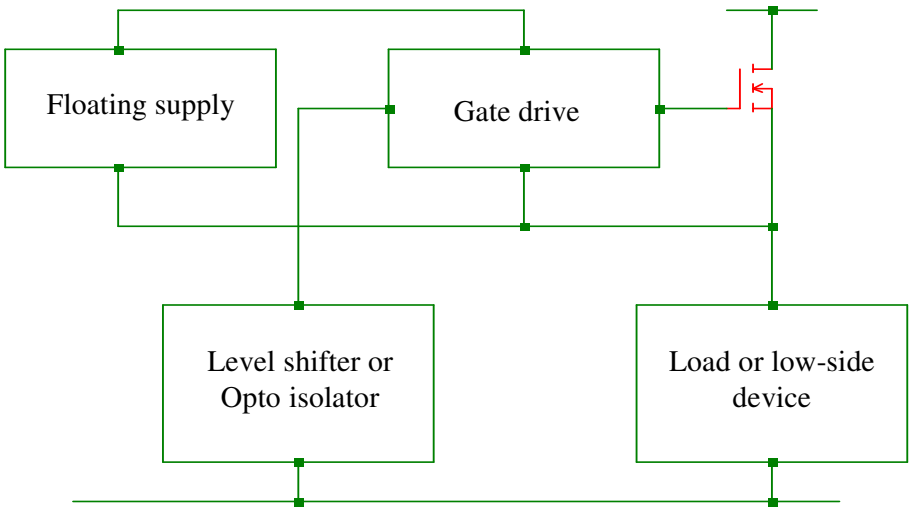

Figure 19: Block diagram of a floating supply gate-drive technique (Rashid 2004:779)

Key features for the floating supply gate-drive technique:

- Full gate control for indefinite periods of time.
- Cost impact of isolated supply is significant (one required for each high side MOSFET).
- Level shifting a ground referenced signal can be tricky. Level shifter must sustain full voltage, switch fast with minimal propagation delays and low power consumption.
- Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive.

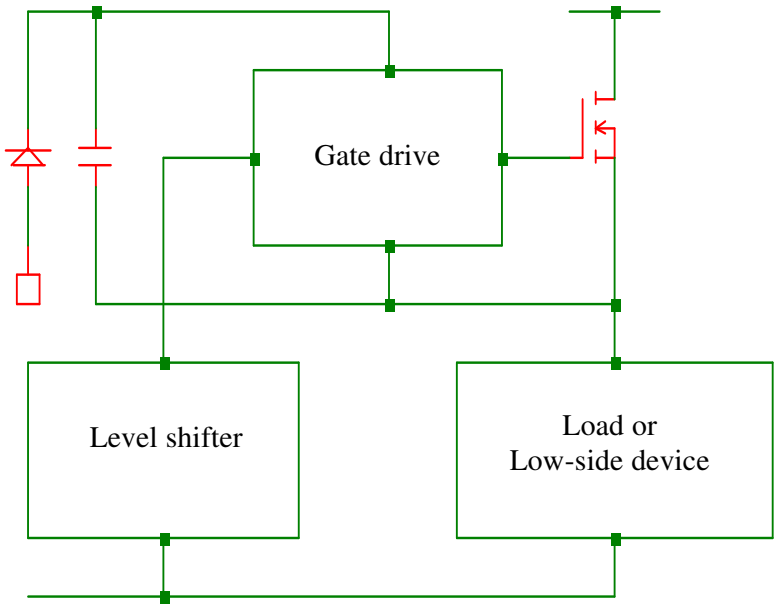

Figure 20: Basic block diagram of a bootstrap capacitor gate-drive technique (Rashid 2004:780)

Key features for the bootstrap capacitor gate-drive technique:

- Simple and inexpensive with some of the limitations of the pulse transformer, duty cycle and on time are both constrained by the need to refresh the bootstrap capacitor.

- If the capacitor is charged from a high voltage rail, power dissipation can be significant.
- Requires level shifter with its associated difficulties.

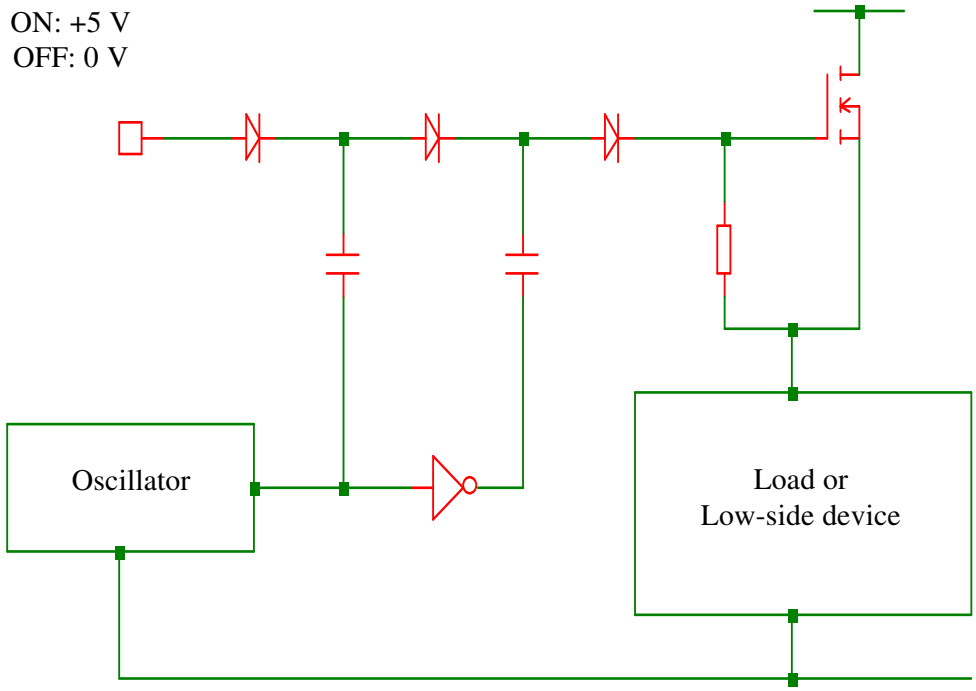

Figure 21: Basic block diagram of a charge pump gate-drive technique (Rashid 2004:780)

Key features for the charge pump gate-drive technique:

- Can be used to generate an 'over-rail' voltage controlled by a level shifter or to 'pump' the gate when MOSFET is turned ON.
- In the first case the problems of a level shifter have to be tackled.
- In the second case turn-ON times tend to be too long for switching applications.
- In either case, gate can be kept ON for an indefinite period of time.
- Inefficiencies in the voltage multiplication circuit may require more than two stages of pumping.

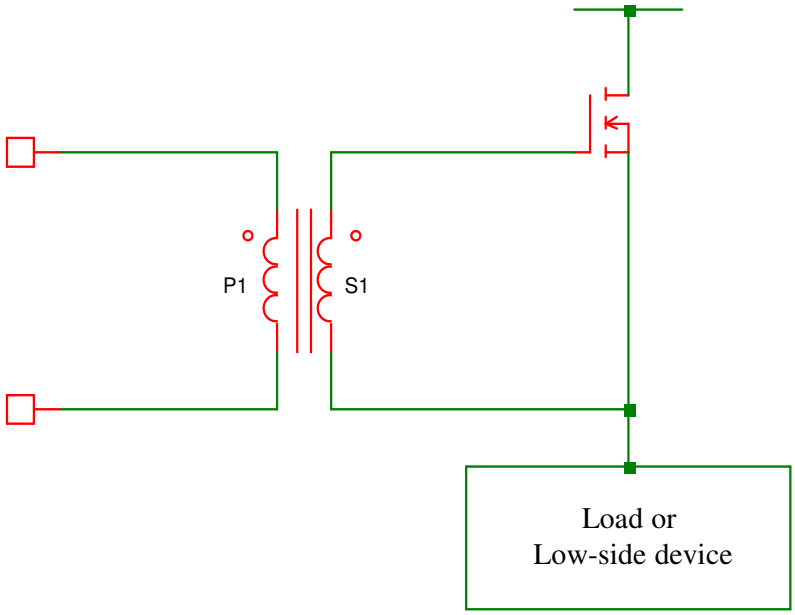

Figure 22: Basic block diagram of a pulse transformer gate-drive technique (Rashid 2004:779)

Key features for the pulse transformer gate-drive technique:

- Simple and cost effective but limited in many respects.
- Operation over wide duty cycles requires complex techniques.
- Transformer size increases significantly as frequency decreases.
- Being significantly parasitic creates less than ideal operation with fast-switching waveforms.

2.10 Floating Supply

The simplest way of generating a floating supply, is to use a transformer isolated supply (Mohan *et al.* 2003:703). Compared to other methods, this type of supply is able to supply a continuous, large amount of current. A mains frequency transformer supply is cheap, but is usually very bulky. By employing a high frequency isolated DC–DC converter, fed from an existing DC supply, an isolated floating supply can be generated employing a much smaller isolation transformer (Khan 2007:546).

2.10.1 Level Shifting

The second requirement for driving a switch module is that the control signal V_{sig1} as shown in Figure 23 fed from the PWM electronics needs to be conveyed to the floating driver circuitry. A level-shifting circuit is required in order to achieve this (Khan 2007:546).

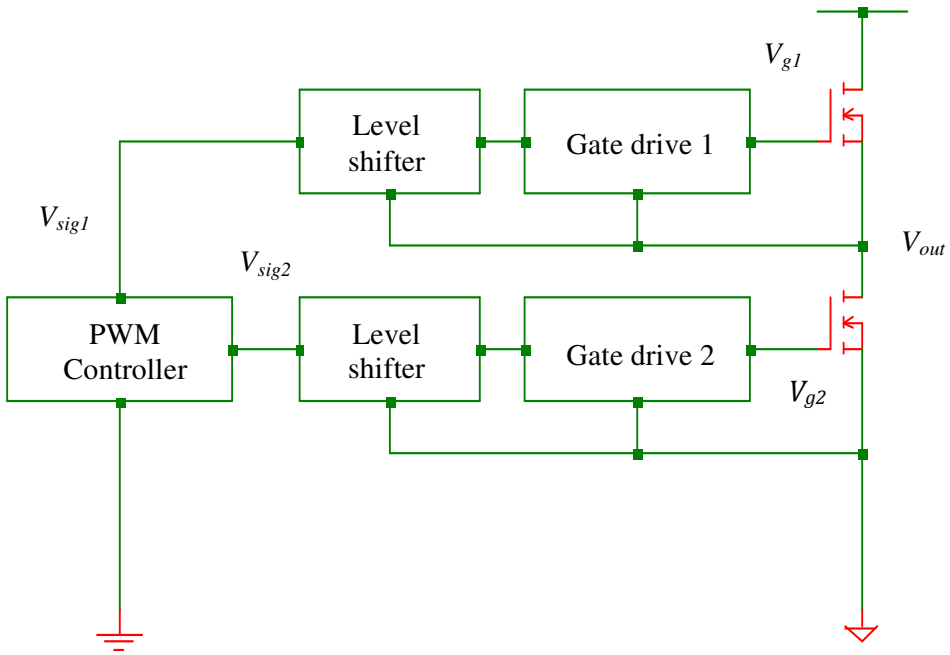

Figure 23: The concept of level shifting (Khan 2007:546)

The gate drive 1 and gate drive 2 are the respective high-side and low-side gate drive circuits. In order to signal the high-side gate driver circuitry to commence turn-ON of the high-side MOSFET switch, the control signal V_{sig1} which is normally referenced to the control circuit ground potential needs to be referenced to the floating potential V_{out} at the MOSFET 1 source (Andersen 2004:4). This implies that the control signal V_{sig1} will be level shifted to V_{g1} as shown in Figure 23. A level shifter can be thought of as an isolating black-box that transfers a signal across a potential barrier. The maximum level attained by V_{g1} will be $V_{out} + V_{sig}$. In power

converters, operating off the mains voltage, these levels can be in excess of 500 V (Khan 2007:546).

According to Mohan *et al*. (2003:703) level shifting is achieved in one of the following ways:

- Transformer level shifting,
- Optical level shifting by opto-couplers,
- Optical level shifting by fiber optic link and
- Electronic level shifting.

Optical isolation is another technique used for achieving level shifting and galvanic isolation (Waaben 1975:30). An opto-coupler, because it uses light waves to transmit the signal from one section to the other it is found to be a suitable circuit for galvanic isolation as in the schematic diagram shown in Figure 24 (Mohan *et al*. 2003:703).

According to Mohan *et al*. (2003:703) the only trade-off, however, is that a separate floating supply is now required on the receiver end of the gate driver interface. Opto-couplers offer a cost effective and easy solution, but are susceptible to noise and fast voltage transitions which are common in gate drive circuits (Bhattacharya 1994:474). This requirement places more demand on the power supply filtering and PCB layout around the opto-coupler in order to achieve reliable operation (Panov & Jovanovic 2005:827).

Other benefits of opto-coupler technology is the small footprint (6-8 pin dual in line or surface mount package), output enable pin and compatibility with any logic level input since its input is current-driven as presented in Annexure B. Typical opto-coupler isolation voltages are in the region of 5 kV which is sufficient, since most semiconductors breakdown voltages are lower than this (Khan 2007:548).

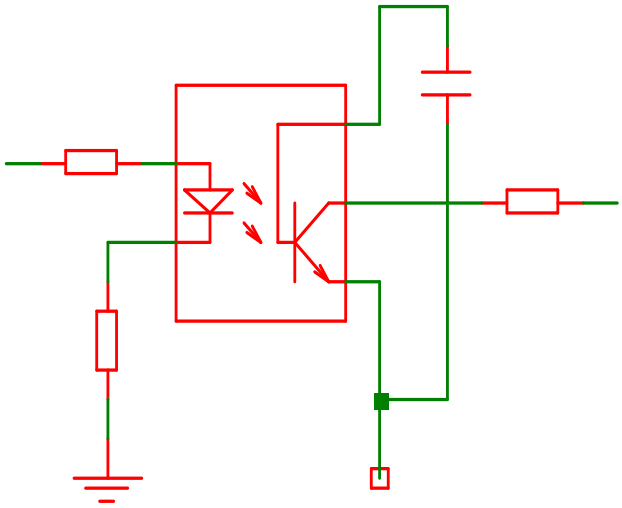

Figure 24: Schematic diagram containing an opto–coupling circuit (Mohan *et al*. 2003:703)

2.10.2 Selection of frequency

According to Dobbs (2005:8) the UC3825N is a high speed PWM controller which is compatible with both voltage and current mode topologies. Its practical operational switching frequencies are up to 1 MHz. Most of its features and the advantages that come with this IC are stipulated on its datasheet (Annexure C).

The selection of oscillator frequency (f_{osc}) can be done by either, choosing a timing capacitor C_T and then using the nomograph as shown in Figure 25 to select the timing resistor R_T according to the desired frequency or by using the formula in Eq. 15 and the datasheet to determine the components (Janse van Rensburg 2005:26). Suppose for 100 kHz, a capacitor of 10 nF can be chosen and then a resistor R_T would be calculated as shown in the equation 15 (Janse van Rensburg 2005:26).

$$R_T = \frac{1.25}{(f_{osc} \times C_T)} \tag{15}$$

$$R_T = \frac{1.25}{(f_{OSC} \times C_T)} = \frac{1.25}{100 \times 10^3 \times 10 \times 10^{-9}}$$

$$R_T = 1.25 \quad \text{k}\Omega$$

Timing Resistance vs. Frequency

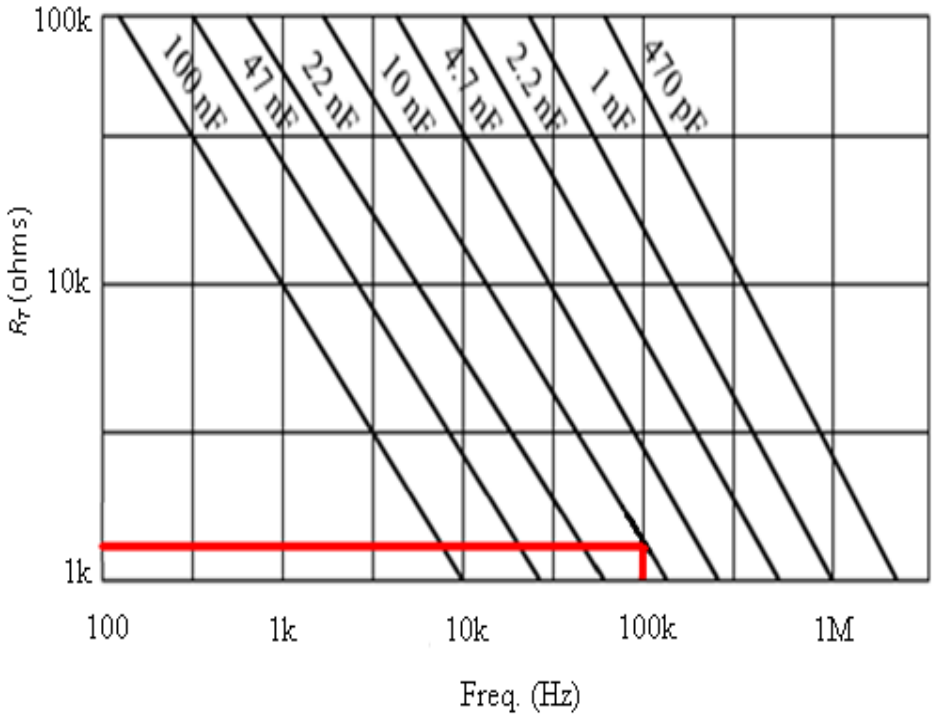

Figure 25: A simple C_T R_T nomograph (Janse van Rensburg 2005:26)

2.11 Power converters

Agrawal (2001:43) states that "power circuits and systems are constituted from inductors, capacitors, transformers, motors and switches. Therefore, power electronics is strongly dependent on the components' characteristics which in a real world are not very ideal."

2.11.1 Magnetic components and circuit design

The materials from which magnetic components are fabricated and the process of fabrication have a lot to do with the non-ideal behaviour of the components. Therefore, there must be an analysis based on the basic concepts and characteristics of these magnetic components (Agrawal 2001:43).

According to Sullivan (1999:283) a salient difficulty in the design of high-frequency inductors and transformers is eddy-current effects in the windings. These effects include skin-effect losses and proximity-effect losses which otherwise limit the performance of high-frequency magnetic components (Schaef & Sullivan 2012:1011).

2.11.2 Skin effect and proximity effect in Litz-wire

The skin effect refers to the tendency of current flow in a conductor to be confined to a layer in the conductor close to its outer surface. Proximity effect is the tendency for current to flow in loops or concentrated distributions due to the presence of magnetic fields generated by nearby conductors (Sullivan 1999:283). The DC impedance of a conductor which has a circular cross-section, is uniform and may be said to consist of a resistance per unit length of conductor is given by:

$$R_{DC} = \frac{1}{\pi r^2 \sigma} \tag{16}$$

Where:

$\sigma \equiv$ Material conductivity

$r \equiv$ Radius of the wire

The wire will also exhibit an effective inductance per unit length at very low frequency due to its internal fields (Shen, De Rooij, Odendaal, Van Wyk & Boroyevich 2003:888). At low frequencies this has the value

$$L = \frac{\mu_o}{8\pi} \tag{17}$$

Where:

$$\mu_o \equiv 4\pi \times 10^{-7}$$

The electrical resistance of the conductor with all its cross-sectional area in use is known as the 'DC resistance' with the AC resistance of the same conductor referring to a higher figure resulting from the skin effect.

According to Pressman (1991:300) the degree to which frequency affects the effective resistance of a solid wire conductor is impacted by the gauge of that wire. As a rule, large-gauge wires exhibit a more pronounced skin effect than small-gauge wires at any given frequency. The equation for approximating skin effect at high frequencies is given by:

$$R_{AC} = (R_{DC})(w)\sqrt{f} \tag{18}$$

Where:

$R_{AC} \equiv$ AC resistance in Ω
$R_{DC} \equiv$ DC resistance in Ω
$w \equiv$ Wire gauge in m
$f \equiv$ Frequency of AC in (MHz)

Bartoli, Noferi, Reatti, & Kazimierczuk (1996:1691) state that in transformers and inductors proximity effect losses are generally more significant than skin effect losses. In Litz wire windings, proximity effect may be sub-divided into internal proximity effect and outer proximity effect. The reason for twisting or weaving Litz wire, rather than just grouping fine conductors together is to ensure that the strand currents are equal. Simple twisted bunched conductor wire can accomplish this adequately where proximity effect would be the only significant problem with solid

wire. Where skin effect would also be a problem, more complex Litz wire construction can be used to ensure equal strand currents. Therefore, in a well designed construction, strand currents are nearly equal (Pressman 1991:300).

According to Xi & Sullivan (2009:855) the multi-strand configuration or Litz wire construction illustrated in Figure 26 is designed to minimise the power losses exhibited in solid conductors due to skin effect and also to reduce the severe eddy-current losses that otherwise limit the performance of high-frequency magnetic components. At low frequencies, skin effect is negligible and current is distributed uniformly across the conductor. However, as the frequency increases the depth to which the flow can penetrate is reduced.

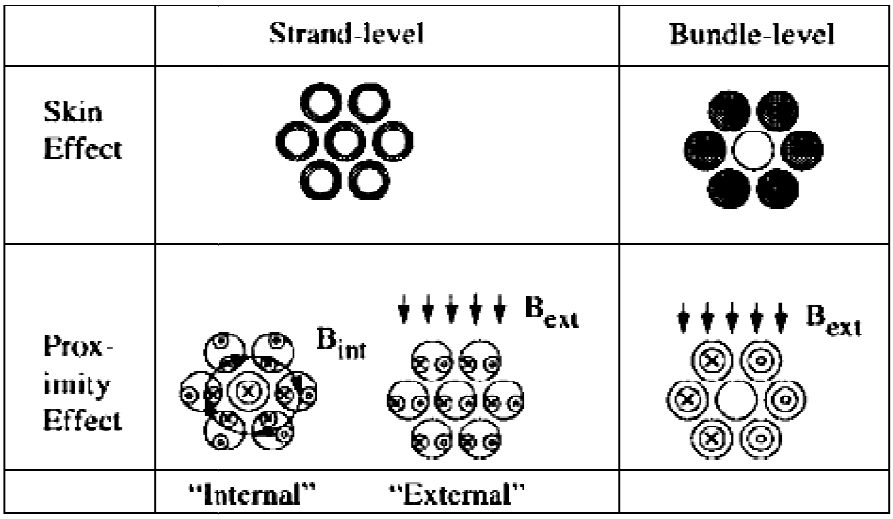

Figure 26: Types of eddy-current effects in Litz wire (Sullivan 1999:284)

Litz wire constructions counteract this effect by increasing the amount of surface area without significantly increasing the size of the conductor (Xi & Sullivan 2009:855). The problems of skin effect and eddy-current loss that the finite conductivity of magnetic components causes, is also largely avoided in ferrite core materials. The very large resistivity found in ferrites minimises these problems (Xu & Sullivan 2003:289).

2.12 DC-DC switch-mode converters

The DC-DC converters are widely used in regulated switch-mode DC power supplies and in DC motor drive applications. The input to these converters is an unregulated DC voltage, which is obtained by rectifying the line voltage and therefore, it will fluctuate owing to changes in its line-voltage magnitude. Switch-mode DC-DC converters are used to convert the unregulated DC input into a controlled DC output at a desired voltage level (Mohan *et al*. 2003:161).

2.12.1 Non-isolated DC-DC buck converter

Buck converters are in widespread use to provide high current, low voltage power for CPUs, chipsets, peripherals and many more (Kazimierczuk 2008:24). An important characteristic of this topology is that it does not need transformers and the voltage stress for the switch is relatively low when compared to other isolated DC-DC converter topologies (Lee 1993:6).

The step-down DC-DC converter topology, commonly known as a buck converter, is as shown in Figure 27.

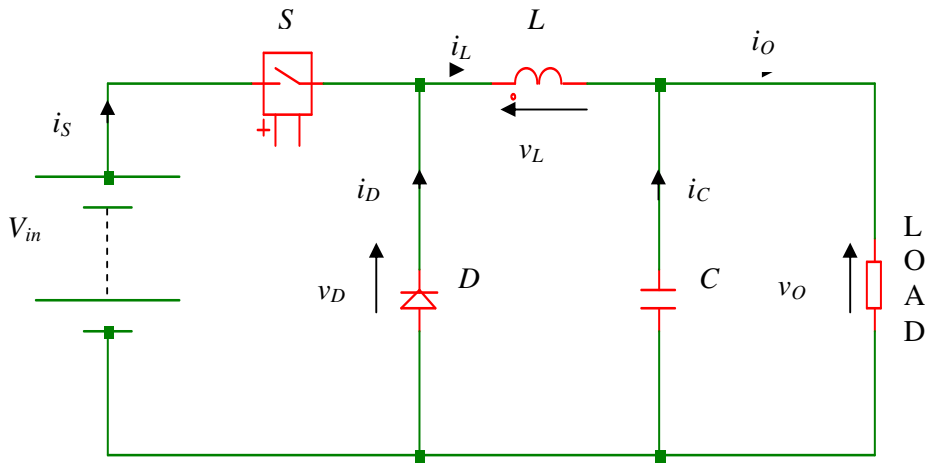

Figure 27: Circuit diagram of the buck converter (Kazimierczuk 2008:24)

It consists of a DC input voltage source V_{in}, controlled switch *S*, diode *D*, filter inductor *L*, filter capacitor *C* and load. According to Janse van Rensburg (2012:102) the output voltage is lower than the supply voltage and its magnitude is directly proportional to the duty cycle of the switch which is operated at a high frequency.

The converter action can be divided into two distinct periods:

- Switch *S* closed: When switch *S* is closed, the diode *D* is reversed biased and does not conduct. The current via the inductor *L* increases linearly during this period. Energy is thus transferred into the inductor's magnetic field. The energy in an inductor's magnetic field is given by $W = \frac{LI^2}{2}$.
- Switch *S* open: When the switch *S* is opened, the inductor polarity is reversed $\left(v = L\frac{di}{dt} \right)$ thereby forward biasing the diode *D*. The inductor current decreases linearly during this period.

The inductor current, whether increasing or decreasing is shared by the capacitor *C* and load. Taking the load current as essentially constant, it can be noted that while the inductor current exceeds the load current, the capacitor takes up the difference and is charged. Also, when the load current exceeds the inductor current, the capacitor supplies the difference and is discharged. The nett charge and discharge over one cycle is zero so the capacitor voltage stays essentially constant (Janse van Rensburg 2012:102). Figure 28 shows waveforms for the voltage and currents.

The converter was analyzed mathematically with the assumptions that the switching action of the converter has reached a steady-state (Kazimierczuk 2008:24). The waveforms shown for the supply, the inductor, the load voltages and the load currents are just for a continuous current flow in the inductor *L* (Janse van Rensburg 2012:104).

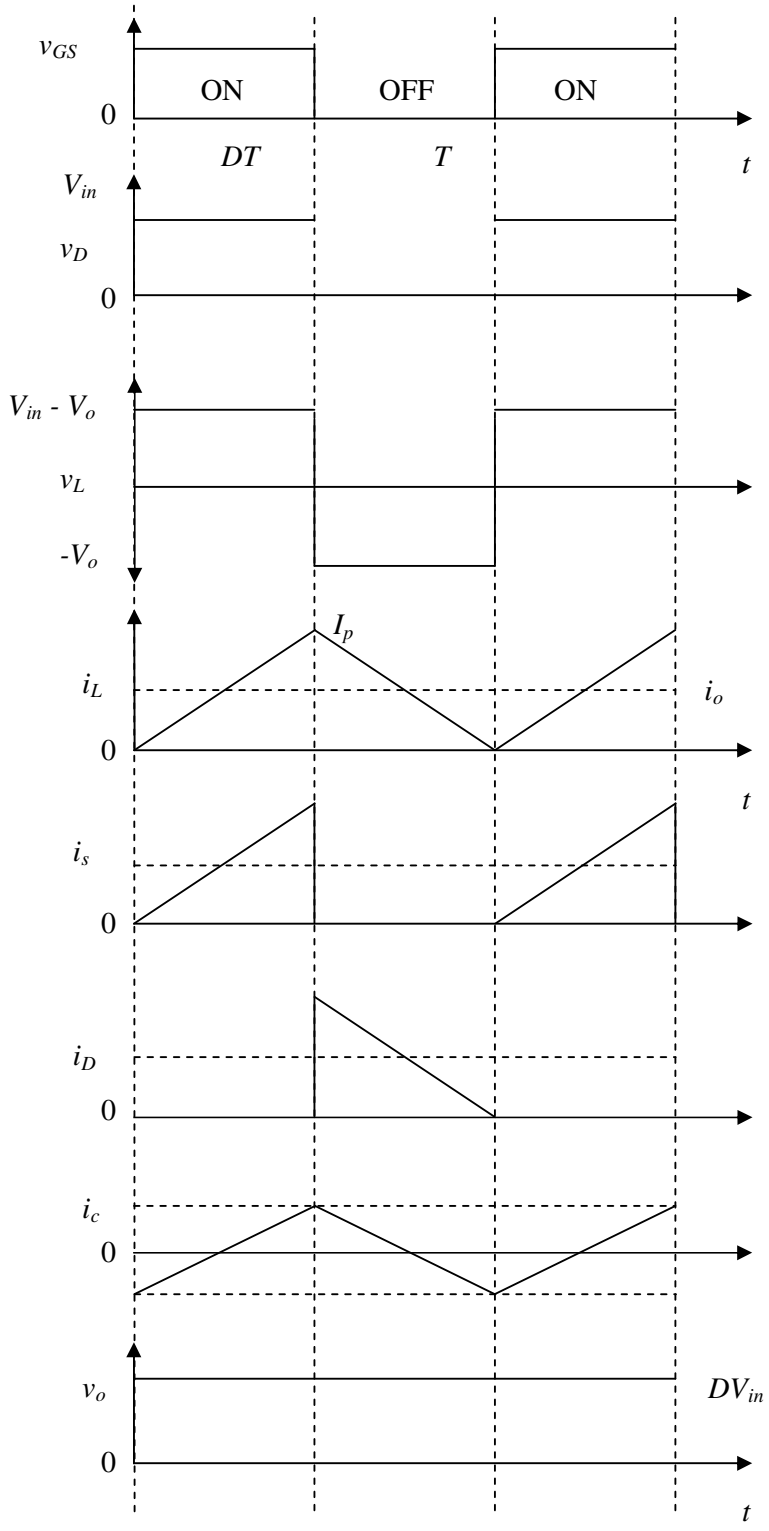

Figure 28: Voltage and current waveforms for the buck converter (Janse van Rensburg 2012:103)

2.12.2 Isolated DC-DC converter topology

According to Kularatna (2008:129) bridge converters are generally used for higher-power and higher-voltage conversion because there are several power switches to share the dissipation and the voltage stress. In general, half-bridge and full-bridge topologies are used for very high-power application and it is quite important to consider the losses in the circuits and the design complications due to their high-side switches operating with their source terminals (in the case of MOSFETs) or emitters (in IGBTs or power transistors) at floating levels (Rossetto & Spiazzi 1997:983). Transistors on the upper parts of the bridge (high-side transistors) require special circuitry to drive floating gate terminals.

As Kularatna (2008:129) stated that, in a high-power DC-DC converter design, to achieve adequate efficiency an efficiency budget or a loss calculation should be developed. In general, losses are contributed from many different sources and the important ones are (Hyosang, Taeyoung & Byungcho 2009:41):

- Rectification losses (low-frequency rectifiers on the input side and high-frequency rectification circuits on the output side),
- Switching losses in power semiconductors,
- Core losses in magnetic components,
- Losses owing to control and supervisory circuits and
- PCB losses associated with high-current tracks on the PCB board.

2.12.3 Half-bridge converter

According to Lee (1998:126) in half-bridge or full-bridge circuits based on MOSFETs, low-side (n-channel) transistors need to be driven by a positive gate voltage with respect to the ground plane, but the high-side transistors' gate needs to be driven by a positive voltage with respect to its source terminals. This topology has the advantage of minimal switches and low stress across switches (Jain, Jain & Daniele 1997:548). According to Kazimierczuk (2008:289) gate-driver circuits are

useful in any switching systems topology where two switches operate at high and low sides as shown in Figure 29.

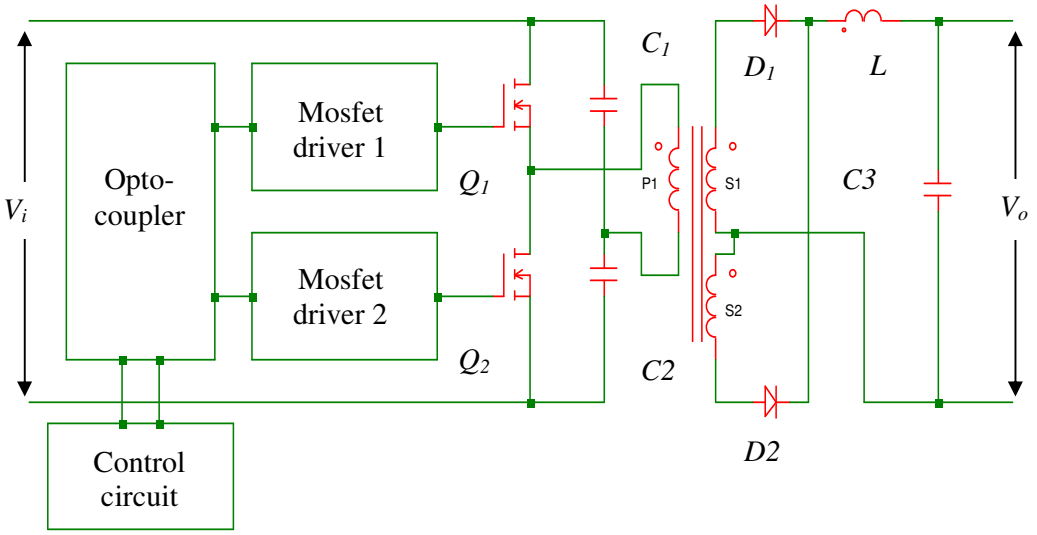

Figure 29: Basic half-bridge converter topology (Lee 1993:9)

Simultaneous conduction of top and bottom switches in the half-bridge (as well as full-bridge) configuration should be avoided at all cost, because it causes a short circuit in the primary part of the converter, commonly resulting in harmful effects (McLyman 1997(a):984). Therefore interlock delay is required to determine the correct or required switching sequence of the switches (Lee 1998:126).

To justify the use of these for efficient power circuit designs, an understanding should be maintained and attention should also be paid to the parasitic capacitances at the gate input (Kularatna 2008:130).

2.12.4 Interlock delay time minimization for half-bridge DC-DC converter

According to Jalakas, Vinnikov, Lehtla & Bolgov (2009:438) the selection of a proper interlock delay time for voltage-sourced inverters with MOSFETSs or IGBTs

in switch mode power converters is very important. Too long an interlock delay time may lead to higher filtering inductances and increased semiconductor losses (Kularatna 2008:130). Too small an interlock delay can cause the shoot through of inverter bridge arms, input voltage distortion, shortened lifespan of transistors and even a failure of semiconductor switching devices (McLyman 1997(a):984).

Theoretically, the minimum interlock delay time between switching different inverter arm transistors ON and OFF is the maximum control signal propagation delay from the control system to the MOSFET/IGBT plus the time that a MOSFET/IGBT needs to turn ON or turn OFF as shown in Figure 30 (Jalakas *et al*. 2009:438).

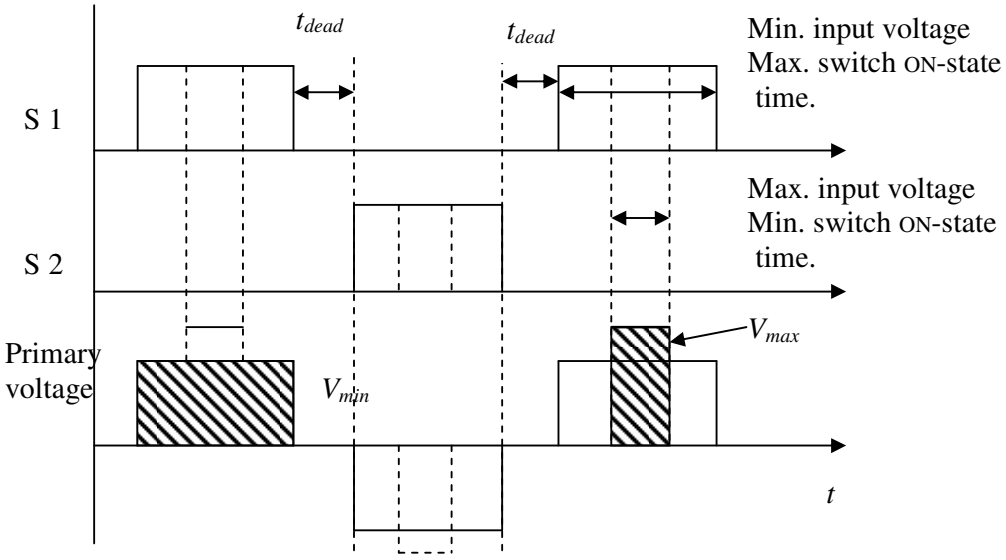

Figure 30: Timing diagrams of a half-bridge converter (Jalakas *et al*. 2009:438)

The duty ratio of inverter switches is controlled in accordance with the input voltage. The most challenging operational point of the converter is at the minimum input voltage, when the switch ON-state time becomes maximal as shown in Figure 30. Here, the threat related to the cross conduction of top and bottom arm transistors should be considered (Pressman 1991:93-100). Jalakas *et al*. (2009:438) studied these converters and came up with the way in which the interlock delay time can be minimized (See Figure 31).

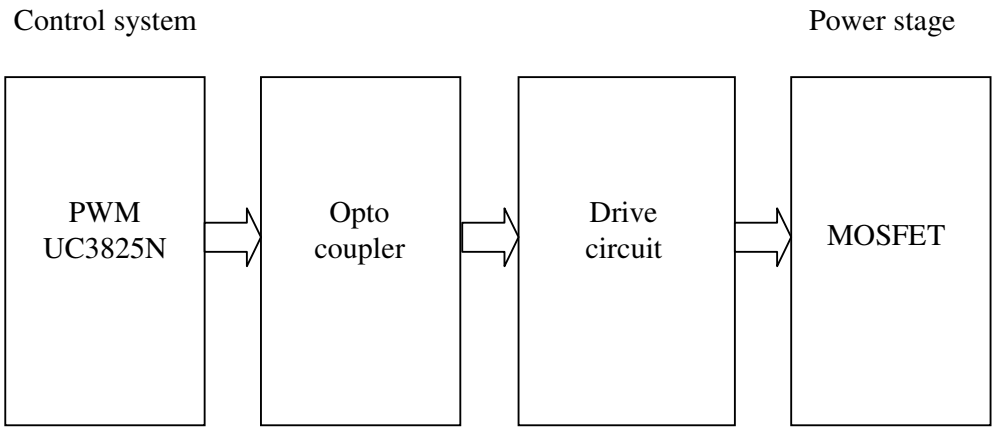

Figure 31: Control signal flow in the experimental converter (Jalakas *et al.* 2009:438)

To calculate the right delay time, the signal propagation delay from the control system to the MOSFET/IGBT must be known, including the turn-ON delay, the turn-OFF delay as well as the rise and fall times of the transistors as presented in Figure 32.

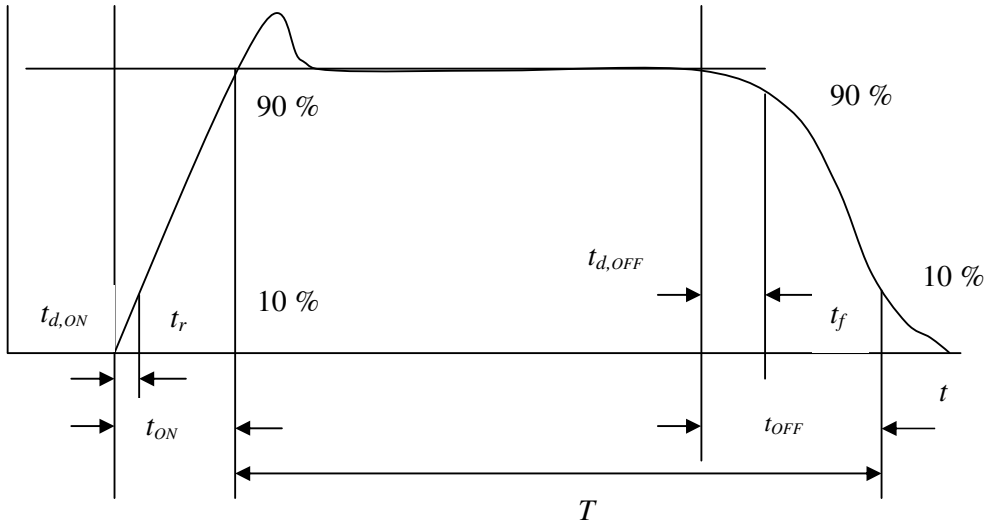

Figure 32: Switching transients of a typical MOSFET (Jalakas *et al*. 2009:438)

Equation 19 (overleaf) sums all these delays and the result is multiplied with the safety margin *b*

$$t_d = \left[(t_{OFF\_\max} - t_{ON,\min}) + (t_{PD\_\max} - t_{PD,\min}) + (t_{PD\_CS,\max} - t_{PD\_CS,\min}) + (t_{OT,\max} + t_{OT,\min}) \right] \times b \quad (19)$$

Where:

$t_{OFF\_\max}$ ≡ maximum turn-OFF time of the transistor in ns

$t_{ON\_\min}$ ≡ minimum turn-ON time of the transistor in ns

$t_{OT,\max}$ ≡ maximum propagation delay of the opto-coupler in ns

$t_{OT,\min}$ ≡ minimum propagation delay of the opto-coupler in ns

$t_{PD\_\max}$ ≡ maximum propagation delay of the driver in ns

$t_{PD\_\min}$ ≡ maximum propagation delay of the driver in ns

$t_{PD\_CS,\max}$ ≡ maximum propagation delay of the control system in ns

$t_{PD\_CS,\min}$ ≡ minimum propagation delay of the control system in ns

Equations 20 and 21 relate to the delays when the high power MOSFETs are turned OFF and when they are turned ON. This is due to the structure of these transistors when they are in operation.

$$t_{OFF,\max} = t_{d\_OFF,\max} + t_{f,\max} \quad (20)$$

$$t_{ON,\min} = t_{d\_ON,\min} + t_{r,\min} \quad (21)$$

Where:

$t_{d\_OFF,max}$ ≡ the maximum turn- OFF delay time of the transistor in ns

$t_{f,max}$ ≡ maximum fall time of the transistor in ns

$t_{d\_ON,min}$ ≡ the minimum turn- ON delay time of the transistor in ns

$t_{r,min}$ ≡ minimum rise time of the transistor in ns

All delays and transition times of all the devices in the signal flow path in the experimental device are given on their respective datasheets. To achieve proper regulation, the inverter switch duty cycle must change proportionally to the input

voltage change, while the maximum and minimum switch duty cycles should be selected upon the system requirements (Jalakas *et al*. 2009:439).

2.13 Single-phase AC voltage control

According to Mazda (1997:169) regulation of the AC power circuits to a load by phase-control methods has several disadvantages, one being the high harmonic content in the output which is especially evident at large delay angles. Sub-harmonic frequency components may be generated that are undesirable as they may set up sub-harmonic resonance in the power supply system. According to Rashid (2001:312) these may cause a lamp to flicker and may interfere with the natural frequencies of the system loads causing shaft oscillations. An alternative to phase control is chopper regulation, which is illustrated in Figure 33.

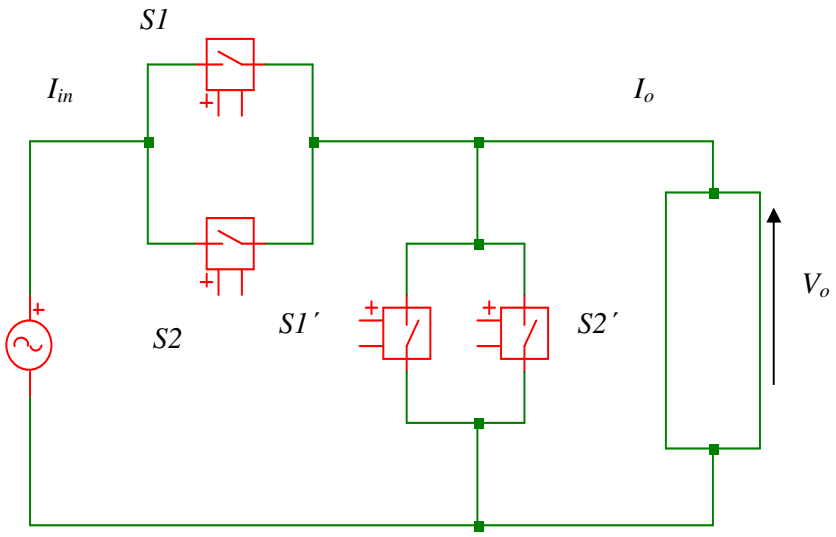

Figure 33: Circuit diagram of an AC regulator (Rashid 2001:312)

The performance of AC voltage controllers can be improved in terms of harmonics, quality of output current and input power factor by pulse width modulation (PWM) control in PWM AC choppers (Rashid 2001:312). To operate an AC chopper, fully controlled switches *S1* and *S2* connected in anti-parallel are turned ON and OFF many

times during the positive and negative half-cycles of the input voltage respectively, *S1'* and *S2'* provide the freewheeling paths for the load current when *S1* and *S2* are OFF (Mazda 1997:169). An input capacitor filter may be provided to attenuate the high switching frequency current drawn from the supply and also to improve the input power factor (Janse van Rensburg 2005:57). According to Mazda (1997:170) when the power semiconductor switch *S1* is closed for some period *t*, power is supplied to the load from the AC supply given by:

$$v'_s = V_m \sin \omega_p t = \sqrt{2} V_s \sin \omega_p t \tag{22}$$

Where:

$V_s \equiv$ input AC signal

$V_m \equiv$ peak input AC signal

$\omega_p \equiv$ radian frequency

The magnitude of the load voltage is equal to the AC source provided the voltage drop across *S1* is neglected. For an inductive load, *S2* must be closed when *S1* opens the load current free-wheeling in *S2* and its voltage is low. Assuming that *S1* is open for a certain period the load waveforms are as in Figure 34. It can be seen that the voltage across the load can be controlled by changing the ON period during an operating cycle (Mazda 1997:170). The specific mode of control selected in this study for the control of an AC chopper is 'equal time ratio control' (ETRC), since it provides a linear relationship between the fundamental component and the control variable *D*. This eases the control of the chopper considerably (Addoweesh 1993:1001).

According to Janse van Rensburg (2005:57) the more inductive the load, the nearer the rms value of the output current is to that of the fundamental. This is also dependent on the ratio between chopping frequency and that of the AC waveform (Janse van Rensburg, Nicolae & Case 2005:2). It should be pointed out that there are two frequencies in this system. One is the utility supply frequency (f_p = 50 Hz) and

the other one is the chopping frequency (f_c) which is much higher than the utility frequency. The situation described can be seen to be as that of a train of amplitude modulated pulses as shown in Figure 34 (Janse van Rensburg 2005:57).

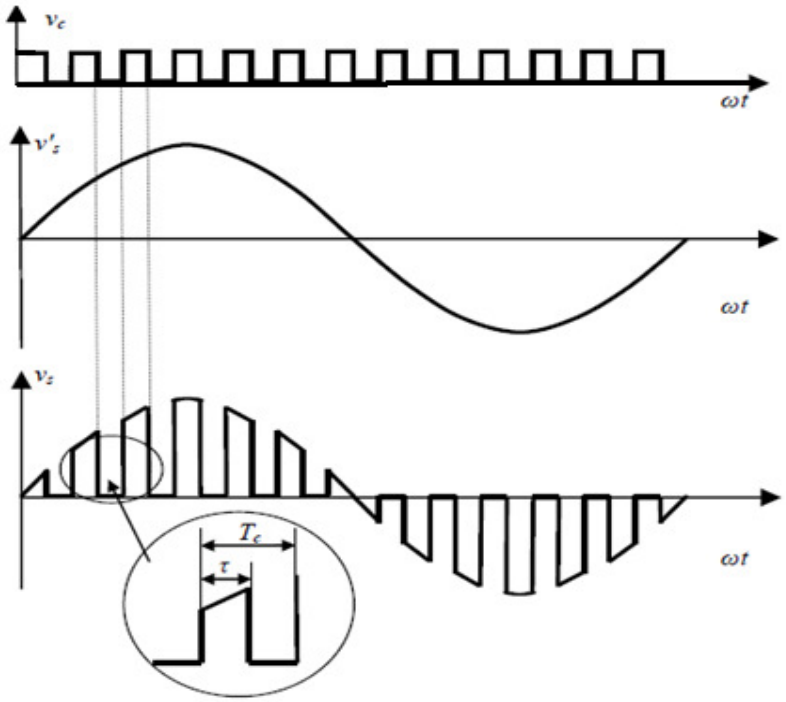

Figure 34: Output waveform in AC choppers (Janse van Rensburg 2005:57)

The mathematical expression for the waveform can be obtained as:

$$v_s(t) = v_c(t) \times v'_s(t) \tag{23}$$

Where:

$v'_s \equiv$ is given by eq. 22 and

$v_c \equiv$ the control signal

According to Mazda (1997:169) the rms output voltage function can be given as:

$$v_O = (D)V_S \tag{24}$$

Where:

$D \equiv$ duty cycle

Equations 23 and 24 reveal that the load voltage v_o depends largely on the duty cycle of the control frequency and the input voltage. This shows that there is a direct conversion from alternating source to the load with the possibility of controlling the output voltage via the duty cycle (Janse van Rensburg *et al.* 2005:2).

2.14 Heat dissipation

Physical construction of the MOSFET module is very important to achieving the maximum performance and reliability, especially if the application pushes the limits of the MOSFETs used (Smith, Montague, Sniegowski, Murray & McWhorter 1995:610). Therefore, smooth faced-off aluminium bars or commercially available heat-sink can be used as in Figure 35 (Swart & Pienaar 2007:5).

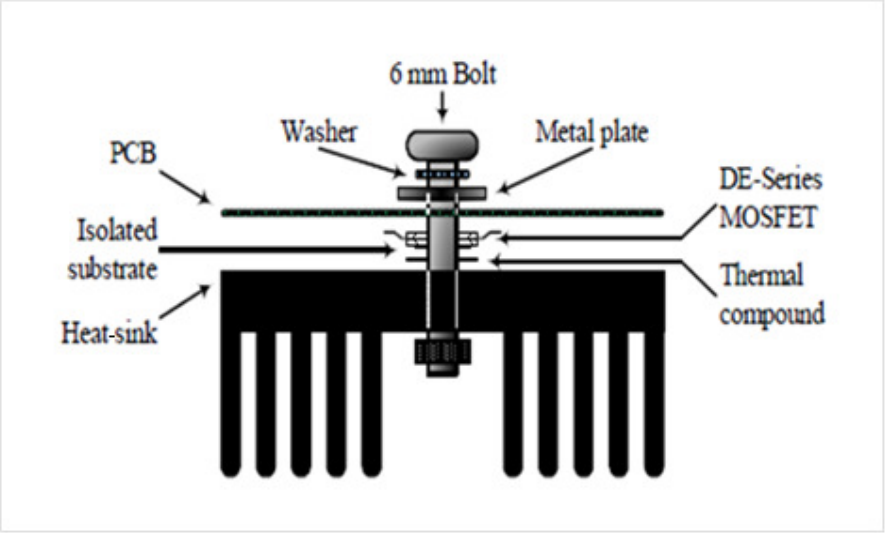

Figure 35: Mounting a MOSFET on a heat-sink (Swart & Piennar 2007:5)

According to Swart & Pienaar (2007:5) good heat sinking is critical and important to protect MOSFETs against excessive heating. Thermal paste is used on the drain tabs and fans to improve thermal conductivity. Brass screws through the drain tabs give a very low resistance electrical connection. This also minimizes soldering and makes replacing individual MOSFETs very simple and easy (Colton 2009:16)

2.15 Summary

This chapter considered the history of power electronics and the need for switching in power processing. The switch module was reviewed in full with its structure, the operation and all the components that make it up. These components as well as their characteristics and the advantages that go with were discussed and reviewed. This chapter also covered the analysis of different kinds of DC-DC converters and also AC conversion.

The next chapter will concentrate on the actual design of the switch module and all the converters that will be used to test and verify the characteristics of the module.

Chapter 3 Design aspects of the switch module

The previous chapter explained and related the literature concerning the design of the power switch module. Drive circuit techniques and requirements were discussed and the bi-directionality of the module was also discussed together with the galvanic isolation technique.

This chapter focuses on the practical design of the power switch module and additional converter topologies as well as their magnetic components. The module is used to validate computer simulations and mathematical calculations for power converters.

3.1 Introduction

According to Lenk (2005:225) the general idea of worst-case analysis (WCA) is to take each and every component of the design, find its worst possible value(s) for the function or functions it is intended to perform and verify, either mathematically or through simulations that the function is correctly performed even when all these worst-case values occur simultaneously.

The development and characterization of the power switch module and its functional materials in particular, is based on low cost materials and to commercially available components. In order to realize full commercialisation, cost of manufacturing should be minimised. As part to achieving this, proper selection of materials for the manufacturing should be made but without compromise to quality (Kularatna 2008:32).

3.2 A detailed circuitry of the bidirectional switch module

Hardware design consists of an isolated DC floating power supply, opto-coupler, drive circuit and the power stage. Figure 36 shows a detailed circuitry of the switch

module which is used as the simulation model. Any control circuit can be used to provide the signal to the module.

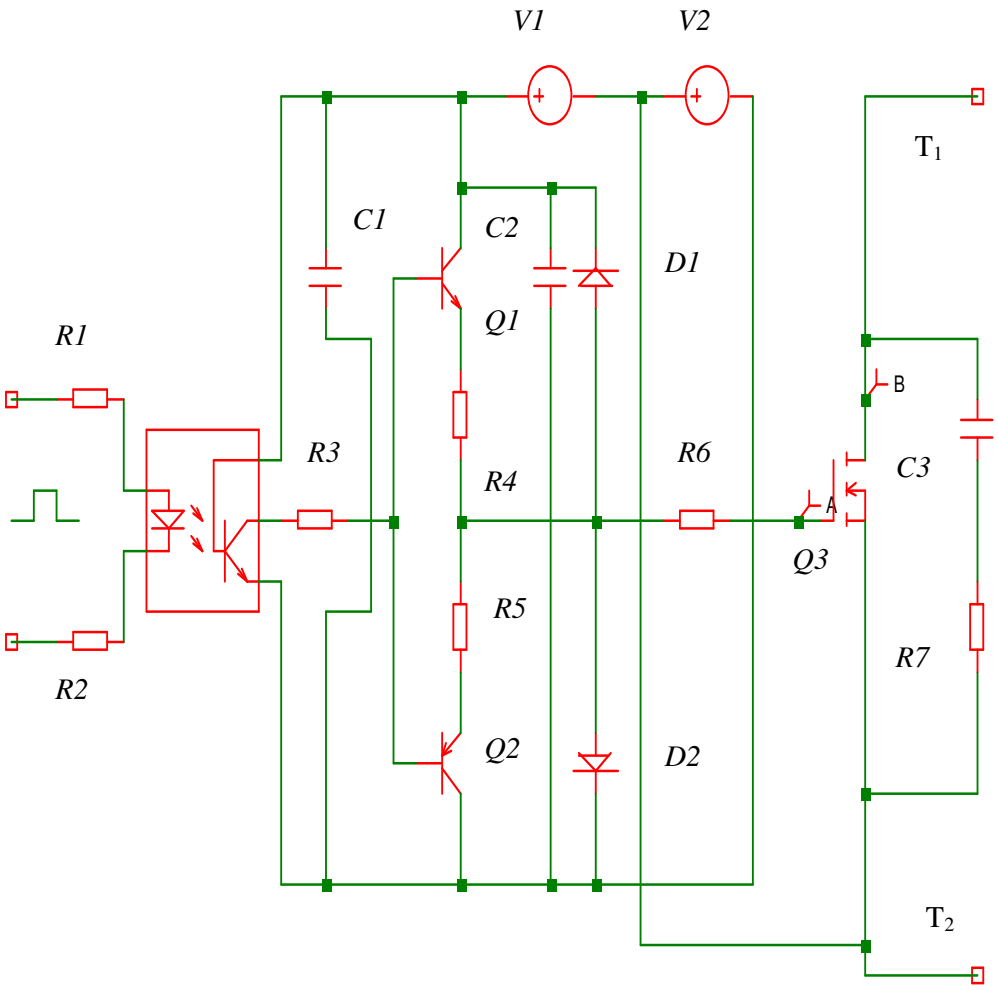

Figure 36: A detailed circuitry of the bidirectional switch module

The negative terminal of supply *V1* and the positive terminal of supply *V2* were connected together as ground and connected to the source terminal of the power MOSFET *Q3* as shown in the Figure 36 (Khan 2007:543). This idea was broken down into smaller functional blocks and then modeled as shown in Figure 37 where simulation graphs provide the basis for a floating voltage supply.

3.2.1 Isolated power supply

The floating power supply was provided by a galvanic isolated power supply designed especially for this application as shown in Figure 37. The system was fed from a single phase 220 V AC power supply which was transformed to 16.5 V rms voltage. The simulation model of the power supply produced the simulation graph in Figure 38 where the AC voltage has been stepped down to 16.06 V rms as the transformer requirements have shown. The voltage was then rectified to DC using a single phase bridge rectifier circuit (*D3-D10*) and the voltage regulators 7815 and 7915 to ± 15 V DC. Figure 39 presented the simulation of the rectified voltage which has been regulated to positive 15 V and negative 15 V.

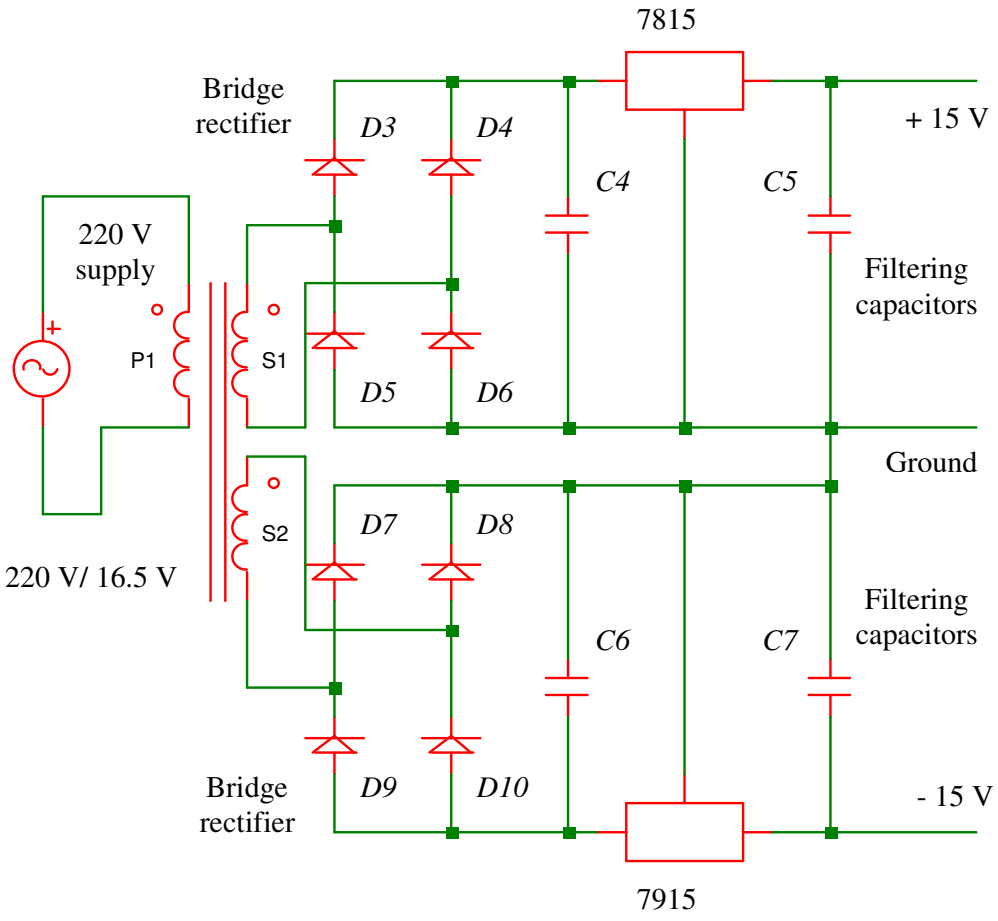

Figure 37: Isolated power supply for a gate-drive circuit

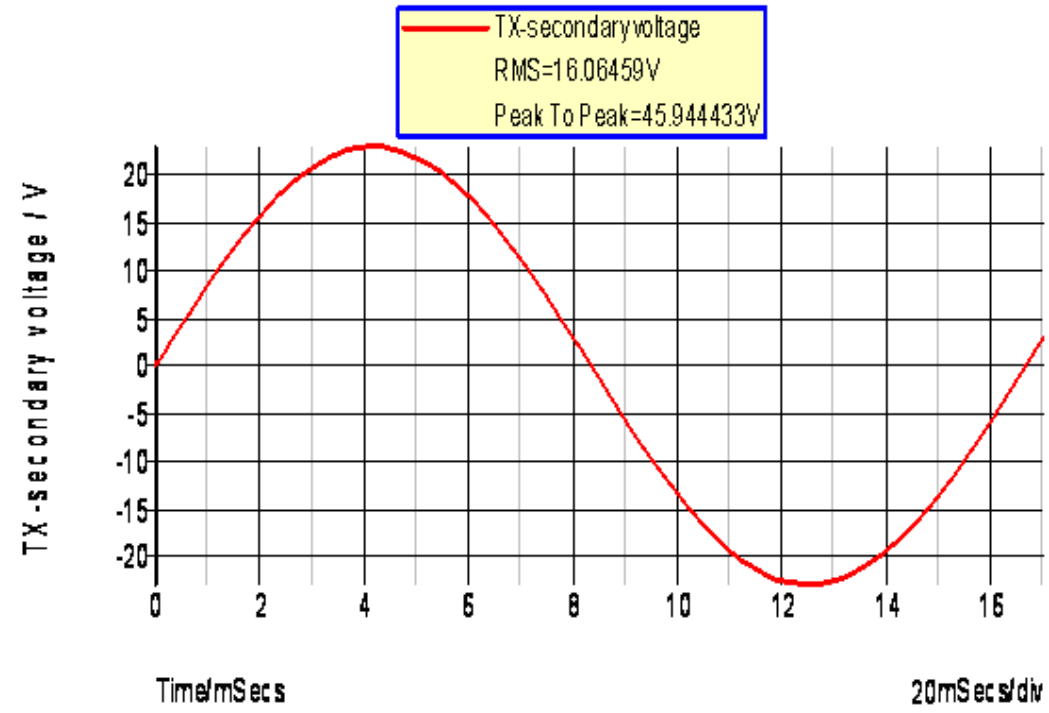

Figure 38: Transformed V_{AC} supply

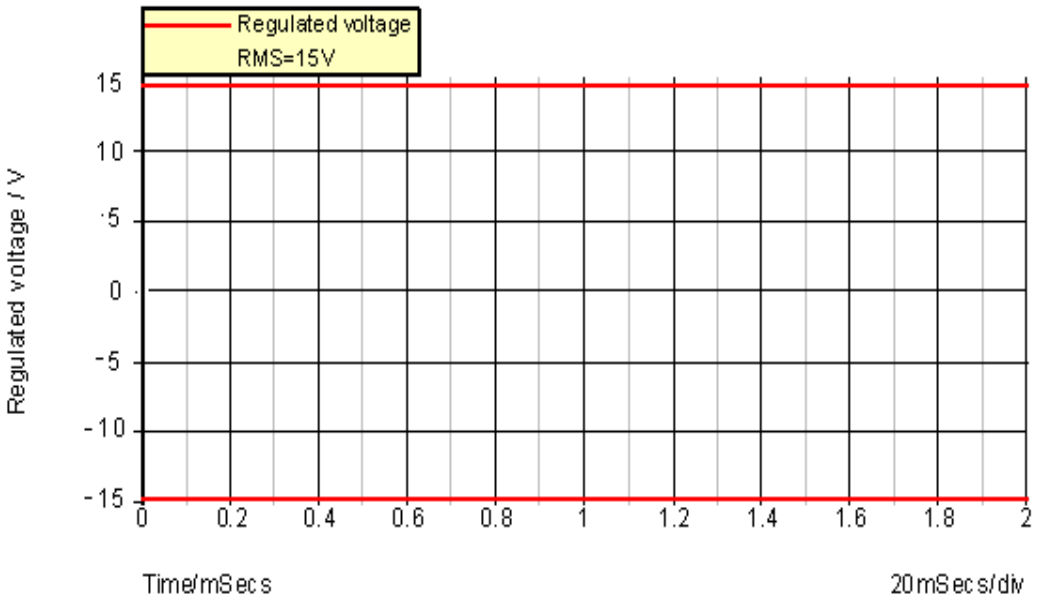

Figure 39: Regulated dual supply 15-0-15 V

3.2.2 Opto-coupler circuit

Resistors *R1* and *R2* were used to protect the input of the opto-coupler and the output was also protected by decoupling it with a 100 nF capacitor *C1*. The receiver end of the opto-coupler was also connected to the floating supply. Pin 1 and pin 4 were not connected, only pins 2 and 3 were used as input. Pin 8 was connected to the positive terminal and pin 5 was connected to the negative terminal of the floating supply. In that way the supply voltage is floating and the high current transients of driving the gate were localised in a very small loop area, reducing the value of parasitic inductances (Balogh 2001:12). Pin 6 and pin 7 are used as outputs. This type of opto-coupler has a built-in drive circuit which isolates and amplifies the signal according to the voltage signal required. The datasheet for this type of an opto-coupler is provided in Annexure B.

3.2.3 Gate-drive circuit

The gate-drive circuit consists of *Q1* (BC 327 pnp) and its complement *Q2* (BC 337 npn) transistors due to their more efficient area utilisation and better performance (Khan 2007:543). The BC type of transistors have low voltage and high current features, have a transition frequency (f_T) of 100 MHz, are able to source 1 A of current and their general purpose is for switching driver circuits. Their datasheets are provided in Annexure D and E respectively. The driver circuit is decoupled with a 100 nF capacitor *C2* placed across the collectors of the upper npn and lower pnp transistors (Balogh 2001:12). The emitters of the gate-drive transistors were also protected by two resistors *R4* and *R5* which also limit the current that is going into the gate of the MOSFET. This is done to protect the switch from overheating that could result in high losses and/or damage to the MOSFET (Khan 2007:544).

3.2.4 Driver protection

Balogh (2001:12) indicated that direct drive and gate-drive ICs using a bipolar output stage must be provided with a suitable protection for the output bipolar transistors

against reverse currents. To provide a path for reverse currents, low forward voltage drop Schottky diodes *D1* and *D2* have been provided to protect the output as shown in Figure 36. The diodes have been placed very close to the output pins and to the bypass capacitor. The gate resistor (*R6*) was chosen in such a way that it has an influence in the speed of switching, determines the switching losses of the converter and also the required delays for the commutation.

3.3 Choice of switches

The IRF530N MOSFETs were chosen because of their very low $R_{DS\,(ON)}$ (0.16 Ω) to carry the input current of 14 A at 100 V, the reason being to reduce the high power losses (Smith *et al* 1995:610). So as to protect and prolong their lifespan, semiconductors have to be operated within the limits given on their datasheets (Vishay Siliconix 2010:2). According to Rashid (2004:150) MOSFETs have a positive temperature coefficient and because of this, paralleling and operation is much easier. But care must also be taken because paralleling may also lead to ringing and unwanted oscillations from the leakage inductance and capacitance.

3.3.1 Snubber circuit

According to Rashid (2004:154) transistors require certain turn-ON and turn-OFF times. Therefore, a snubber circuit is added to a transistor to slow the rise in drain voltage and the power dissipated by the transistor is reduced. The capacitor *C3* holds V_{DS} low during current turn-OFF and is calculated as

$$C3 = \frac{I_D \times t_f}{V_{DS}} = \frac{1.086 \times 579.319}{10} = 62.9 \text{ nF} \qquad (25)$$

Where:

I_D ≡ drain current in A

t_f ≡ rise time in ns

V_{DS} ≡ drain-to-source voltage in V

The matching resistor *R7* was chosen to discharge *C3* in less than the minimum ON-time t_{ON}. For a discharge time of one-third, the switching period T_s is usually adequate.

$$R7 = \frac{1}{3f_S C3} = \frac{1}{3\left(100\times10^{3}\times62.9\times10^{-9}\right)} = 52.9\ \Omega \qquad (26)$$

Therefore, a 100 nF capacitor and a 68 Ω resistor were chosen for this purpose.

3.4 Test control circuit

The control IC used for testing was a PWM UC3825 IC. The PSIM and SIMetrix5.6 simulation software packages allow for a UC3825N PWM IC controller to be evaluated as shown with the circuitry in Figure 40.

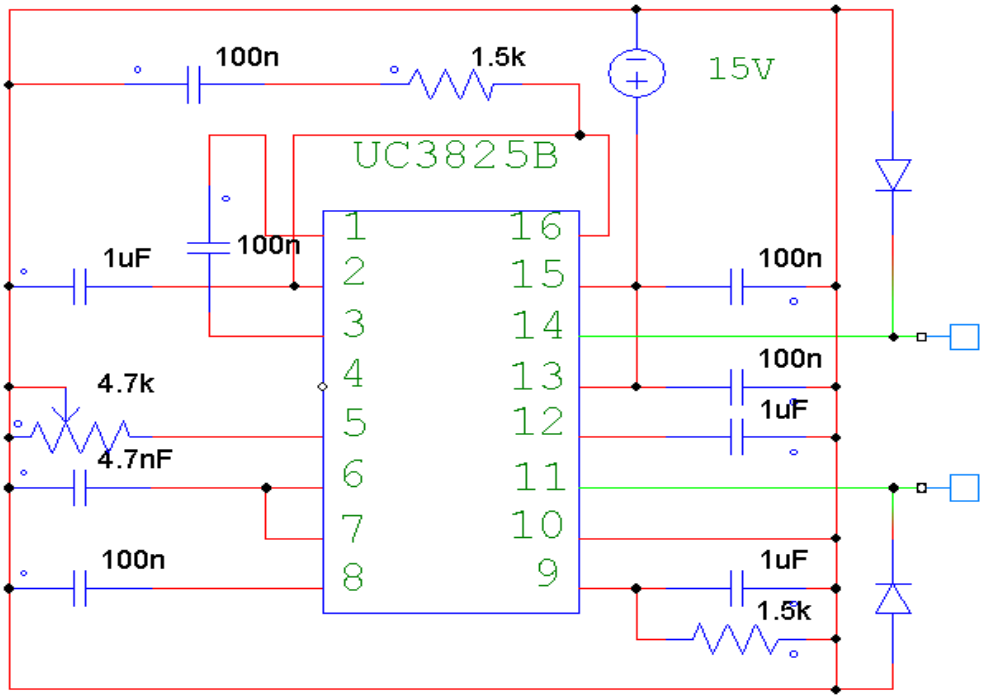

Figure 40: Simulation model for control circuit

These packages were used as the simulation tools and the main aim was to see if the module would switch up to 100 kHz. Using these packages, the module was modeled and various simulations done to evaluate the controller action. The control circuit outputs two signals of amplitude 5 V at 100 kHz. For simplicity reasons, this figure shows the model used for control circuitry and all the components used were all available in the laboratory.

3.4 1 Test control simulation results

Figures 41 and Figure 42 both present the simulations results recorded. As can be seen in Figure 41 both the signals are 180 ° out of phase and they have a dead time which can be adjusted by varying the capacitance at pin 6 to suit the switch requirements (Jalakas *et al.* 2009:438). This is also compared with Figure 42 simulation results obtained at the same voltage and same frequency.

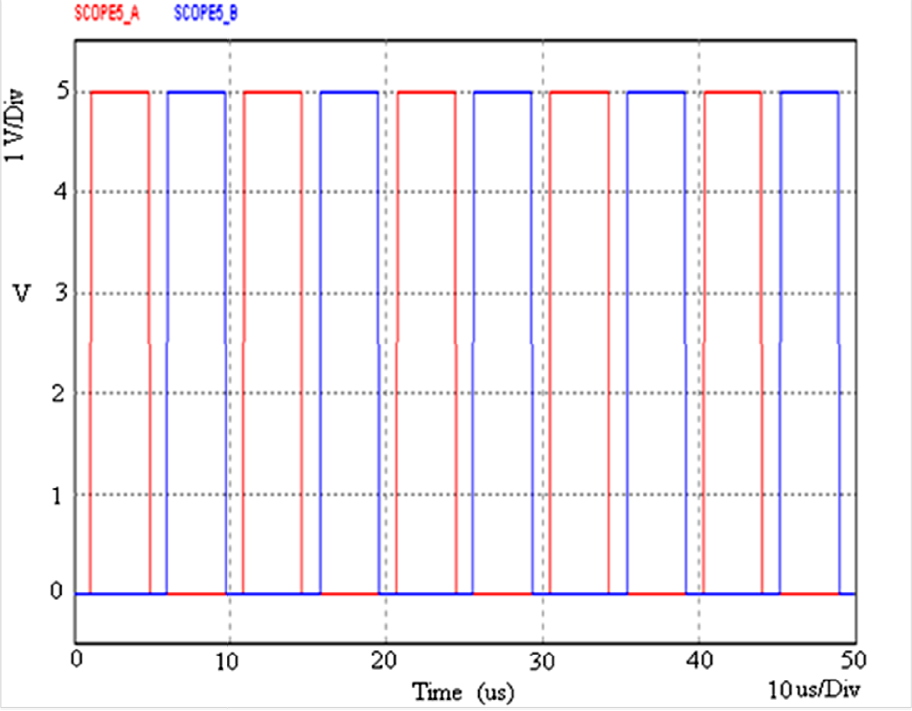

Figure 41: PSIM Simulation results of control with dead time

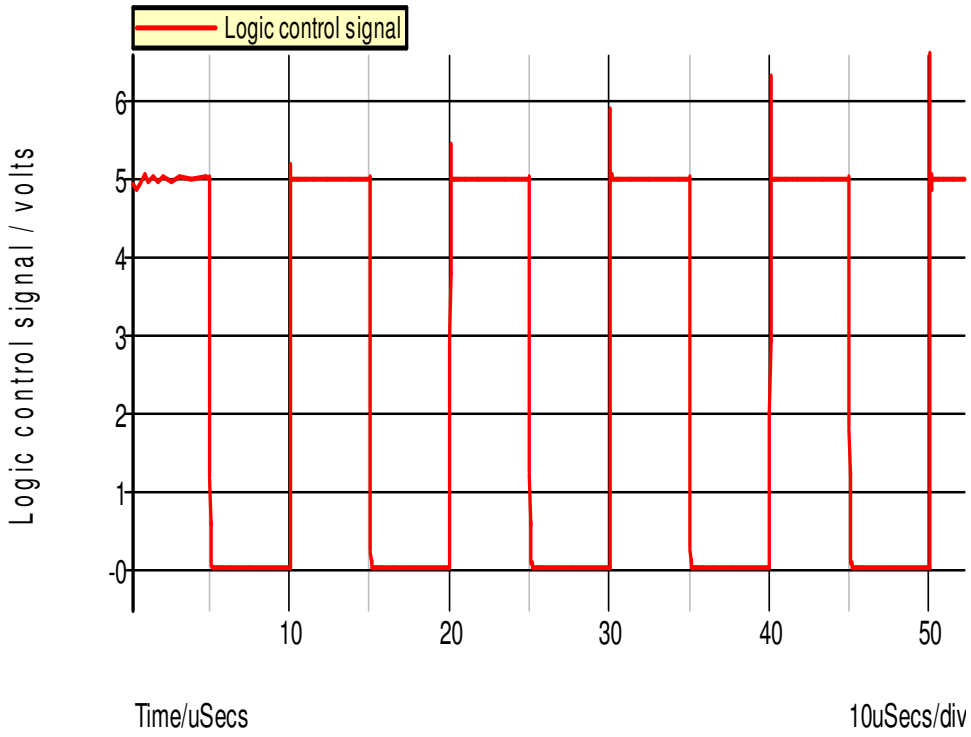

Figure 42: SIMetrix simulation results of control model

As it can be seen from the simulation graphs of Figures 41 and 42, most control ICs just output only a 5 V logic signal which is not enough to drive a MOSFET and again MOSFETs do not accept logic signals. Therefore, a gate-drive circuit was designed which will change this voltage into the required voltage level required by MOSFET (Khan 2007:546).

3.5 Simulating the gate-drive circuit

The effect of the complementary totem-pole on the gate of a high-power MOSFET was also investigated by means of simulations. From the simulation model in Figure 43 and measuring at the gate-to-emitter for IGBT or gate-to-source for MOSFET, it shows that the control voltage can swing between the positive and negative voltages (+15 V and -15 V) at a frequency of 100 kHz and this is presented in the simulation graph in Figure 44.

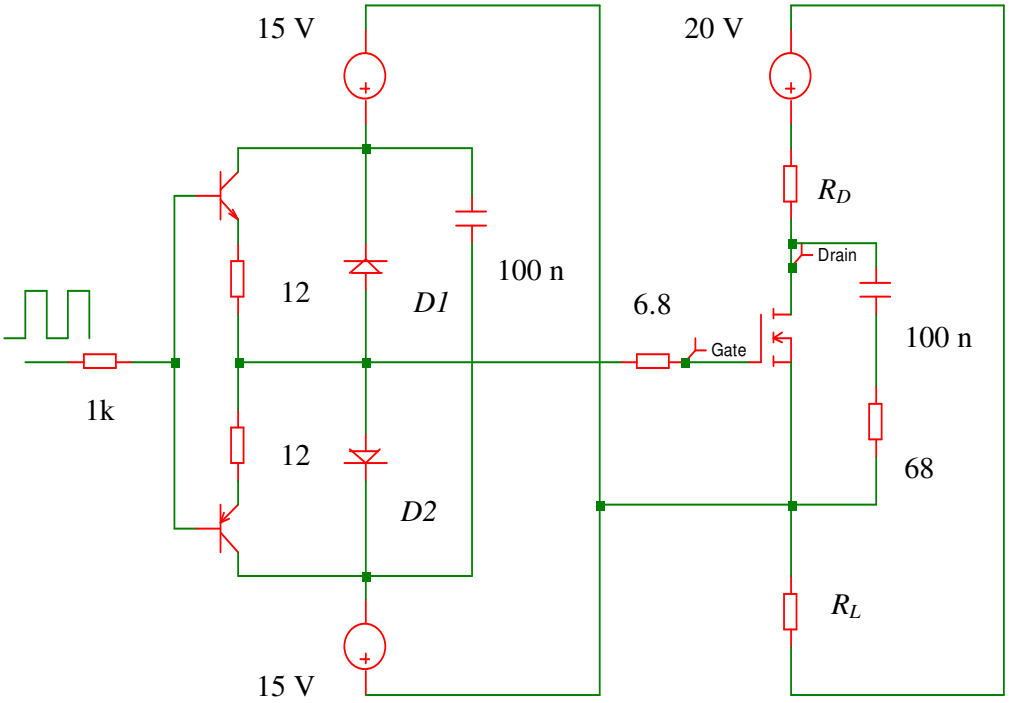

Figure 43: Simulation model of the complementary totem-pole gate driver

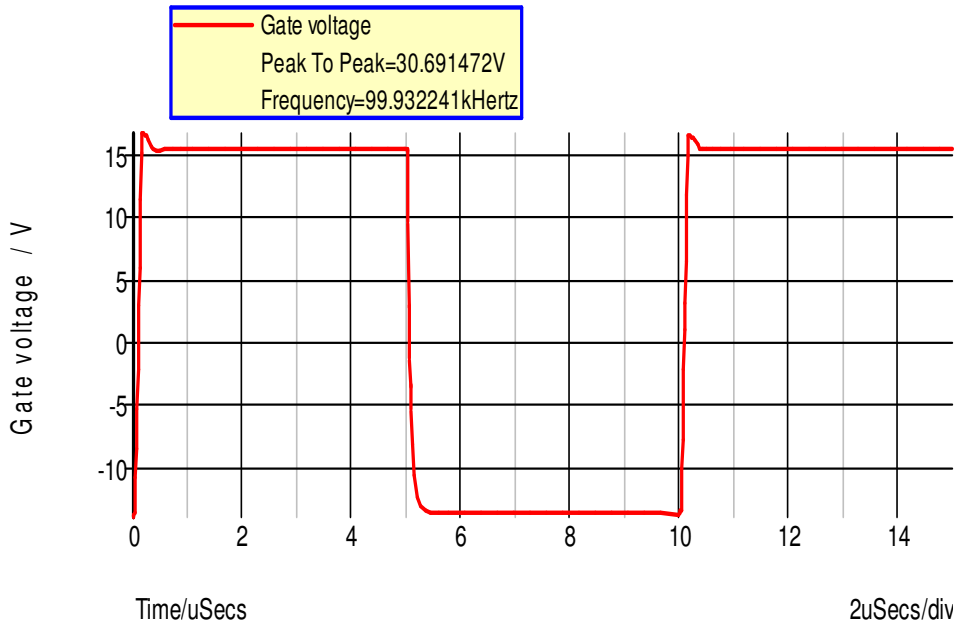

Figure 44: Gate-to-source voltage swing between + 15 V and – 15 V

As far as driving an IGBT is concerned, it resembles a MOSFET and hence all turn-ON and turn-OFF phenomena, diagrams and driver circuits designed for driving a MOSFET apply equally well to an IGBT (Mohan *et al*. 2003:636).

The supply voltage was initially set to 20 V. The input signal to the complementary emitter stage was a 100 kHz 15 V square wave. A 50% duty cycle was utilised with the total time period being 10 µs. Figure 45 below shows the simulation results where the red trace represents the gate signal to the MOSFET gate while the green trace represents the drain voltage. The gate signal of ± 15 V supplied by the drive circuit, successfully switches the 20 V drain supply that is across the MOSFET.

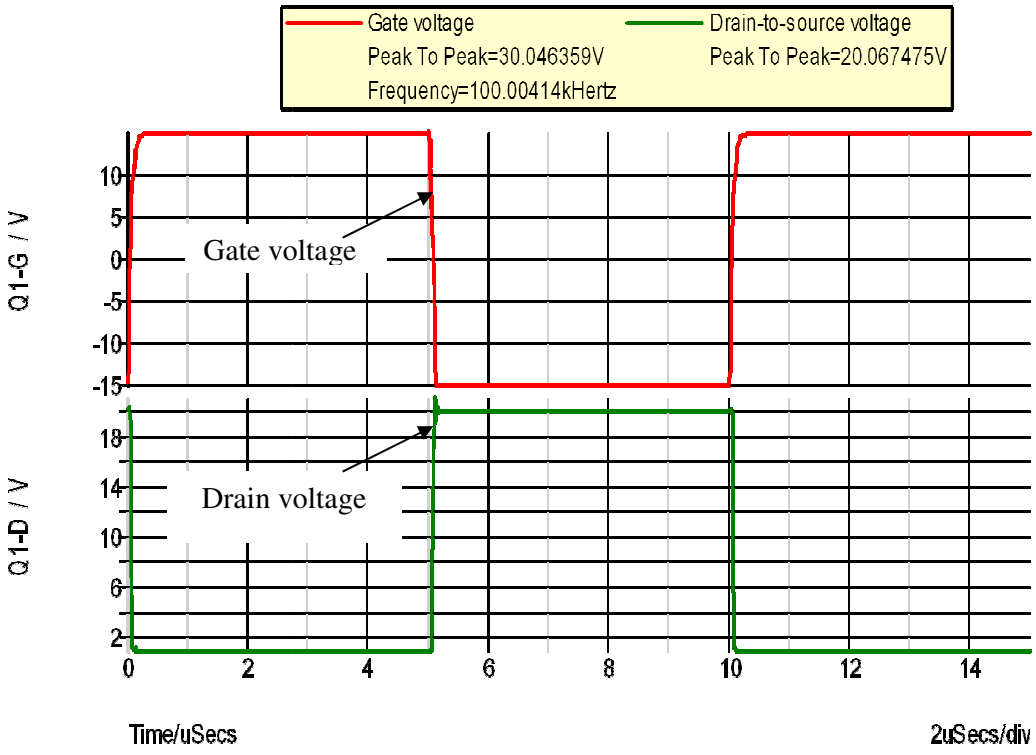

Figure 45: Gate voltage and drain output voltage

From the resulting period of 10 µs, it can be clearly seen that the frequency of operation is 100 kHz as was initially desired.

3.6 Design of DC-DC buck converter

A buck converter was analysed mathematically with the values listed in Table 2. Mathematical analyses of the converter were done with the assumption that the converter is in its steady-state and the components were lossless and could not dissipate power (Erickson & Maksimovic 2001:18).

Table 2: Buck converter specifications

Input voltage (V_i)	20 V
Output voltage (V_o)	10 V (±10)
Output current (I_o)	2 A
Operating Frequency (f)	100 kHz

According to Janse van Rensburg (2012:108) with the specifications listed in Table 2, the converter can be mathematically analysed as follows:

$$T = \frac{1}{f} = \left(\frac{1}{100\times10^3}\right) = 10\ \mu s \tag{27}$$

$$D = \frac{t_{on}}{T} = \frac{V_o}{V_i} = \left(\frac{10}{20}\right) = 0.5 \tag{28}$$

The ripple current ΔI was calculated by equation 29 which is 10% of the output current (I_o).

$$\Delta I = \left(I_o \times \frac{10}{100}\right) = \left(2\times\frac{10}{100}\right) = 0.2\ \text{A} \tag{29}$$

The inductance L that was required to maintain the converter was then calculated as:

$$L = \left(\frac{V_o[1-D]}{\Delta I \times f}\right) = \left(\frac{10[1-0.5]}{0.2\times100\times10^3}\right) = 250\ \mu\text{H} \tag{30}$$

The current that is flowing to the load passes through the inductor. Thus, the average inductor current (I_{ave}) which is the area under the current curve for one cycle and it is equal to the average load current (Kazimierczuk 2008:26). The load resistor R_{Load} can be calculated from the output voltage (V_o) and the average current. This is the load that has to be used in the simulation and the prototype.

$$I_{ave} = \frac{I_p}{2} = \left(\frac{200\times10^{-3}}{2}\right) = 0.1 \text{ A} \tag{31}$$

$$R_{Load} = \frac{V_o}{I_{ave}} = \left(\frac{10}{0.1}\right) = 100\,\Omega \tag{32}$$

After analysing the converter mathematically, a simulation model for the buck converter was constructed as shown in Figure 46.

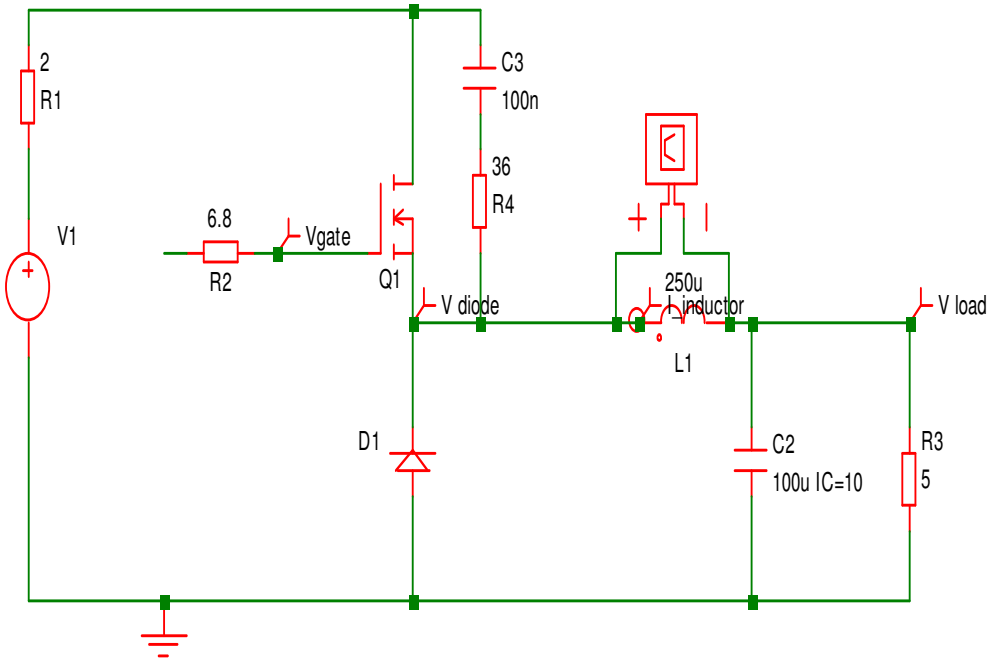

Figure 46: Simulation model of a buck converter

All the calculations done on the buck converter topology were also proven by simulation graphs which formed a platform of what should be expected with the actual model. The following section is about the simulations done on the model of a buck converter with values obtained from the mathematical calculations.

3.6.1 Buck converter simulations

Figure 47 presents the gate voltage when the converter is switched ON and Figure 48 the voltage measured at the diode (V_{diode}) as shown in the simulation model. Figures 49, 50 and 51 presented the voltage across the inductor ($V_{inductor}$), the current ($I_{\_inductor}$) that is flowing through the inductor and the voltage (V_{load}) measured across the load respectively.

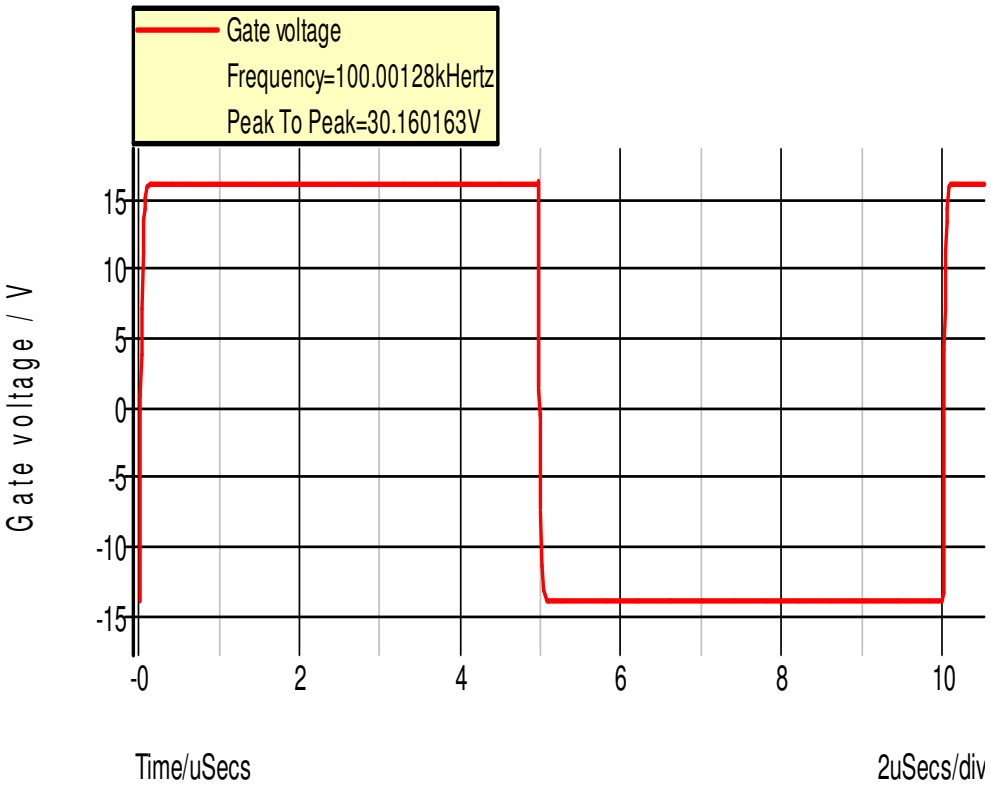

Figure 47: Gate voltage into the MOSFET

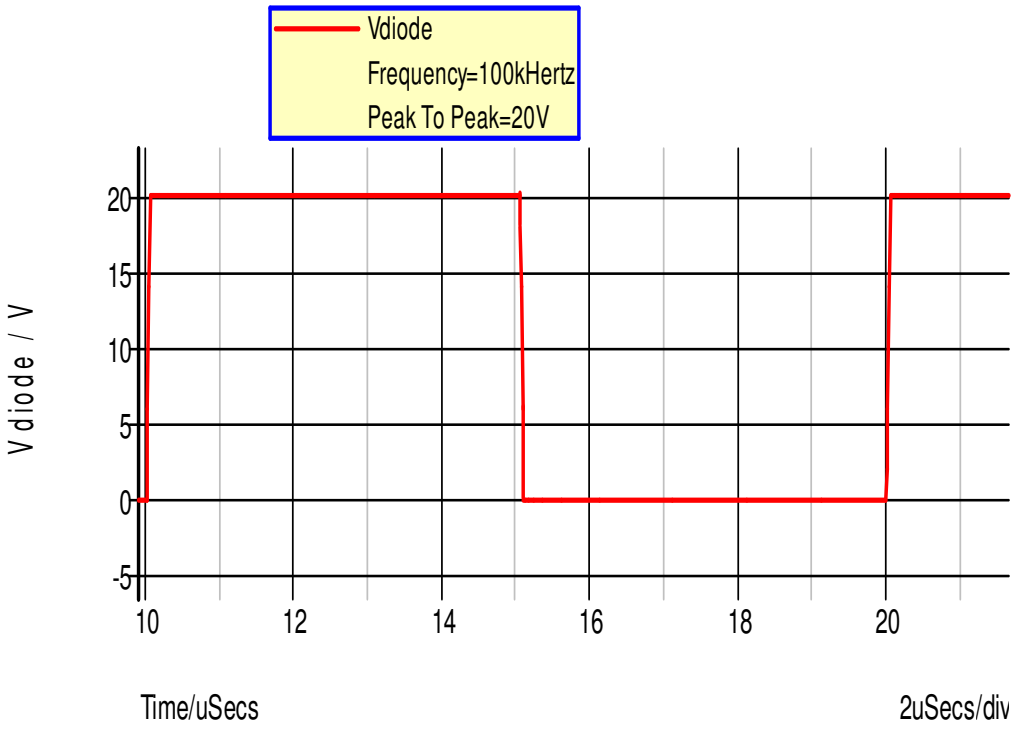

Figure 48: Diode voltage in a buck converter

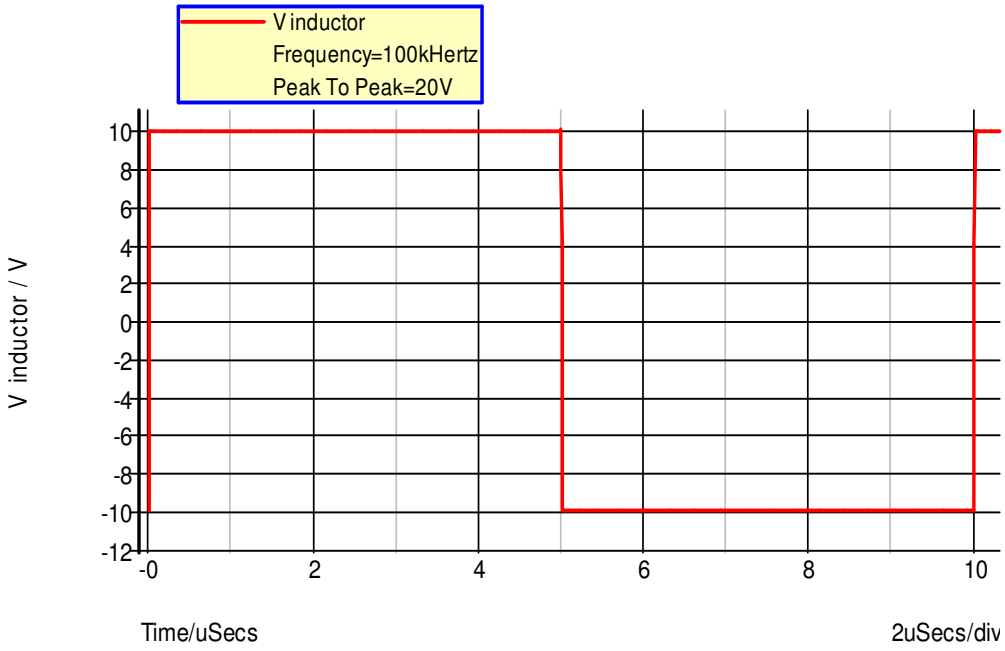

Figure 49: Inductor voltage in a buck converter

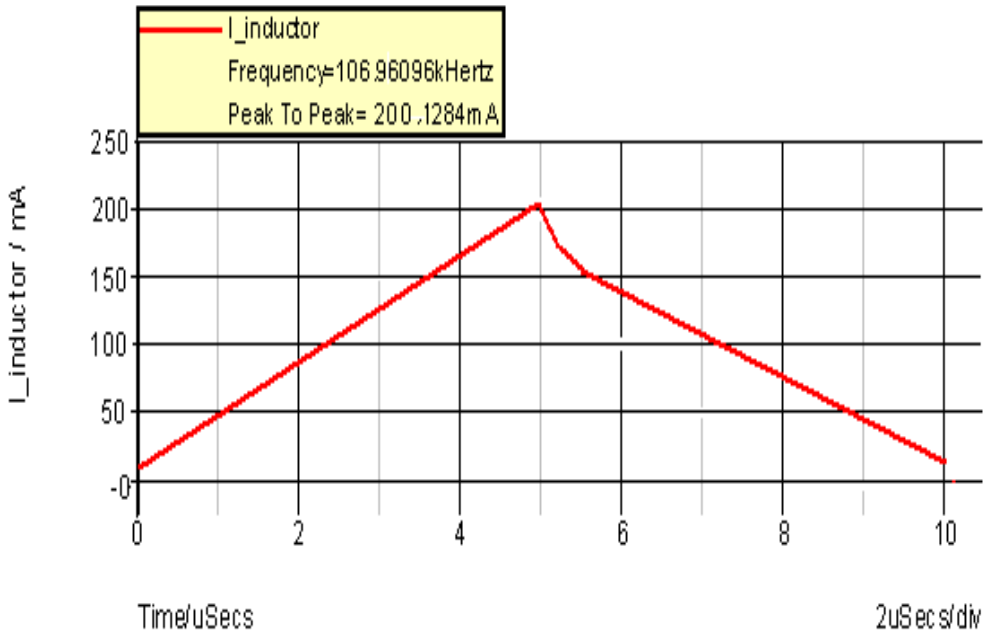

Figure 50: Inductor current

Figure 51 shows the step response of the output voltage. The output voltage took about 0.25 µs to finally reach its steady-state value of 10 V.

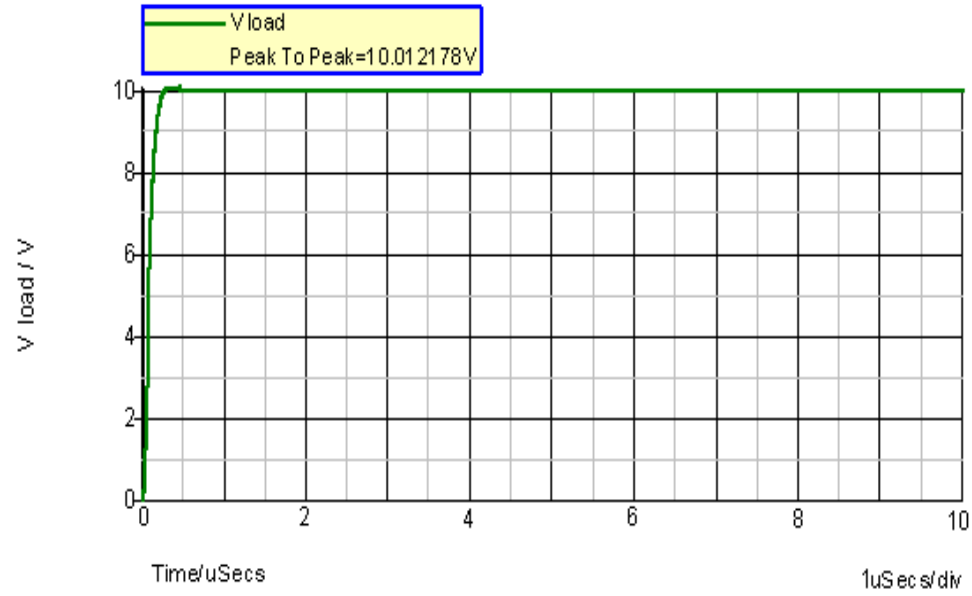

Figure 51: Output voltage in a buck converter

The difference in the mathematical and simulation results is extremely small and thus, the results can be regarded as the same. Based on mathematical and simulation results, a buck converter circuit was identified and constructed with the consideration to find the most suitable components.

3.6.2 Inductor design

The E-core type ETD/34/N87 which is recommended for power applications in the frequency range up to 500 kHz was used as it is the material available in the lab. According to Janse van Rensburg (2012:109) the air gap is first determined by

$$\frac{1}{2}\left(LI^2{}_{\max}\right) = \frac{B^2{}_{\max}}{2\mu_0} gA_c \tag{33}$$

Where:

L ≡ inductance of the conductor in μH
I ≡ current flowing through the conductor in A
B ≡ flux density in Tesla
A_c ≡ cross sectional area of the limb mm^2
g ≡ air gap between the limbs in mm

The energy stored in the gap (g) is given by the left side of the equation:

$$W = \frac{1}{2}\left(LI^2{}_{\max}\right) = \frac{1}{2}\left(250\times10^{-6}\right)(2)^2 = 500\times10^{-6} \text{ J} \tag{34}$$

In accordance with IEC Standard 1185, the ETD/34/N87 core with a centre limb has a diameter of 11 mm and the cross sectional area of the limb can be calculated as

$$A_c = \pi\times\left(\frac{d}{2}\right)^2 = \pi\times\left(\frac{11}{2}\right)^2 = 30.25 \qquad \text{mm}^2 \tag{35}$$

Where:

$d \equiv$ diameter of the limb

From equation 33 it can be seen that:

$$gA_c = \frac{2\mu_0 W}{B^2_{\max}} = \frac{2\times 4\pi\times 10^{-7}\times 500\times 10^{-6}}{(0.3)^2} = 13\times 10^{-9}\ \text{m}^3$$

$$g = \frac{13998\times 10^{-9}}{30.25\times 10^{-6}} = 0.46\ \text{mm} \tag{36}$$

The air gap (g) is found to be approximately 0.5 mm which is in the middle limb as illustrated in Figure 52. ETD/34/N87 core type with 0.5 mm gap was chosen for this purpose. From the datasheet the A_L value for N87 is 2600. And the number of turns N can be calculated as follows:

$$N = 1000\sqrt{\left(\frac{0.250}{A_L}\right)} = 1000\sqrt{\left(\frac{0.250}{2600}\right)} = 10\ \text{turns} \tag{37}$$

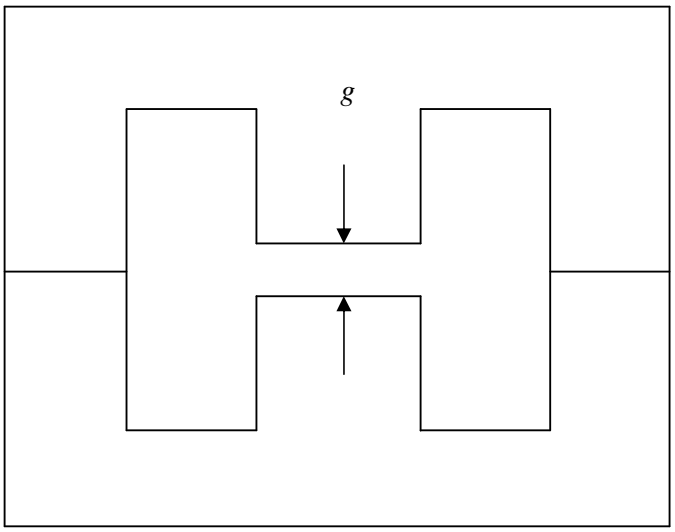

Figure 52: Air gap in an E-core

An inductor shown in Figure 53 was then constructed and the measurements were taken with the BK PRECISION 889A bench LCR/ESR meter and it read 261 μH, 2 Ω and 81.8 as the quality factor of the inductor.

Both the calculated and measured values were compared and the error percentage was calculated as follows:

$$\% \ error \ = \left(\frac{261 \ - \ 250}{250} \right) \times 100\% \ = \ 4\,\% \tag{38}$$

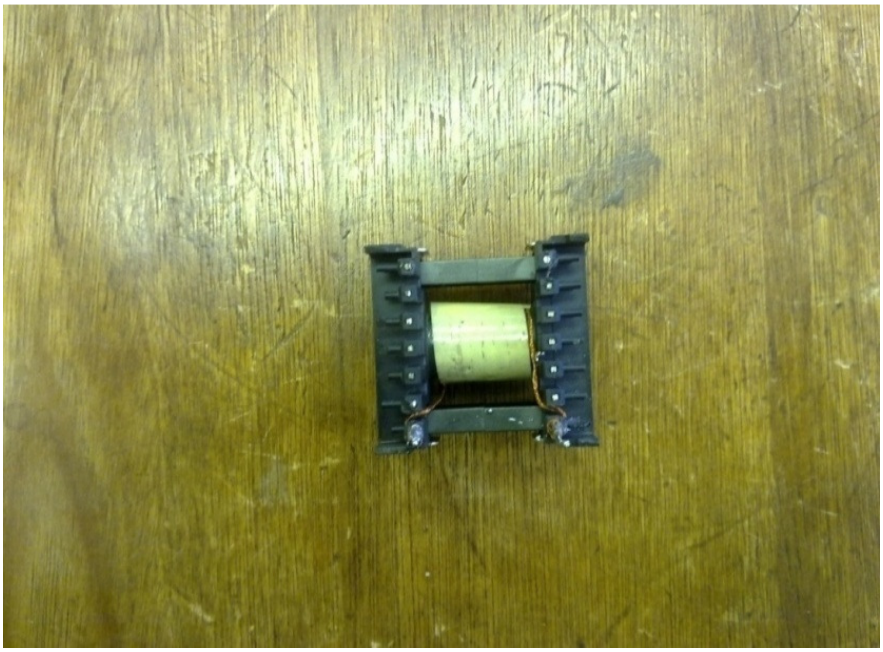

Figure 53: An inductor constructed with Litz wire

Equations 39 and 40 were used to calculate the quality factor of the inductor and the error percentage on the quality factor.

$$Q \ = \left(\frac{2\pi fL}{R} \right) \ = \left(\frac{2 \times \pi \times \left(100 \times 10^{3} \right) \times \left(261 \times 10^{-6} \right)}{2} \right) \ = \ 81.99 \tag{39}$$

$$\% \ error \ = \ \left(\frac{81.99 \ - \ 81.8}{81.8} \right) \times 100 \ \% \ = \ 0.23 \, \% \qquad (40)$$

3.7 Design of a half-bridge converter

In this design two 470 µF/63 V capacitors were used to create the midpoint voltage of the half-bridge as shown in Figure 54. In this way the parasitic inductance of the loops formed by these capacitors with the switches and the transformer primary winding, can be minimised and also the discharge energy during faults is reduced (Rossetto & Spiazzi 1997:984). These capacitors were selected based on equivalent series resistance (ESR), ripple current, cost and availability (McLyman 1997(a):984). A 2 µF/250 V_{AC} capacitor was used as DC blocking capacitor and is also used to keep the midpoint voltage steady.

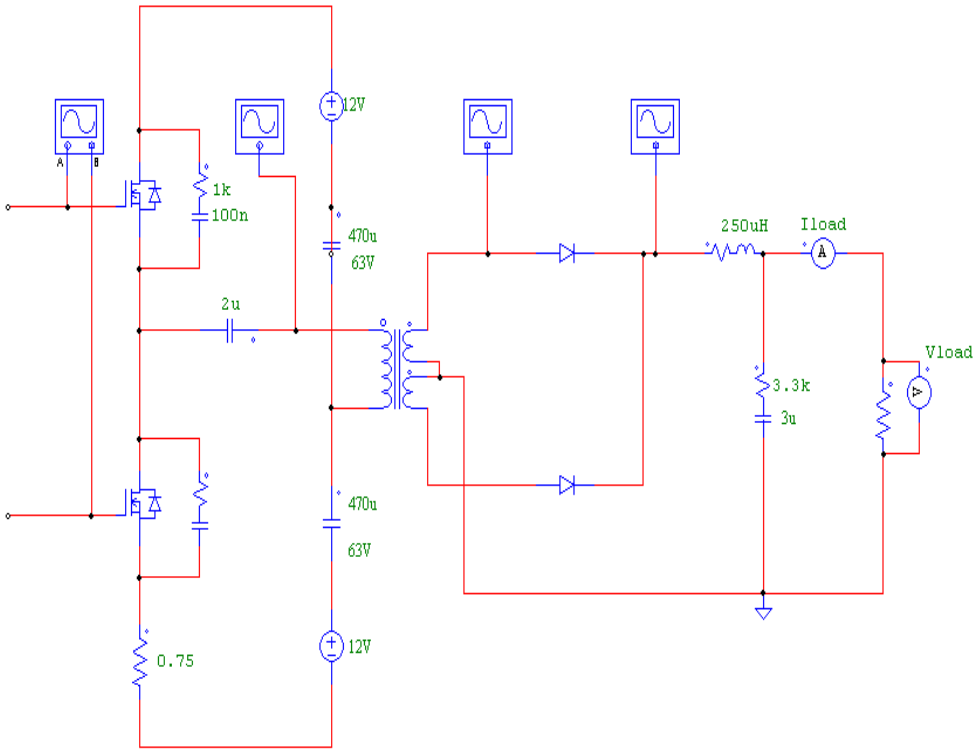

Figure 54: Simulation model of a half-bridge converter

A half-bridge converter was built, with the following target specifications in Table 3:

Table 3: Half-bridge converter specifications

Input voltage (V_i)	10-30 V (nominal 24)
Output voltage (V_o)	6 V±5%
Efficiency	>96%
Transformer turns ratio	1:2
Frequency (f)	100 kHz
Maximum duty ratio	0.5
Operating flux density	0.2 T
Diode voltage drop (V_d)	1 V
Output current (I_o)	10 A

In this research the specifications and the mathematical model were intended to give true values or more accurate values than those that would be obtained from the prototype.

3.7.1 Half-bridge mathematical calculations

According to Lee (1993:126) when the converter is switched ON, the primary voltage of the transformer becomes half the input voltage and can be calculated as shown in equation (41). The secondary voltage and output voltage can also be calculated as shown in equations (42) and (43) respectively.

$$v_p = \frac{1}{2}V_{in} = \frac{24}{2} = 12 \text{ V} \tag{41}$$

$$v_{s1} = \frac{1}{2}V_{in}\frac{N_s}{N_p} = \frac{1}{2}\times 24 \times \frac{1}{2} = 6 \text{ V} \tag{42}$$

$$V_o = DV_{in}\frac{N_s}{N_p} = \frac{1}{2} \times 24 \times \frac{1}{2} = 6 \text{ V} \quad (43)$$

The secondary output power (P_o) and total input power (P_{in}) were calculated in equations (44) and (45) respectively

$$P_o = I_o \times (V_o + V_d) = 10(6+1) = 70 \text{ W} \quad (44)$$

$$P_{in} = \frac{P_o}{\eta} = \frac{70}{0.96} = 72.5 \text{ W} \quad (45)$$

From the specifications, the Power Stage designer tool was used to simulate this idea. This computer-aided software from Texas Instruments is used in the design of converters. Annexure G provides the screenshot of the Power Stage designer tool which proposes the values of inductor and transformer which need to be used. The computer-aided design confirmed the calculations and even provided the inductance of the output filter that could be used to achieve the desired current ripple at all input voltages.

3.7.2 High-frequency transformer design

The high-frequency (HF) transformer is an integral part of bridge converters (McLyman 1997(b):120). The design employs an ETD34/17/11 ferrite core which was developed specifically for power transformer cores used in power supplies and operates up to 100 kHz. The primary and secondary windings are made of Litz wire AWG26 in order to minimise leakage inductance and the skin effect that is prevalent in copper conductors (Sullivan 1999:283). A cross-section of the winding topology showing the primary and secondary termination is shown in Figure 55. The secondary of 5 turns is sandwiched between the two primary windings of 5 turns each to improve coupling (Schaef, & Sullivan, 2012:1012).

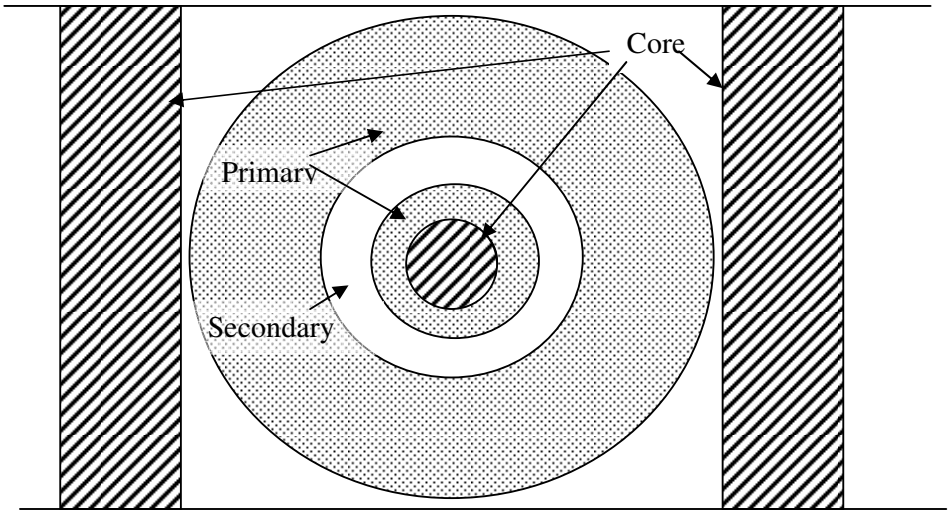

Figure 55: Cross section of a HF transformer

3.7.3 High-bridge converter simulations

The converter was also simulated and the results presented in the graphs that follow. Figure 56 presented the voltage measured at the primary side of the transformer.

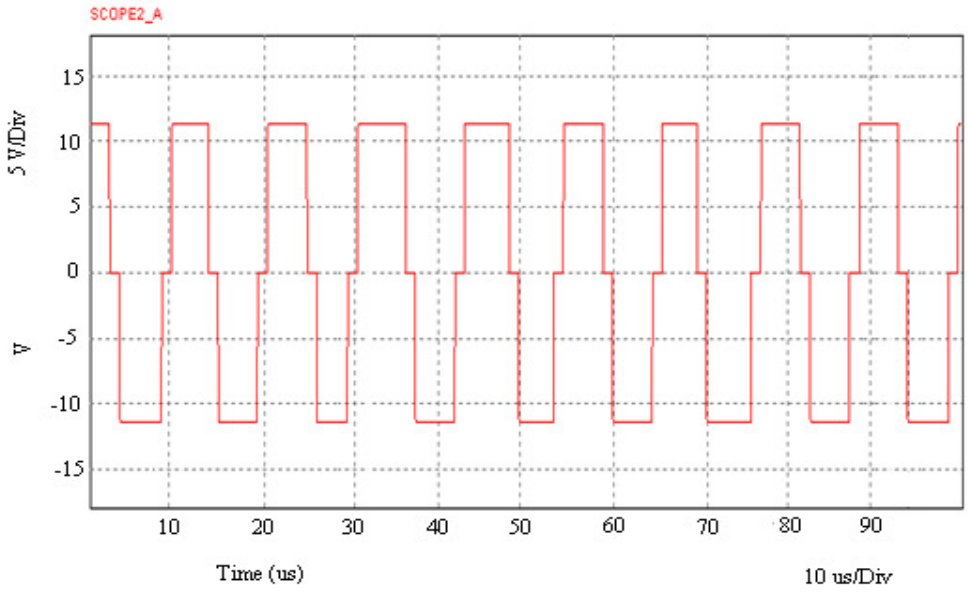

Figure 56: Voltage measured at the primary of the transformer

From the transformer primary terminal, it can be seen that transistors are switching ON alternatively. Figure 57 shows the transformer primary current, Figure 58 shows the current that is flowing through the inductor and Figure 59 shows the rectified voltage from the simulation model.

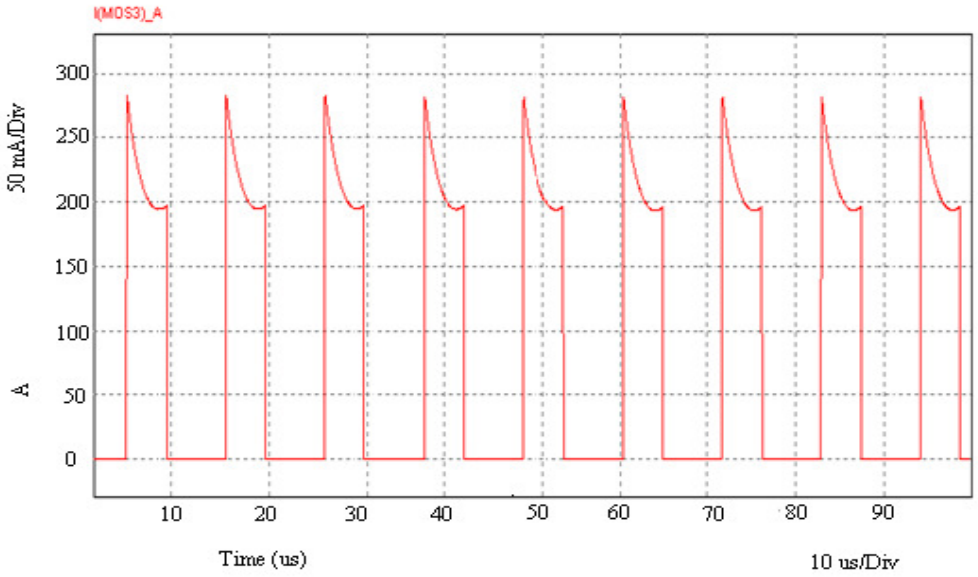

Figure 57: Transformer primary current

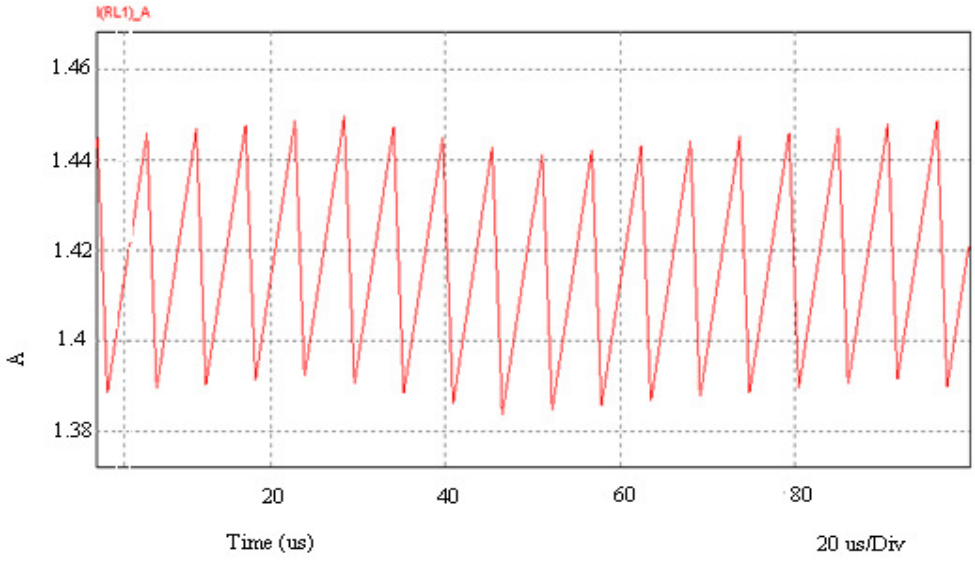

Figure 58: Inductor current

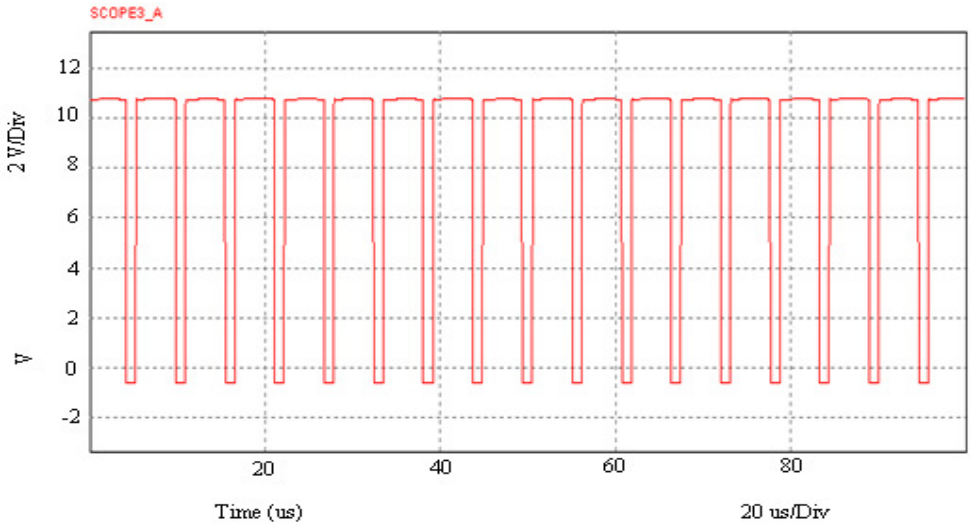

Figure 59: Rectified voltage

3.8 AC chopper with UC3825N as the controller

The whole idea here is to vary and control the rms voltage on AC systems such as motor drives, lamps and the rest. In this research, to do just that the AC signal has to be switched ON and OFF repetitively. Equal time ratio control (ETRC) was selected as the specific mode of control for the control of the AC chopper.

3.8.1 Mathematical calculation of the output voltage

Based on equation 24 in the literature study in Chapter 2 (Mazda 1997:169), for a 20% ratio the output voltage is calculated and found to be 20 V. The calculated results are tabulated in Table 4 for different duty cycles.

Both the calculated results and the simulation results are used as a basis for the design consideration of the AC converter. Simulation of the circuit with UC3825N as the controller was done on SIMetrix simulation software. The simulation model is as shown in Figure 60.

Table 4: Calculated output results for different duty ratios

Duty cycle (D) in %	Calculated output voltage (v_o)
20	20
30	30
40	40
50	50
60	60
70	70

MUR820 type rectifier diodes were used because they are ultrafast, can handle up to 600 V, 8 A and have very low forward voltage and low leakage current. These rectification diodes also have an operating junction temperature of 175 °C which is suitable for power MOSFETs. The MUR820 datasheet is provided as Annexure H.

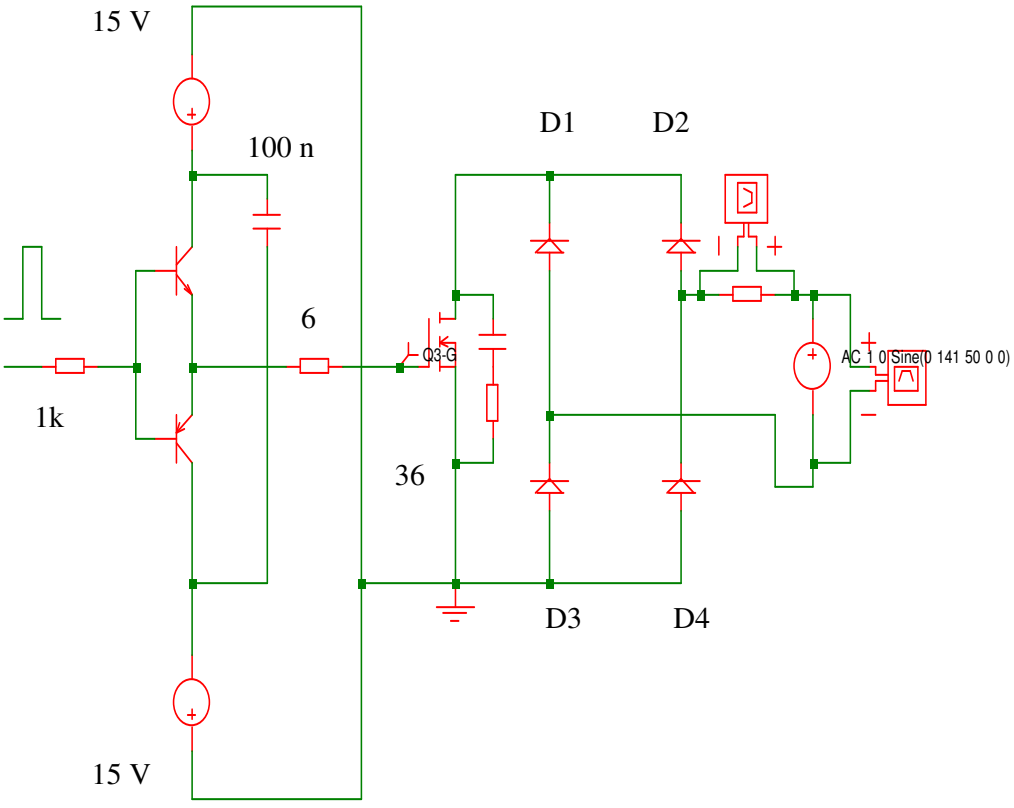

Figure 60: Simulation model of an AC chopper system in SIMetrix

3.8.2 AC converter simulation graphs

The AC supply line was modeled with a universal source of unit amplitude at 100 V rms and 50 Hz as shown in Figure 61 below. Figure 62 presented the control switching signal 1.92 kHz much higher than the fundamental utility frequency which is going to modulate the input signal (Janse van Rensburg 2005:57).

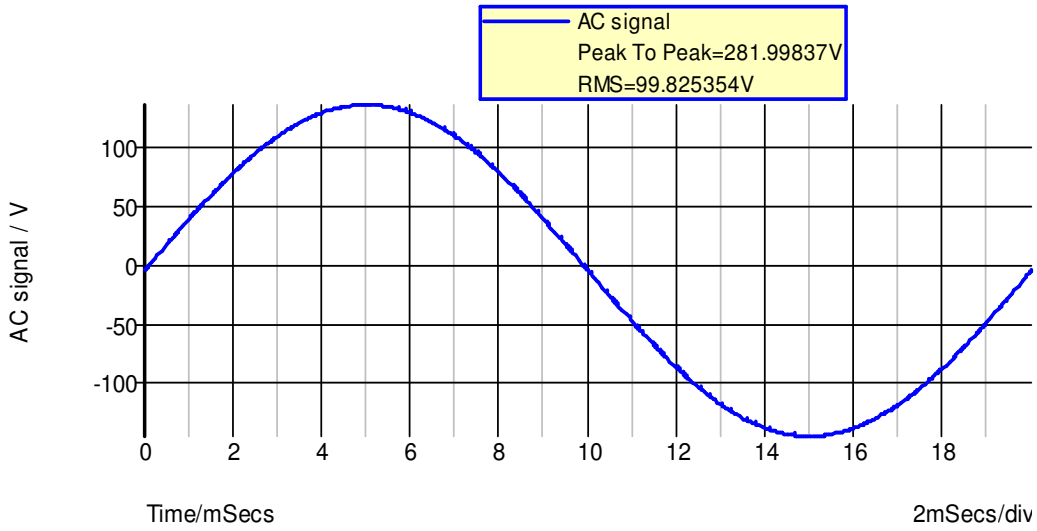

Figure 61: AC signal at 100 V/50 Hz

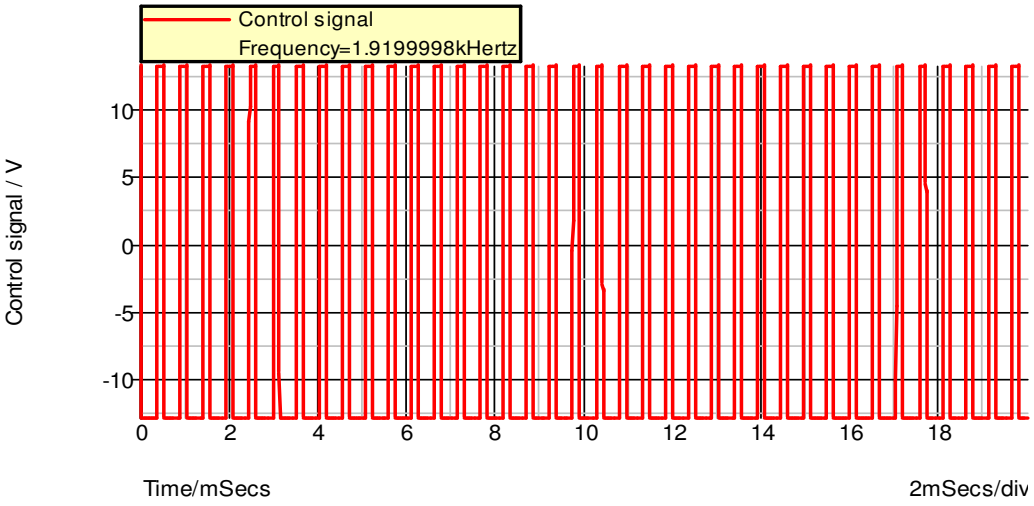

Figure 62: Control signal at 1.92 kHz

Figure 63 and Figure 64 show one cycle of the chopped voltage waveform over the load. The simulation graphs show the measured load voltage at 30% duty cycle and 70% duty cycle respectively.

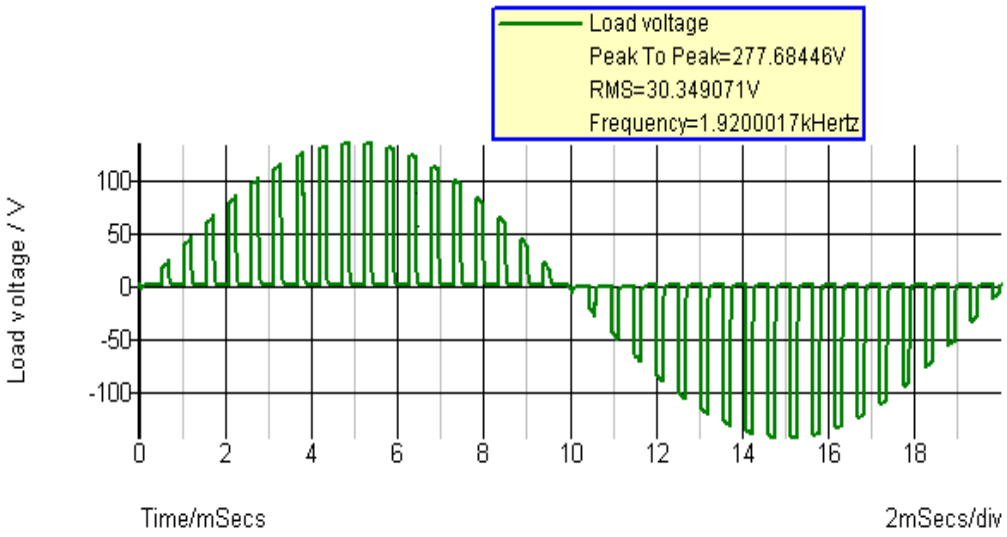

Figure 63: Simulation graph for load voltage at 1.92 kHz with 30% duty cycle

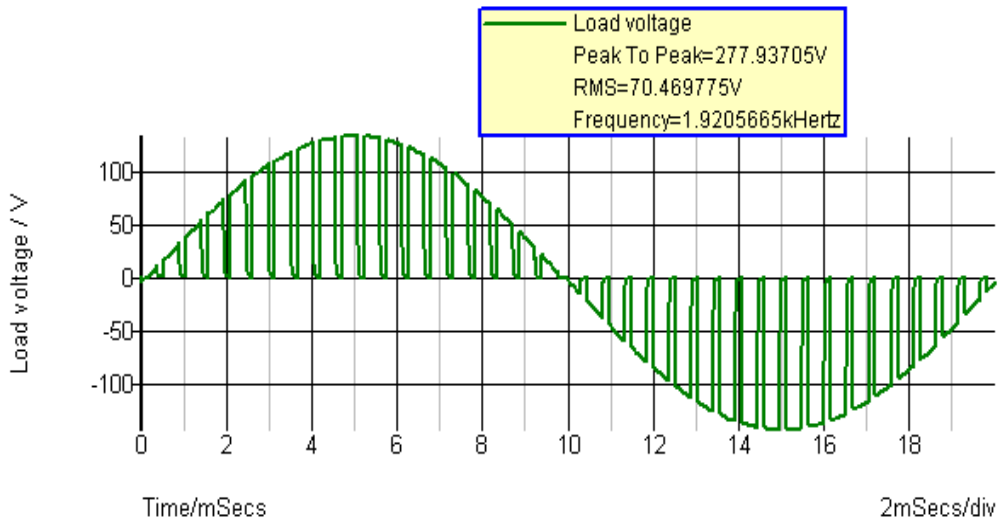

Figure 64: Simulation graph for load voltage at 1.92 kHz with 70% duty cycle

Based on the literature review presented in Chapter 2, mathematical calculations show a close correlation to the simulations performed. The switch module circuit was then designed and the PCB was manufactured using EAGLE software and machined in the fuel cell laboratory at Vaal University of Technology. The complete circuit diagram of the switch module is included as Annexure I.

3.9 PCB board manufacturing

As can be seen from Figure 65, the track widths that were selected had to be modified, based on the size of the pads to which it runs into. This was done so as to avoid too wide traces leading into a pad, because they would pull the heat away when the component is soldered to the pad and may also cause cold solder joints (Jacob 2002:88).

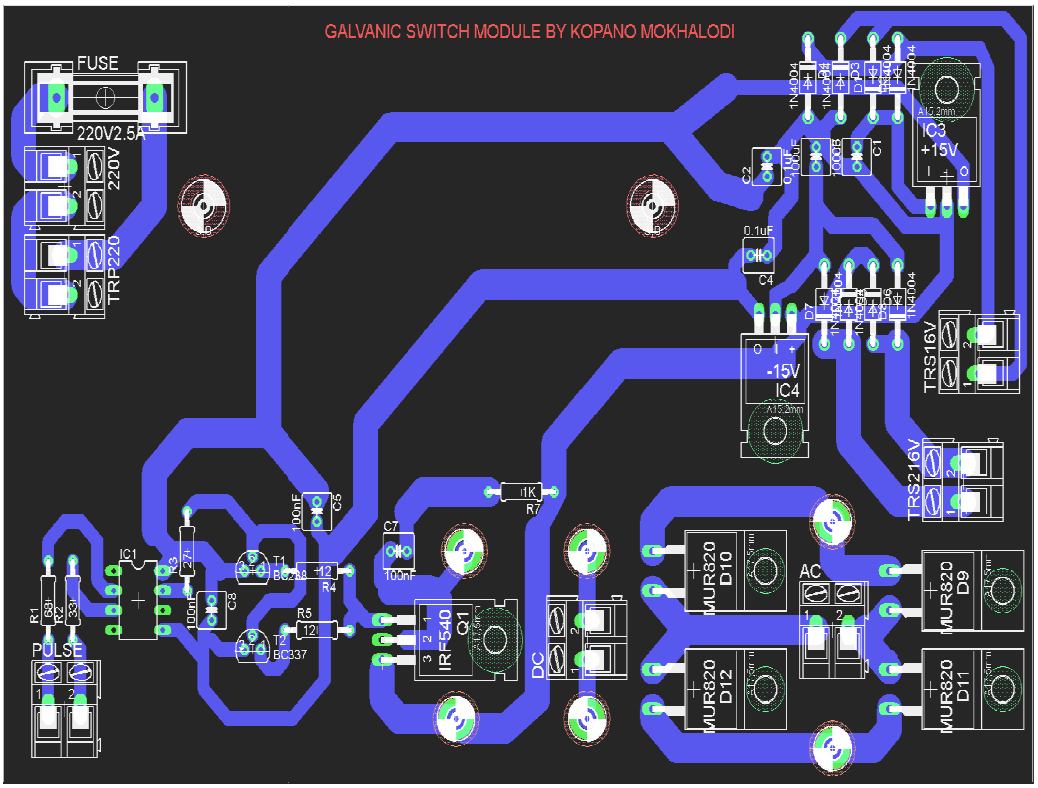

Figure 65: PCB board layout of the module in eagle software

According to Jacob (2002:88) the standard MIL-STD-275 provides two graphs that show how to determine the relationship between current, track temperature rise, copper thickness and track width. The widest traces were chosen as this would lower the resistance, resulting in a smaller voltage drop (Jones 2004:6). As with wire gauge, size determines how hot the track can get. As a general rule, for small signal tracks carrying less than 750 mA, the widths were set at 0.1" (2.54 mm) and 0.3" (8 mm) for power and ground tracks. On the PCB layout, right angles have been avoided at all cost (Jacob 2002: 89).

3.10 Completed prototype module

Figure 66 shows the prototype switch module which was built and tested in the laboratory. The individual terminals that connect to the module are labeled and indicated.

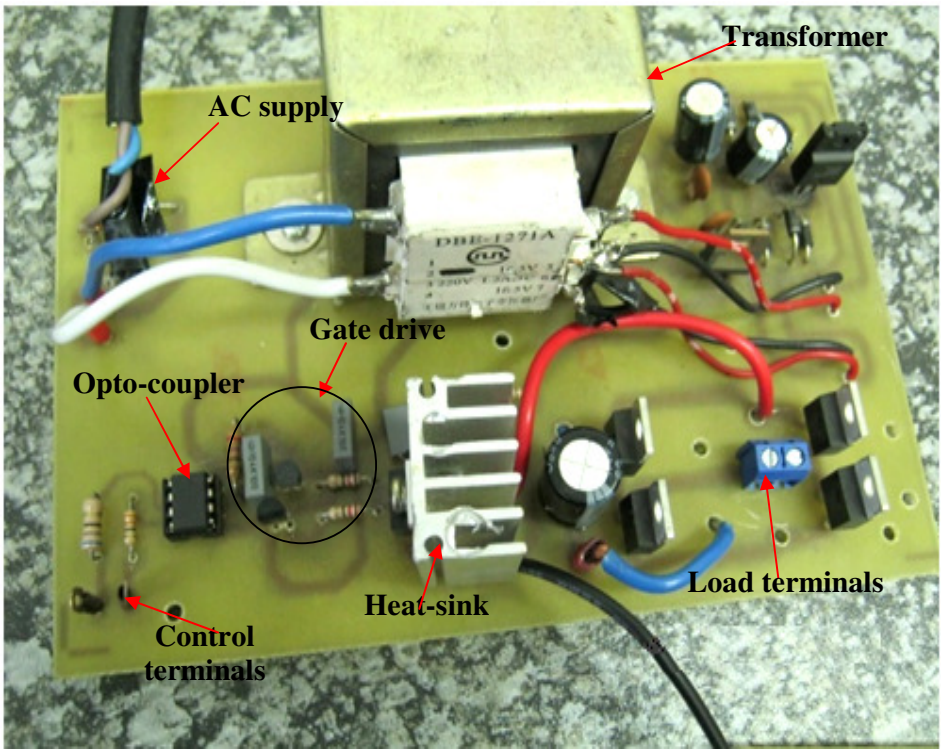

Figure 66: Prototype of the switch module

These are the control terminals, AC supply and load terminals as shown in the figure. The transformer is centre tapped in order to provide a dual supply required to the gate-drive and the opto-coupler for floating supply.

The purpose of worst-case analysis (WCA) was to ensure that the design is robust; that is, even if all the varying conditions mentioned occur in a single supply, the switch module would still operate within specifications over its lifetime (Lenk 1998:225).

3.11 Summary

This chapter covered the circuit design principles which formed a platform of what should be expected with the actual switch module. Based on mathematical and simulations results a suitable gate-drive circuit was identified with design components' specifications in consideration to find the most suitable components to be used.

Also in this chapter, mathematical calculations and the results of many simulations to illustrate the various aspects of the switch module were also presented and discussed in detail. Several simulations had to be run to ensure that the module would operate as expected in each application. These included the generation of logic control signals, the concept of level shifting and the floating of the power supply. Simulations were also run to test the module under different converter topologies to see how it would operate and analyze its behavior. Each function of the simulation was broken down into smaller blocks and explained, along with the basic control schemes. It has also been shown that the simulation results agree favourably with the mathematical models presented.

In the next chapter, the experimental hardware setup of the switch module and the converter topologies to test its application are discussed. The practical models and all the results obtained with these models are presented.

Chapter 4 Measurements and results

The previous chapter presented the actual design of the module and the results of many simulations to illustrate the various aspects of the switch module. These included the generation of logic control signals and the concept of level shifting together with the floating of the power supply. The module has also been simulated in two simulation software packages SIMetrix and PSIM. It has also been shown that the simulation results agree favourably with the mathematical models presented.

In this chapter the results obtained from the experimental switch module and the converter topologies are presented, compared and contrasted with the mathematical and simulation results. The methods followed with each topology and the results obtained for each topology are also presented.

4.1 Introduction

The main objective of this research was to develop a universal bidirectional galvanic isolated switch module which can be used to drive any MOSFET or IGBT in any position in any topology; therefore, several tests were done to establish the working electrical characteristics of the switch module. The other objective of this research project was to validate the proposed switch module under practical converter operating conditions. The actual results of the prototype module were compared with the simulation results obtained with simulation softwares and the other theoretical analyses discussed in Chapters 2 and 3. These include the control of the module, the gate drive, the power stage and the converter topology applications.

4.2 Electrical characteristics of the power switch module

The module is built up from a serial linkage of distinguishable building blocks of which the actual physical assembly may not appear so. The fundamental characterization of each block is to develop a relationship between the input and the

output and to the next block. Each block was analyzed by means of testing it independently and the results are presented by means of graphs that follow.

To analyze this switch module, the UC3825N controller was implemented to provide the required control logic signals. Figure 67 shows the evolution of the main control signals from the PWM controller. Two 180 degree out of phase output signals, with dead time, determine the right switching sequence and the delay times of the power switches.

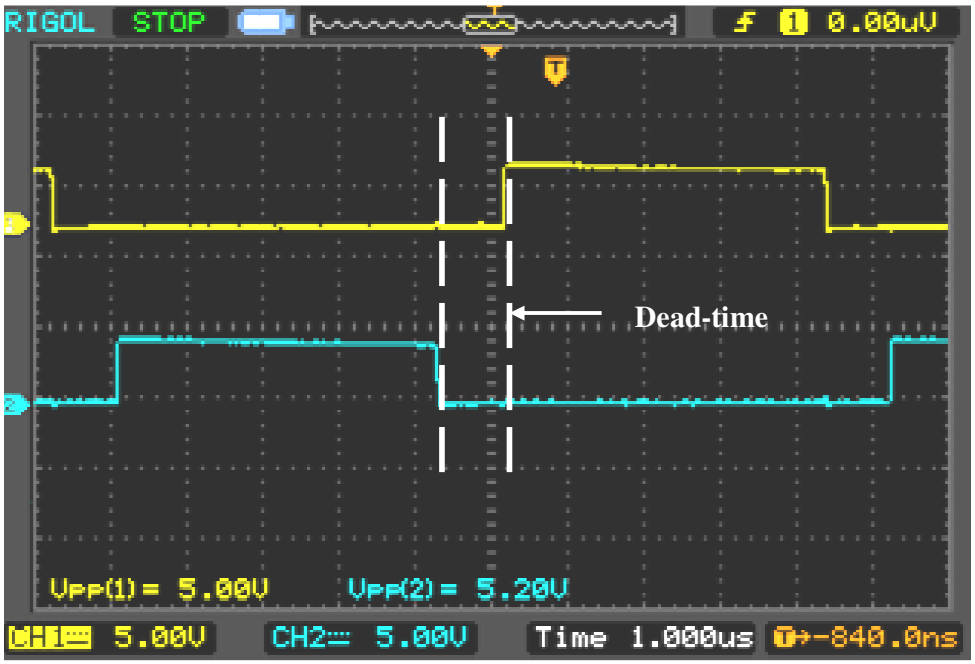

Figure 67: Main control signals from the PWM controller 0 to 5 Volts

The gate-drive circuit was also tested to prove that it provided the isolated DC floating supply for galvanic isolation required between the control and the power stage. From the experimental model's result shown in Figure 68 it is evident that the module is switching at 100 kHz and the gate-drive voltages are swinging between + 15 V and – 15 V as was demonstrated with the simulation graphs in Figure 44 in Chapter 3. Both figures are similar in frequency and amplitude. Comparing both

figures yields no real significant differences. Signal voltages, switching times and frequencies are similar for both the simulated and experimental models.

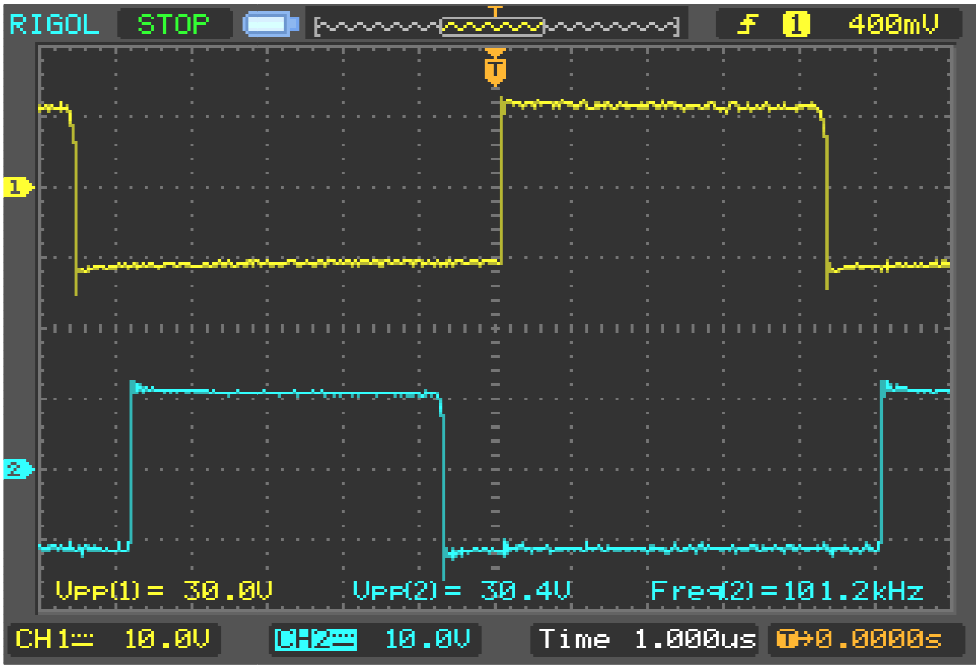

Figure 68: Gate voltages V_{GS} of both switches

The waveforms of Figure 69 and Figure 70 present the currents and voltages across the switches. They illustrate the turn-ON and the turn-OFF characteristics of the switch module when a 20 V is applied. These are the possible switching situations that can be found in power devices.

A 20 V input supply was used as the drain voltage and the gate voltage of ±15 V were also used to model the switching idea. The experimental model's results are shown in Figure 71, where the gate voltage signals and drain voltage are indicated. The experimental model's results for gate voltage and drain voltage for the MOSFET were then compared to the simulated model's results Figure 45. It was found that both Figure 45 and Figure 71 are similar in values and waveform shapes. It could be confirmed that the switch module with a ±15 V floating supply voltage could really switch a 20 V drain voltage at 100 kHz without any problems.

Figure 69: Characteristic current and voltage waveforms at turn-ON

Figure 70: Characteristic current and voltage waveforms at turn-OFF

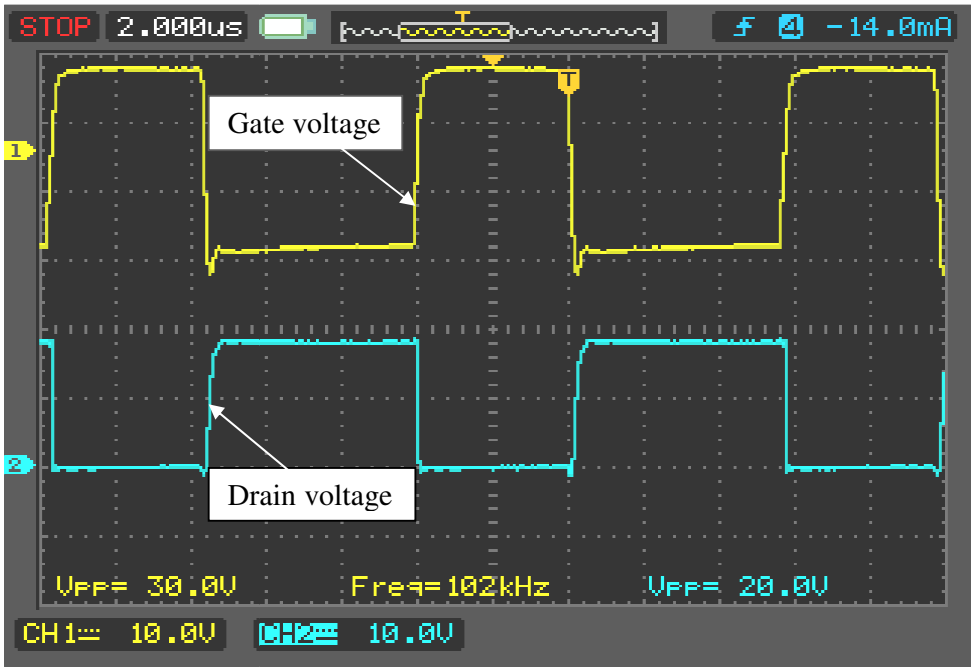

Figure 71: The gate voltage and drain output voltage signals

4.3 Application example of the switch module to converter topologies

In order to validate the proposed switch module in real operation conditions, the switch module was first tested in DC topologies. It was tested in a designed buck converter where galvanic isolation is very much important because the gate of the MOSFET is not referenced to ground making it very difficult to drive the transistor. The module was also tested in a half-bridge converter where the switching network has a totem pole arrangement of switching transistors, resulting in difficulty in driving the transistors. The module was also tested in AC converter applications to test if it would work in a bidirectional way and also to see if it would meet its required specifications.

4.3.1 Buck converter

The purpose of this test was to prove that the module could switch as the high-side transistor where it has an isolated floating driver which provides DC isolation in the

control path. The module provided a floating voltage supply for the gate drive as was initially intended. A DC power supply was used as the input voltage supply which was initially set at 20 V and a DC electronic load was used as a load. The load was set at 100 Ω as per theoretical calculations done in Chapter 3. The results and measurements were obtained by using a 100 MHz Digital Storage Oscilloscope. The experimental set-up is as shown in Figure 72.

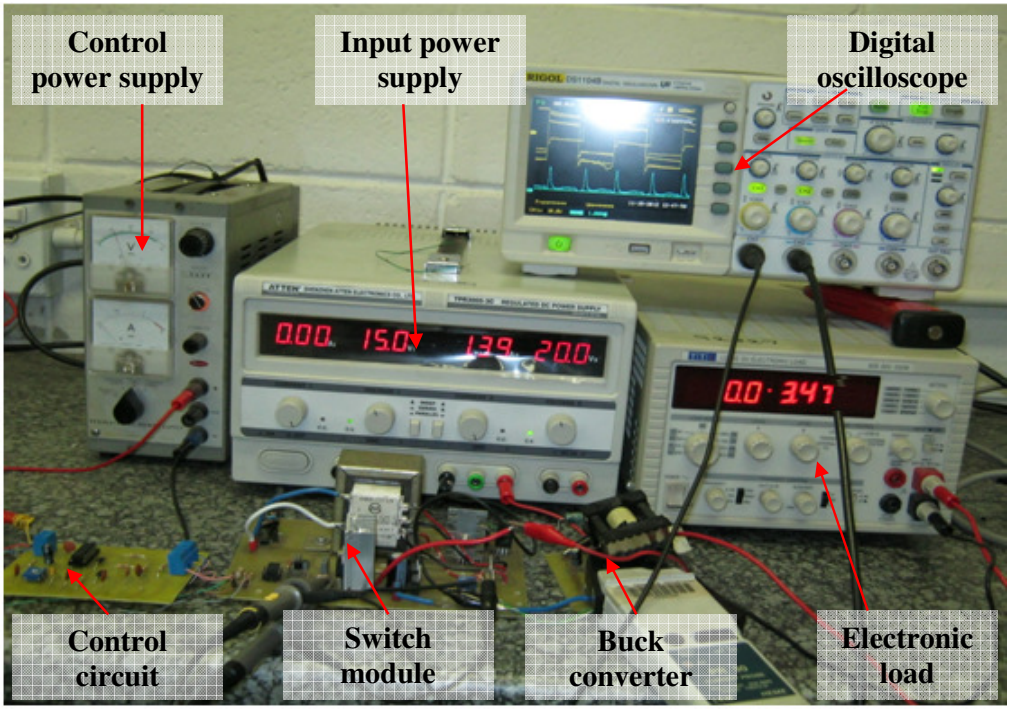

Figure 72: Experimental set-up for a buck converter

Figure 73 shows waveforms results of a buck converter design switched with this module. Channel 1 shows a 20 V chopped diode voltage when the module is switched at high frequency (100 kHz) and it can be seen that the voltage is also floating as is the aim of the module. Channel 2 shows the current through the inductor. These results are similar to the simulation results obtained in Chapter 3. It can be seen that for a 20 V input there is very small or negligible power dissipated across the transistor because the voltage across the diode is still equal the input voltage as was depicted in the theoretical analysis.

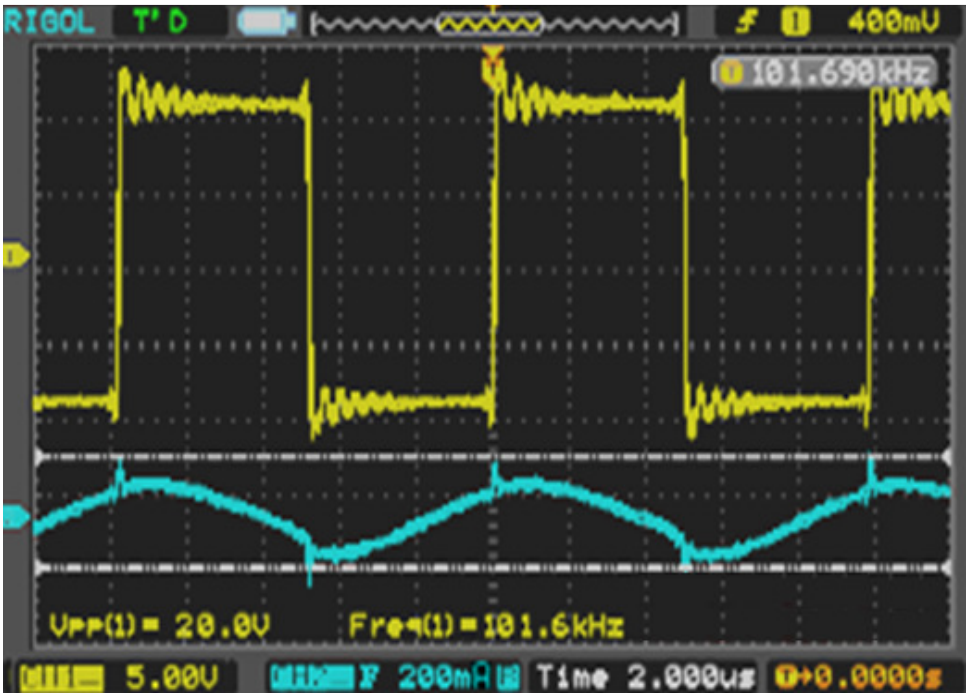

Figure 73: Voltage and current waveforms of a buck converter prototype

The output voltage in the simulation was 10 V as was mentioned in the converter specifications and 9.81 V were recorded in the prototype and the error can then be calculated as:

$$\left(\frac{10-9.8}{10}\right)\times 100\% = 2\% . \tag{46}$$

This was an acceptable error which could be due to components tolerance level.

4.3.2 Bridge converter

A half-bridge converter was constructed. The aim of this experiment was to prove the legitimacy of the switch module in half-bridge converters. In this test, both the upper and lower transistors have isolated floating drivers which provided DC isolation in the control path. The transistors were driven by non-overlapping

voltages that were out of phase by 180° to avoid the situation where both transistors were conducting at the same time.

A nominal voltage of 24 V was used as the input voltage into the bridge converter with the module supplying the gate signal. In Figure 74 traces 1 and 2 present the gate voltages of each MOSFET which clearly show the dead-time. As can be seen from the figure, when the non-conducting semiconductor switch has to be turned-ON, the appropriate conducting switch has to be previously turned-OFF. The third trace presents the voltage across the lower switch which happens to be equal to the transformer primary voltage.

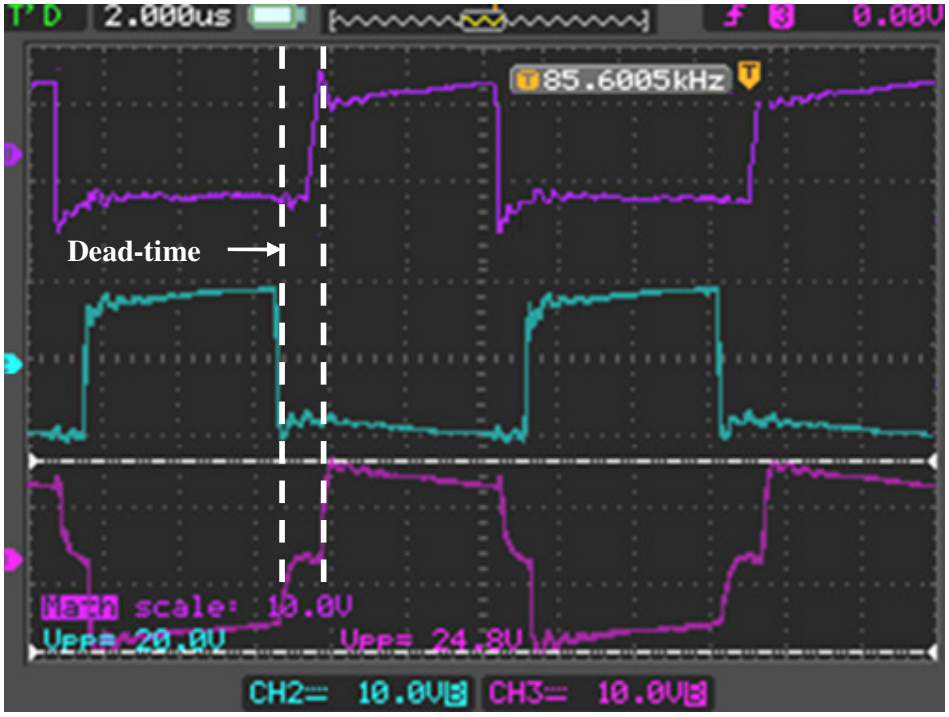

Figure 74: First and second traces: Gate voltages; bottom trace: voltage across the lower switch

From the graph it can be shown that the primary is driven in both directions meaning the transformer core is utilized more effectively. As can be seen from the graph, the input capacitors split the input voltage equally so that the primary only faces half the

input voltage when either transistor is turned ON. Both MOSFETs were switched at 85.6 kHz.

In Figure 75 the upper trace shows the voltage across the secondary terminals of the transformer. Even the secondary reflects the switching ON 7.6 V positive and OFF 7.6 V negative of transistors. The lower trace represents the transformer primary current. Both waveforms show symmetrical behaviours.

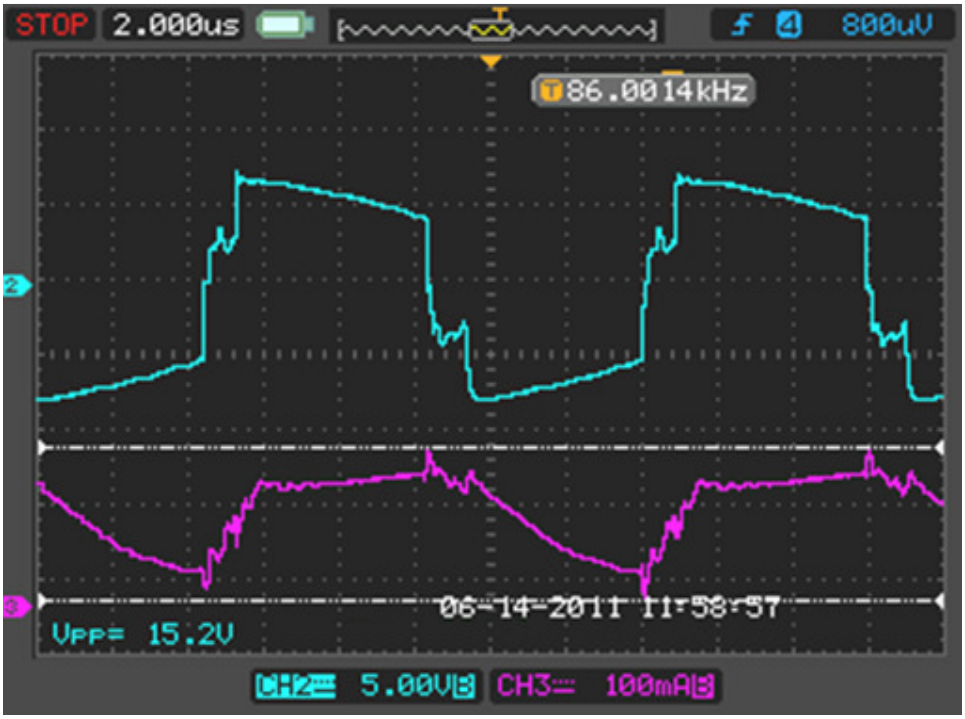

Figure 75: Transformer secondary voltage and primary current

Figure 76 shows the secondary voltage on each half of the winding of the transformer and the current measured through the inductor which is about 220 mA. Figure 77 presents the rectified voltage and the output voltage measured on the load resistor.

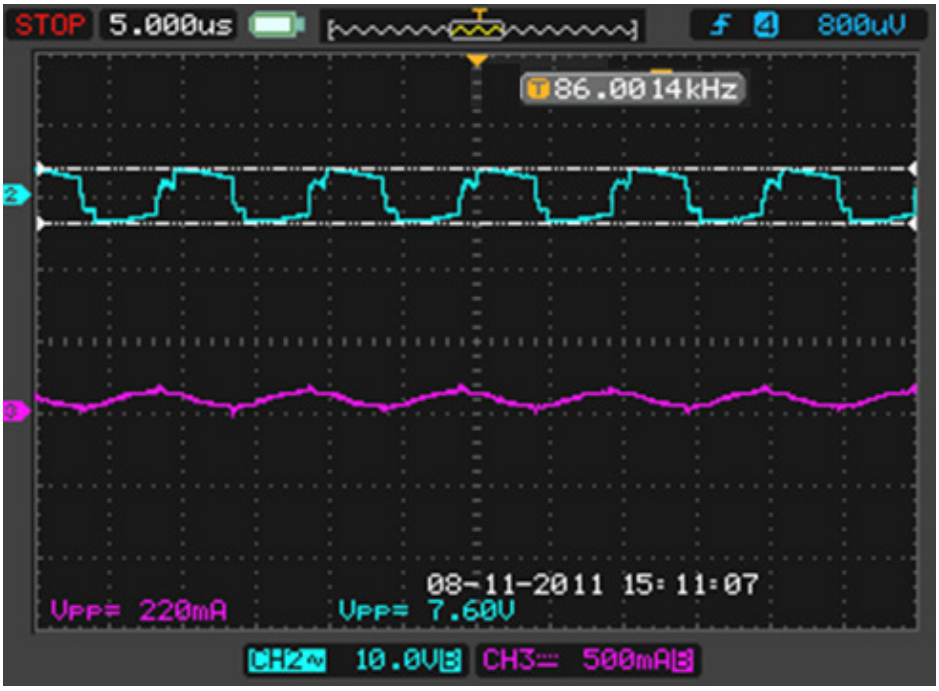

Figure 76: Top trace: Secondary voltage, bottom trace: Inductor current

Figure 77: Top trace: Rectified voltage, bottom trace: Output voltage

The switch module proved its legitimacy in DC converter application where it provided the required galvanic isolation and the floating voltage supply for the gate driver circuits. The next section presents the switch module in an AC converter application to test if it would work in a bidirectional way.

4.3.3 Control of AC chopper

The main aim of this experiment was to verify the validity of the switch module in an AC application, to control and vary the rms voltage on the load to the required value and to analyze the behaviour of the AC converter based on this module. An experimental set-up was built with a single phase mains of 220 V/50 Hz as shown in Figure 78.

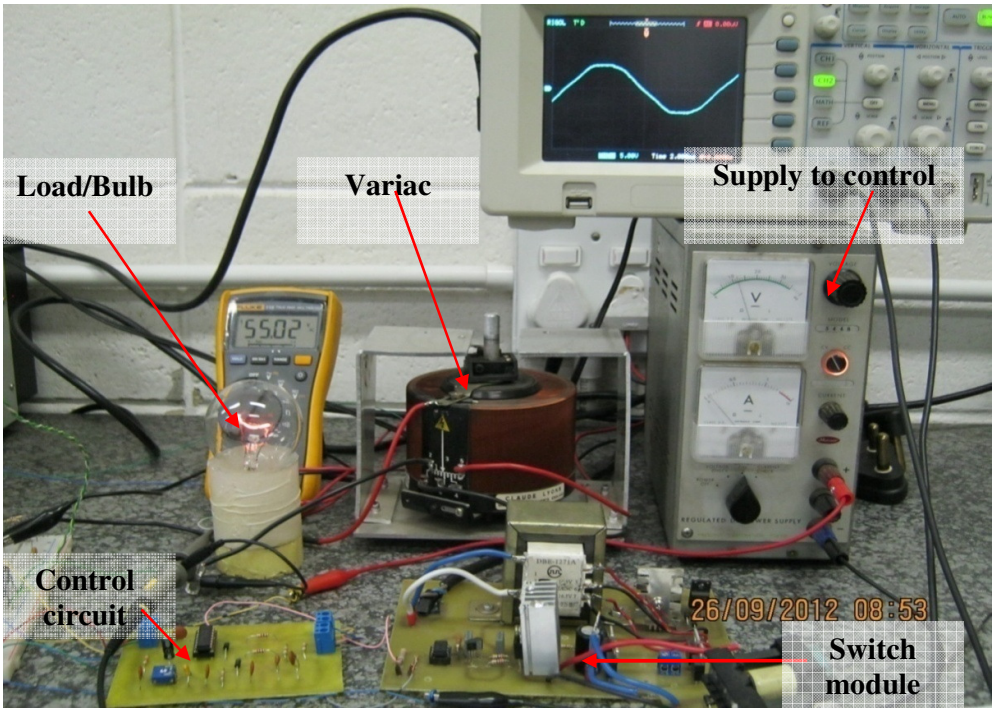

Figure 78: Practical set-up for AC converter

The system was used on a normal 60 W/220 V bulb and a Variac with 220 V input that can vary voltage from 0-275 V at 50 Hz was used to vary the AC voltage to 100

V. This variable or adjustable transformer was used to adjust the AC voltage to safely monitor the load's response to AC power and the results from the oscilloscope were recorded.

An AC voltage signal of 100 V rms shown in Figure 79, has been switched ON and OFF with a control signal of 1.92 kHz at a duty cycle of about 50% as shown in Figure 80. This was done in order to safely monitor the load's response to AC power.

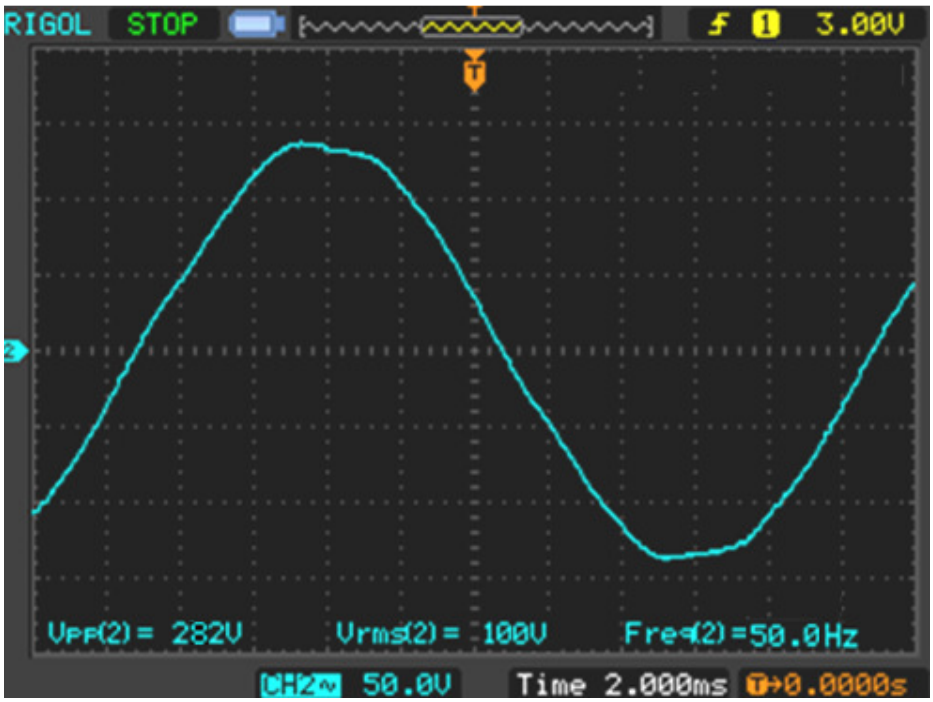

Figure 79: AC source adjusted to 100 V/50 Hz

Figure 81 and Figure 82 indicates the output voltage measured on a normal bulb 60 W – 240 V used as the load at 30% and 70% duty cycle respectively. As was presented earlier with the simulation graphs, this output looks more like a train of pulse amplitude modulated (PAM) pulses.

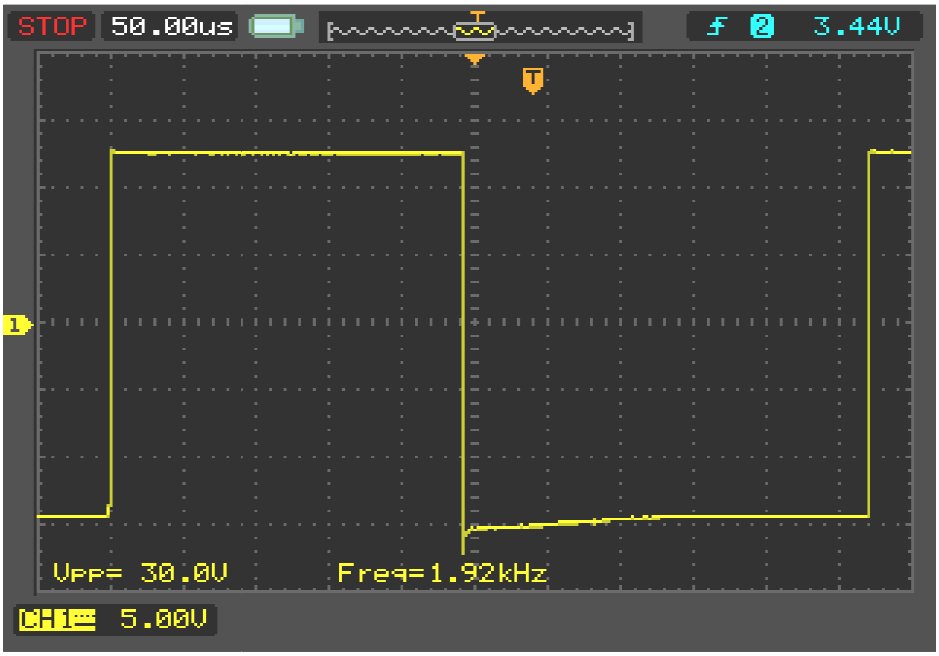

Figure 80: Control signal at 1.92 kHz

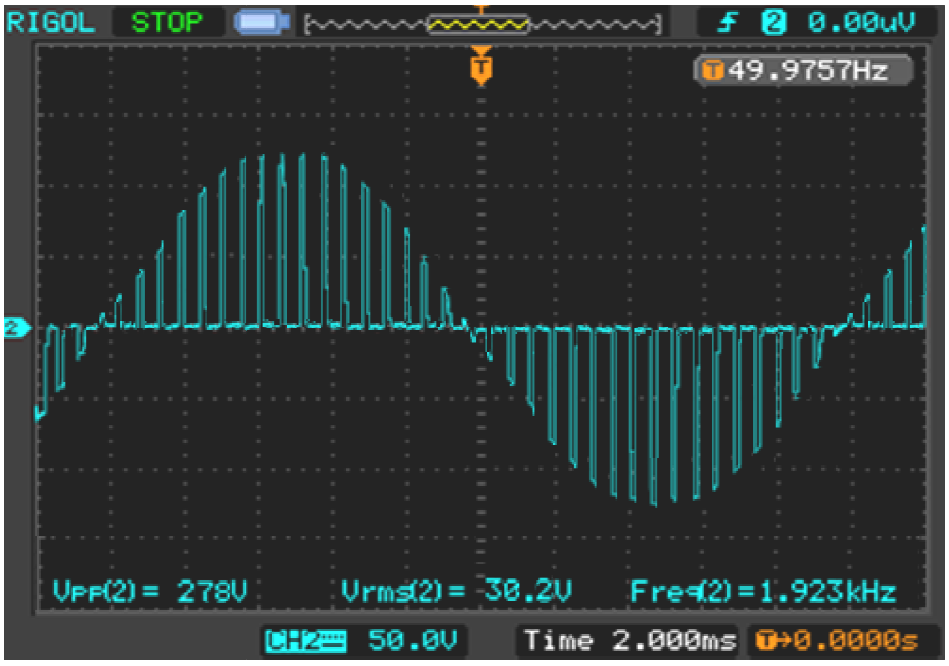

Figure 81: Load voltage at 30% duty cycle

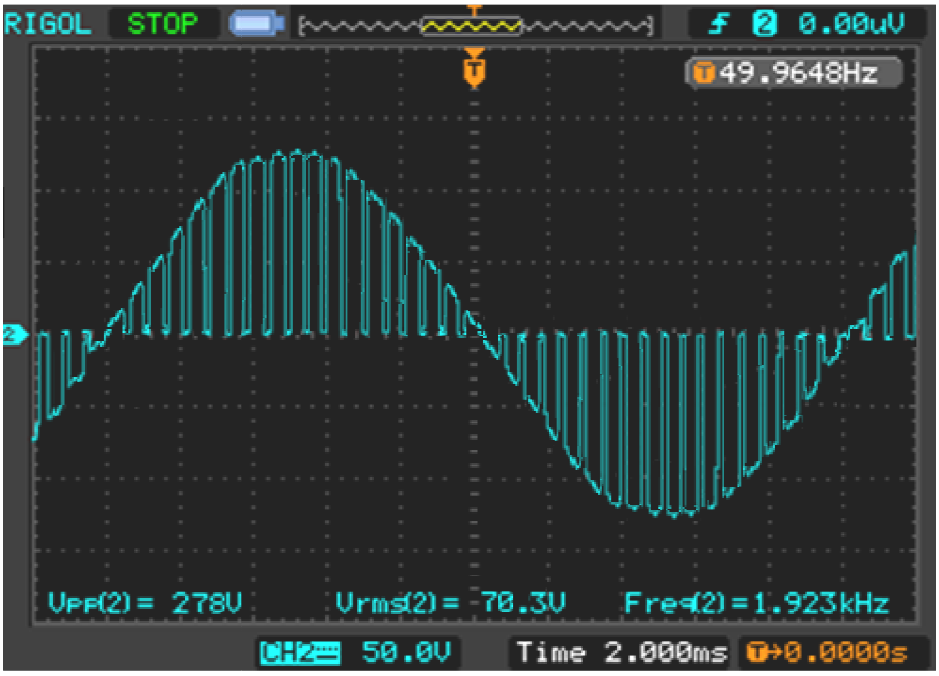

Figure 82: Load voltage at 70% duty cycle

From the prototype results it was realized that the AC output voltage had been chopped to the required rms voltage by adjusting the duty cycle of the switching control and it can also be seen that the AC voltage waveform has kept its sine wave shape. From the output regulation graph, the prototype waveforms show a close match with the simulation results, thereby validating all the theoretical predictions.

This shows that the output voltage can be controlled to the required value by adjusting the duty-cycle. From the graph it reveals that the load voltage v_o depends largely on the duty cycle of the control frequency on the gate of the switch.

4.6 Summary

The switch module prototype was built and tested. The module has achieved what it was set out for, which was to provide galvanic isolation, provide floating voltage supply for the gate-drive, to work in a bidirectional way and to work both in DC and

AC application. The module was optimised to work according to the desired specifications as stated in this chapter and this was followed by several experiments. The measurements and results of the galvanic isolated switch module have been comprehensively covered in this particular chapter. The output waveforms from the test control frequency generation stage incorporating the UC3825N PWM controller, the drive circuit and the power stage have been presented. The results of the complementary totem-pole drive circuit have also been discussed. Experimental results taken were discussed and compared with the simulation results and were found to meet and confirm the theoretical expectations.

The next Chapter considers the conclusions reached with regard to the development of the switch module. Recommendations as to the future research and development on the module will also be put forward.

Chapter 5: Conclusions and recommendations

The previous chapters addressed the switch module design considerations and tests were performed to ensure that the switch module worked accordingly. This chapter focuses on the conclusions drawn from this research and puts forward recommendations for future research.

5.1 Introduction

There were several challenges encountered during the designing phase of this project that were successfully solved. A prototype of the universal galvanic isolated switch module has been successfully completed for the research. It has been tested and also tested on different types of converter topologies and has obtained acceptable results. The work on discrete components laid a foundation and development of skills for addressing complex problems of any form. The following conclusions were drawn.

5.2 Conclusions

Integration of discrete and ICs components provides many advantages in speed, small footprint and power consumption. The ability of the high power MOSFET to operate at 100 kHz has been conclusively proven. The final waveforms from across the IRF530N MOSFETs indicated the successful switching up to 100 kHz and this has been confirmed by both the simulation and experimental results.

From the results obtained, it is clear that the experimental model and the simulated model's results agree favourably. The output from the MOSFET does resemble the input square waveform and exhibit the quality of a square waveform from the controller. It is also evident that it is able to switch rapidly at floating voltages.

Mathematical analysis, Simetrix simulations and experimental results have demonstrated that the proposed switch module functions very well in generating high

frequency voltage signals required by MOSFETs in switching ON and OFF of any converter whether in DC or AC application.

An isolated power supply constructed proved to have supplied a floating voltage supply for the opto-coupler and the gate-drive circuits which was required by the high power MOSFETs. It has also proven that the opto-coupler used in this regard provided galvanic isolation between the control and the power stage and the gate drive provided the required voltage level required to drive the MOSFET.

It has also been proven that the high power MOSFET gate does not significantly change the output waveform of the complementary emitter gate drive. The gate drive thus accomplishes the task of supplying sufficient charge to the gate of the high power MOSFET and also withdrawing it rapidly out of the gate. This proves that it adequately serves the purpose of a high power MOSFET driver.

It was also shown that the effective delay time between switching ON the top and bottom arm transistors in the half-bridge configuration could be decreased and increased depending on the converter topology applied with no effect on the converter reliability.

5.3 Recommendations

For future development, the use of the same module but built from IGBTs should be designed to withstand high temperature, so that the module can be able to work at high voltage level and the results can then be compared to the results of this document. The other factor to be considered for future research on this module is the modeling software for supervisory circuits: Heat-sink temperature monitor or sensor, over-voltage detector and over-current detector. The existence of high frequency MOSFET drivers that have a typical high-output resistance of 0.4 Ω which incorporate an opto-coupler and gate-drive circuit can be investigated in order to provide a simple interface to the module.

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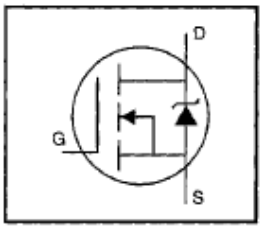
International
IOR Rectifier

PD-9.307O

IRF530

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 100V

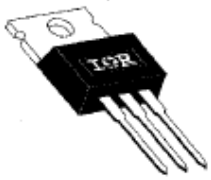
$R_{DS(on)}$ = 0.16Ω

I_D = 14A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	10	
I_{DM}	Pulsed Drain Current ①	56	
P_D @ T_C = 25°C	Power Dissipation	88	W
	Linear Derating Factor	0.59	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	69	mJ
I_{AR}	Avalanche Current ①	14	A
E_{AR}	Repetitive Avalanche Energy ①	8.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

PC410S/925L

SHARP

High Speed OPIC® Photocouplers

Enrico Dani, Silica Italy

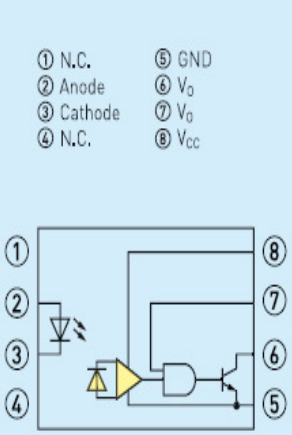
The PC410S Series of Photocouplers contains an LED optically coupled to an OPIC. It is packaged in an 8-pin mini-flat. The Input-output isolation voltage (rms) is 3.75kV. The PC410S is a high-speed device with a typ. response of 10Mb/s while CMR is min. 10kV/μs.

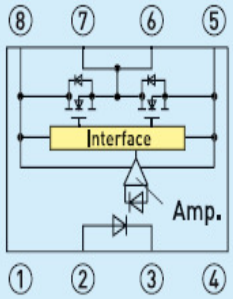
As well as the PC410S, the PC925L Series contains an LED optically coupled to an OPIC chip. It is packaged in an 8-pin DIP, available in SMT gull wing lead form option. The peak output current of the PC925L is 2.5A. Input-output isolation voltage (rms) is 5kV and High speed response (tPHL, tPLH max 0.5μs).

Key Features

- Double transfer mold package (Ideal for Flow Soldering)
- Recognized by UL1577 (Double protection isolation), file No. E64380
- Package resin UL flammability grade (94V-0)
- PC410S:
  - 8-pin mini-flat package
  - High noise immunity due to high instantaneous common mode rejection voltage. (CMH min 10kV/μs, CML min 10kV/μs)
  - High speed response: tPHL typ. 48ns, tPLH typ. 50ns
  - Isolation voltage between input and output (Viso (rms) 3.75kV)
  - Approved by VDE, DIN EN60747-5-2 (as an option), file No. 40009162
- PC925L:
  - 8-pin DIP and SMT packages
  - Built-in direct drive circuit for MOSFET/IGBT drive (IO (peak) 2.5A)
  - High speed response: tPHL, tPLH max 0.5μs
  - Wide operating supply voltage range (V_{CC}±15V to 30V)
  - High noise immunity due to high instantaneous common mode rejection voltage (CMH: MIN. 15kV/μs, CML: MIN. 15kV/μs)
  - Long creepage distance type (wide lead-form type only min 8mm)
  - High isolation voltage between input and output (Viso (rms) 5kV)

① N.C.
② Anode
③ Cathode
④ N.C.
⑤ GND
⑥ V_O
⑦ V_O
⑧ V_{CC}





*As for N.C. pins (①,④), external connection is not allowed.

Key Applications

- Programmable controller
- Inverter
- IGBT/MOSFET gate drive for inverter control

Unitrode Products from Texas Instruments

application INFO available

UC1825
UC2825
UC3825

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)

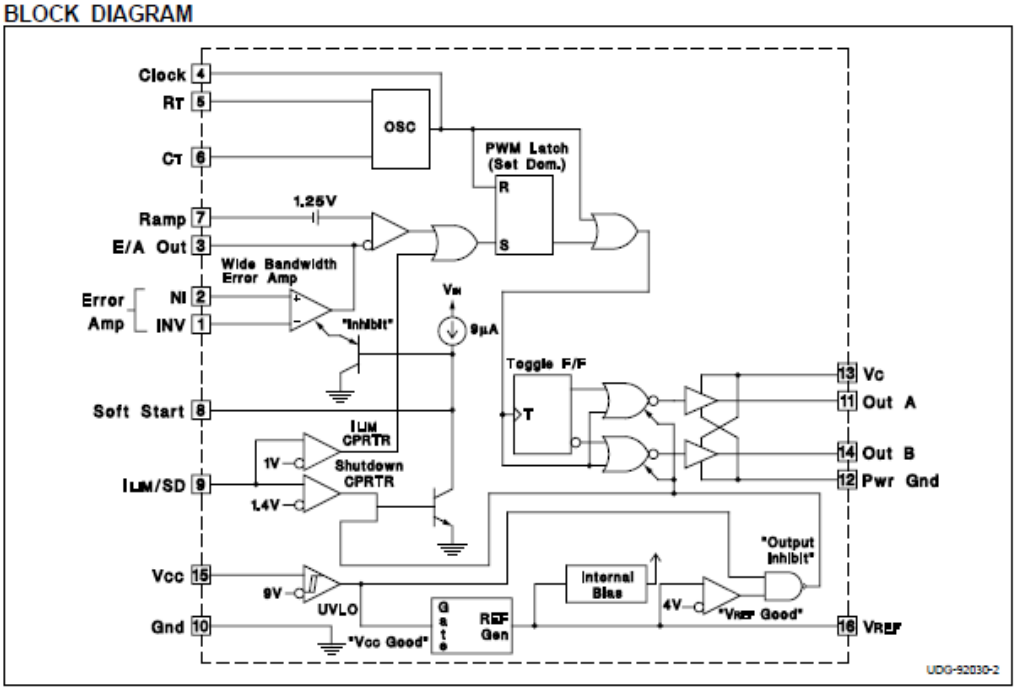
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_O.

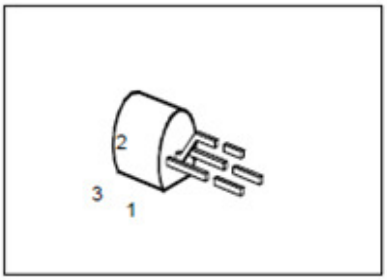
PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			
		MIN	TOP	MAX	MIN	TOP	MAX	UNITS
Reference Section								
Output Voltage	T_O = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J = 2°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs

SIEMENS

PNP Silicon AF Transistors

BC 327
BC 328

- High current gain
- High collector current
- Low collector-emitter saturation voltage
- Complementary types: BC 337, BC 338 (NPN)



Type	Marking	Ordering Code	Pin Configuration 1	2	3	Package[1)]
BC 327	–	Q62702-C311	C	B	E	TO-92
BC 327-16		Q62702-C311-V3				
BC 327-25		Q62702-C311-V4				
BC 327-40		Q62702-C311-V2				
BC 328		Q62702-C312				
BC 328-16		Q62702-C312-V3				
BC 328-25		Q62702-C312-V4				
BC 328-40		Q62702-C312-V2				

Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values min.	typ.	max.	Unit
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 20 MHz	f_t	–	200	–	MHz
Output capacitance V_{CB} = 10 V, f = 1 MHz	C_{obo}	–	12	–	pF
Input capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{ibo}	–	60	–	

NPN general purpose transistor BC337

FEATURES

- High current (max. 500 mA)
- Low voltage (max. 45 V).

APPLICATIONS

- General purpose switching and amplification, e.g. driver and output stages of audio amplifiers.

DESCRIPTION

NPN transistor in a TO-92; SOT54 plastic package.
PNP complement: BC327.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

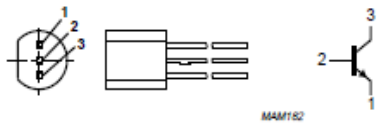


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	45	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	500	mA
I_{CM}	peak collector current		–	1	A
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	625	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

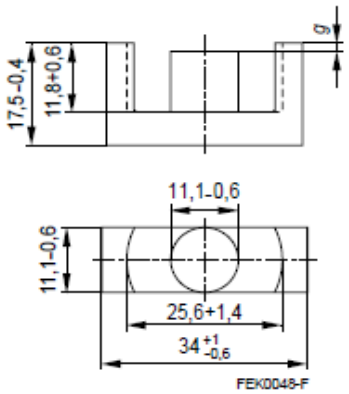
1. Transistor mounted on an FR4 printed-circuit board.

EPCOS

ETD 34/17/11

Core B66361

- To IEC 61185
- For SMPS transformers with optimum weight/performance ratio at small volume
- Delivery mode: single units



Magnetic characteristics (per set)

$\Sigma l/A$ = 0.81 mm^{-1}
l_e = 78.6 mm
A_e = 97.1 mm^2
A_{min} = 91.6 mm^2
V_e = 7630 mm^3

Approx. weight 40 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N27	2400 +30/–20%	1540	< 1.48 (200 mT, 25 kHz, 100 °C)	B66361G0000X127
N87	2600 +30/–20%	1670	< 4.00 (200 mT, 100 kHz, 100 °C)	B66361G0000X187
N97	2650 +30/–20%	1710	< 3.40 (200 mT, 100 kHz, 100 °C)	B66361G0000X197

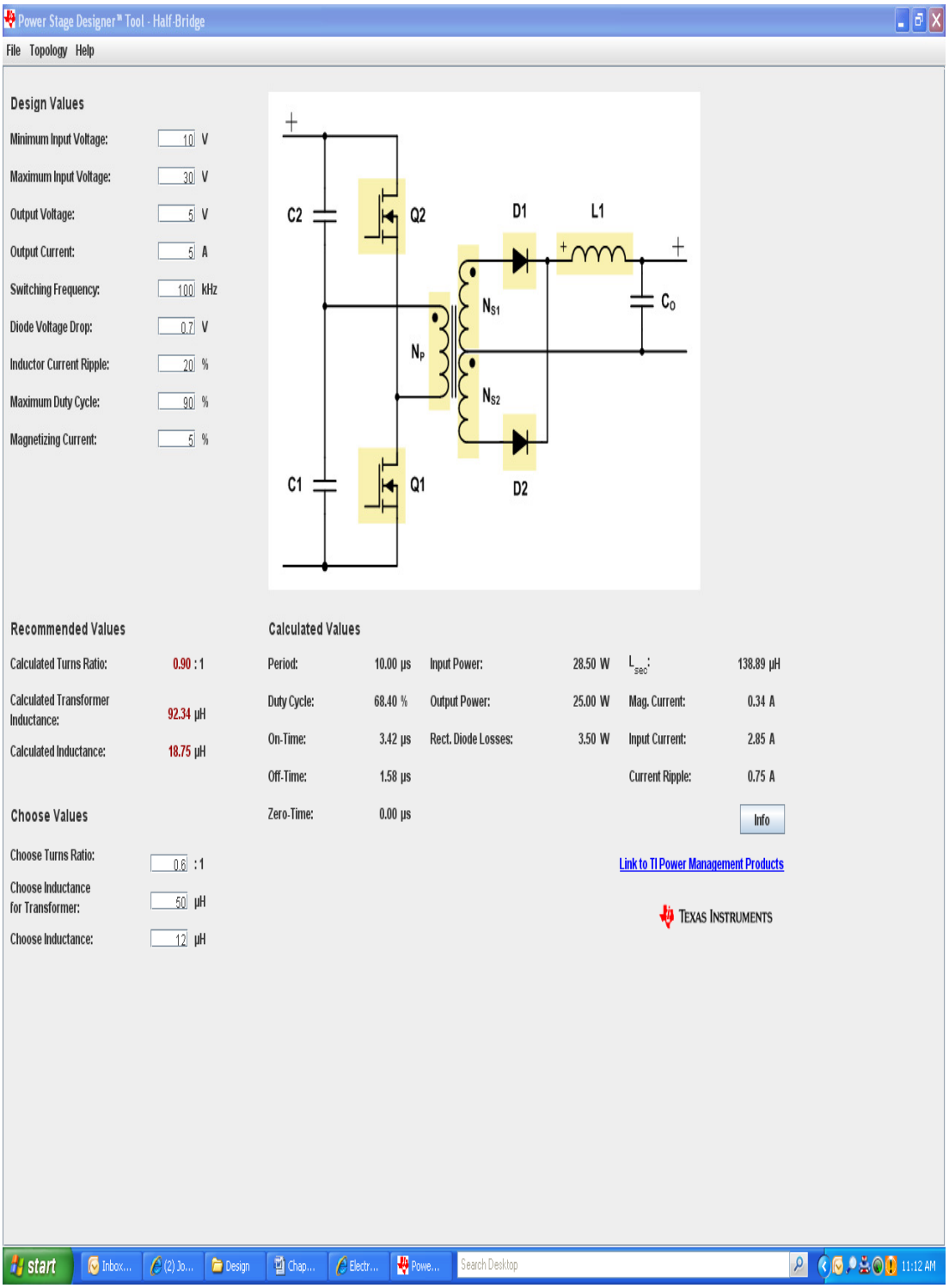
Gapped

Material	g mm	A_L value approx. nH	μ_e	Ordering code ** = 27 (N27) = 87 (N87)
N27, N87	0.10 ±0.02	790	508	B66361G0100X1**
	0.20 ±0.02	482	310	B66361G0200X1**
	0.50 ±0.05	251	161	B66361G0500X1**
	1.00 ±0.05	153	98	B66361G1000X1**

The A_L value in the table applies to a core set comprising one ungapped core (dimension g = 0) and one gapped core (dimension g > 0).

Power Stage designer tool

ANNEXURE G



MUR820 Power rectifiers' datasheet **ANNEXURE H**

MUR805, MUR810, MUR815, MUR820, MUR840, MUR860, MURF860

Preferred Devices

SWITCHMODE™ Power Rectifiers

This series are state−of−the−art devices designed for use in switching power supplies, inverters and as free wheeling diodes.

Features

- Ultrafast 25 and 50 Nanosecond Recovery Time
- 175°C Operating Junction Temperature
- Epoxy Meets UL 94 V−0 @ 0.125 in
- Low Forward Voltage
- Low Leakage Current
- Reverse Voltage to 600 V
- Pb−Free Packages are Available*

Mechanical Characteristics:

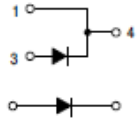
- Case: Epoxy, Molded
- Weight: 1.9 Grams (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max for 10 Seconds

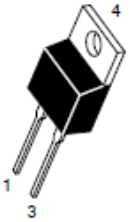
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

ULTRAFAST RECTIFIERS
8.0 AMPERES, 50−600 VOLTS

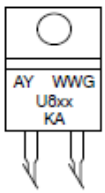


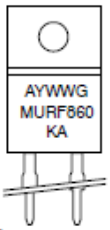


TO−220AC
CASE 221B
PLASTIC

TO−220 FULLPAK
CASE 221E
STYLE 1

MARKING DIAGRAMS





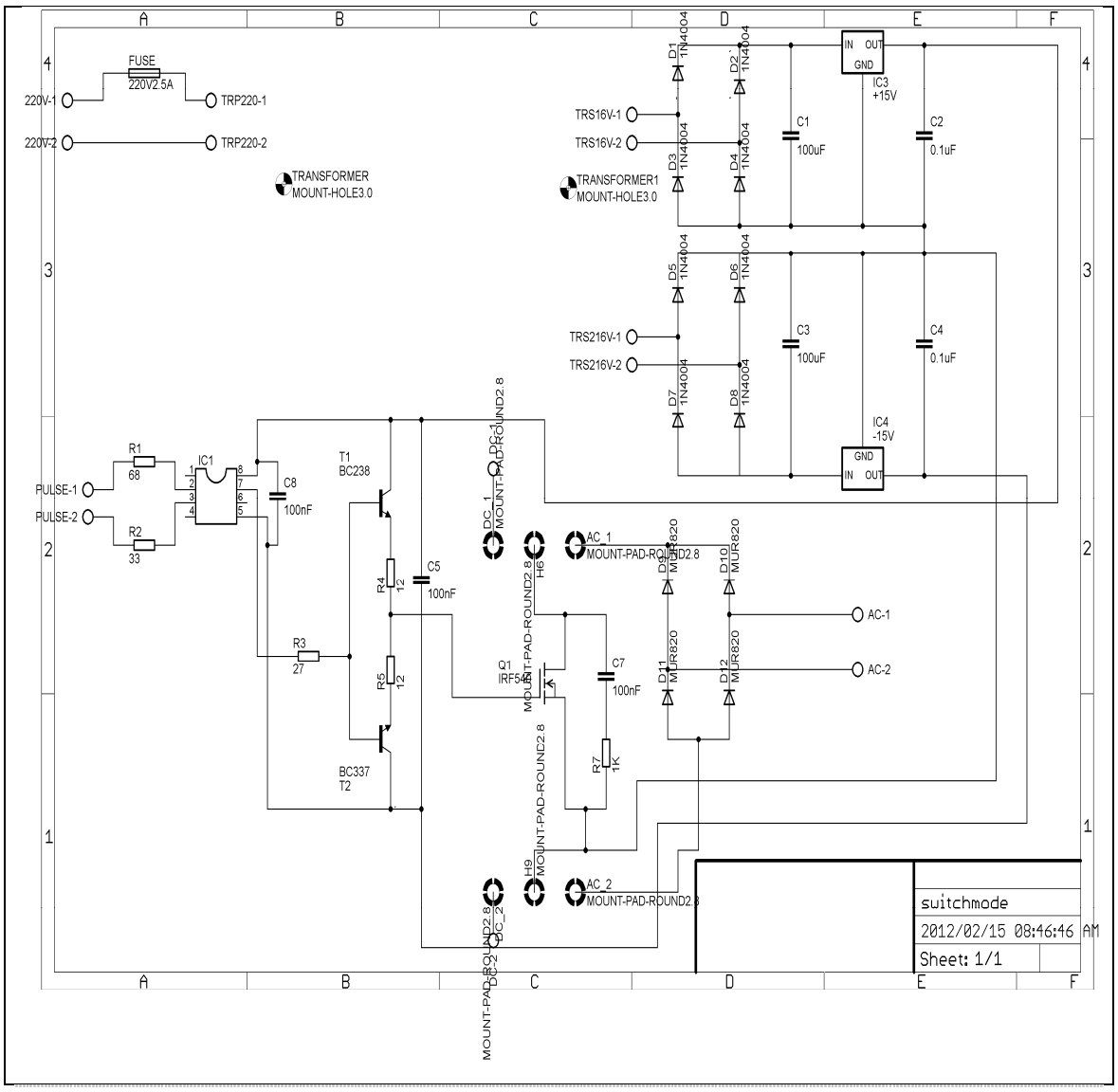
A = Assembly Location
Y = Year
WW = Work Week
U8XX = Device Code
xx = 05, 10, 15, 20, 40, or 60
G = Pb−Free Package
KA = Diode Polarity

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

Complete circuit diagram of the switch module **ANNEXURE I**


FUSE
220V2.5A
220V-1
220V-2
TRP220-1
TRP220-2
TRANSFORMER
MOUNT-HOLE3.0
TRANSFORMER1
MOUNT-HOLE3.0
TRS16V-1
TRS16V-2
TRS216V-1
TRS216V-2
D1 1N4004
D2 1N4004
D3 1N4004
D4 1N4004
D5 1N4004
D6 1N4004
D7 1N4004
D8 1N4004
C1 100uF
C2 0.1uF
C3 100uF
C4 0.1uF
IC3 +15V
IC4 -15V
IN OUT
GND
R1 68
R2 33
R3 27
R4 12
R5 12
R7 1K
C5 100nF
C7 100nF
C8 100nF
IC1
T1 BC238
T2 BC337
Q1 IRF540
PULSE-1
PULSE-2
DC_1
DC_2
AC_1
AC_2
MOUNT-PAD-ROUND2.8
H6
H9
D9 MUR820
D10 MUR820
D11 MUR820
D12 MUR820
AC-1
AC-2
switchmode
2012/02/15 08:46:46 AM
Sheet: 1/1