Design and Development of a High Efficiency Modulated Class E Amplifier

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Declaration

I declare that this is my own, unaided work. It is submitted for the Magister Technologiae to the Department of Applied Electronics and Electronic Communication at the Vaal University of Technology, Vanderbijlpark. It has not been submitted before for any qualification or examination to any educational institution.

Hendrik Lambert Helberg Crafford

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- My mother Marie Crafford, my fiancé Sannie Fowlds, family and friends for their continued encouragement and support.
- God for this opportunity in my life.

Dedication

I dedicate this work to my late father, Corrie Crafford, for proudly motivating and supporting me on reaching higher goals.

Abstract

Amplitude modulation is not commonly associated with effective amplifying. This work focuses on implementing amplitude modulation into a high efficiency Class E amplifier.

Different types of amplifiers are compared with each other, to show the advantages of using a Class E amplifier. The theory of the Class E amplifier is dealt with in detail. A harmonic filter is designed for the amplifier to make it radio spectrum friendly.

The modulation process is implemented with the aid of a transformer into the Class E amplifier. The advantage of this is that the transformer serves both as a radio frequency choke for the Class E circuit as well as a modulator.

The implementation of the amplitude modulation into the high efficient Class E circuit was successful. The final Class E circuit had superb efficiency, the harmonic filter showed good harmonic attenuation and the modulation process had low distortion. All this resulted in a fine low power AM transmitter.

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Glossary of abbreviations and symbols

AC	Alternating current
AM	Amplitude modulation
As	Steepness factor
BJT	Bipolar junction transistor
dB	Decibel
DC	Direct current
DSB	Double side band
DSBFC	Double side band full carrier
η	Efficiency
FET	Field effect transistor
FM	Frequency modulation
FSF	Frequency scaling factor
Hf	High frequency
IC	Integrated circuit
LPF	Low pass filter
Mosfet	Metal oxide field effect transistor
PCB	Printed circuit board
Q	Quality factor
Rf	Radio frequency
RFC	Radio frequency choke
RMS	Root mean square
VCO	Voltage controlled oscillator
VSWR	Voltage standing wave ratio

Chapter 1 Introduction

The increasing popularity of frequency modulation (FM) has resulted in the neglect of the development of amplitude modulation (AM) and little was done to improve its functioning and efficiency. There is at the moment very little unused radio frequency spectrum which has made AM more attractive because it uses less bandwidth when modulated, as compared to FM.

Most of the technology used in AM transmissions dates back to the 1960s. There are modern more effective radio frequency (rf) amplifiers available like Classes D, E and F, which are not currently used in AM. This work focuses on finding a more effective way of amplifying AM.

1.1 Background

In normal radio frequency transmissions a high percentage of the power is lost, due to the low efficiencies of classes A, B and C amplifiers. These amplifiers' efficiencies range between 50 and 90 percent in ideal situations. However, efficiencies tend to be even lower because in reality we do not deal with ideal devices. Typically, the maximum efficiency that would be obtained for a Class C AM transmitter is 75 percent (Butler, 1991). If this is combined with a modulation process which is 75 percent effective, the overall efficiency drops to 56,3 percent.

When a circuit has a low efficiency, it has certain negative implications. Figure 1 shows that for the same input power, different useable output powers can be obtained, depending on the level of efficiency. Higher currents are drawn by low efficiency circuits that provide the same output results as high efficiency circuits. This requires an increase in component sizes to be able to handle the higher temperatures generated. Furthermore, additional cooling has to be provided. These factors necessitate an increase

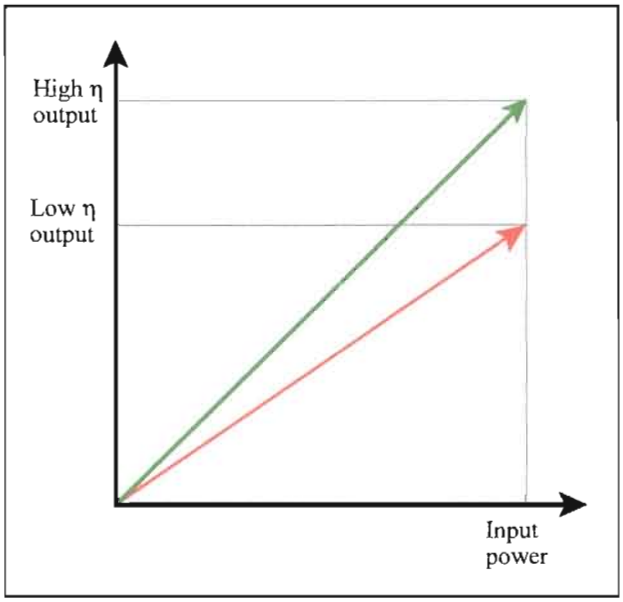

Figure 1 Low versus high efficiency

in the physical size of the equipment making it more cumbersome. These problems are compounded when these amplifiers are implemented in high-power applications where kilowatt transmitters are used. Basically, the power losses due to poor efficiency are very high and in the end it is a very costly problem.

A possible solution to alleviate the problem is to find a more effective amplifier configuration for the transmission process. Such a amplifier is the Class E configuration with an ideal efficiency of 100 percent and a typical efficiency of at least 90 percent.

1.2 Problem statement

The objective is to design an amplitude modulated rf amplifier with the use of a more effective amplifier such as the Class E rf amplifier.

1.3 Methodology

To obtain a general understanding of the functioning of a Class E amplifier, the first step was to design a very simple Class E amplifier. The aim was to gain knowledge on the

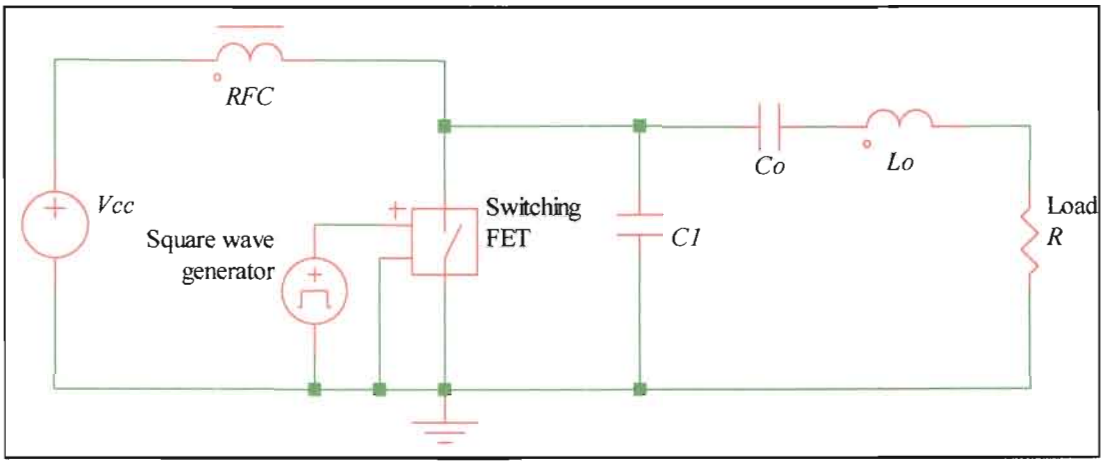

Figure 2 Basic Class E amplifier

basic circuit operation and to apply the theory to practice. For a preliminary theoretical understanding on high efficiency amplifiers, and specifically Class E, various textbook examples and problems were worked out.

A large part of chapter two is dedicated to the different types of amplifiers available, both non high and high efficiency amplifiers. Here reasons are given as to why the Class E amplifier, shown in Figure 2, was the high efficiency amplifier of choice. An in depth study was done on the operation of Class E amplifiers. All the formulae needed to design a Class E amplifier were studied as well.

The Switching Field Effect Transistor (FET) and the square wave generator in Figure 2 are very important aspects of the Class E amplifier. With this in mind, an intensive research study was done to find the correct combination of the two components. This is reported in chapter three. This was followed by the actual design of the Class E amplifier with a carrier frequency of 1,8 MHz to make it more usable for radio amateurs and long distance broadcasting. Since the end product will function as an amplitude modulated (AM) transmitter, a harmonic filter was also designed. The Class E amplifier and filter were software simulated with the aid of Simetrix 4.1.

Furthermore, chapter three dealt with the implementation of AM into the Class E

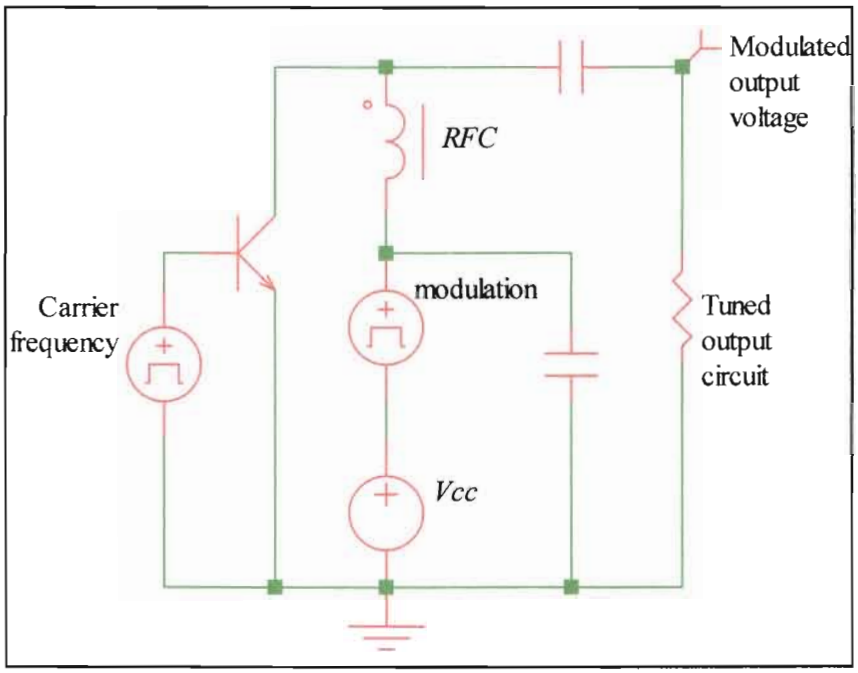

Figure 3 Simple generation of AM
(Krauss, Bostian and Raab, 1980:223)

amplifier by replacing the *RFC* inductor in Figure 2 with a modulation transformer. A basic AM generating circuit is shown in Figure 3. The resulting circuit was also simulated.

All the simulations and calculations were tested with bench top measurements on the built circuit. These results are given in chapter four.

The work done on the project was concluded in chapter five and some future recommendations are given.

1.4 Value of the research

Amplitude modulation was successfully amplified with the use of a Class E amplifier.

This research provides the industry with a high efficient AM radio frequency amplifier which saves on dissipated power. This saving will result in cost saving especially in high

power implementations. Furthermore, the project was completed with fairly low cost components which will benefit the commercial market as well as amateur applications.

The study also broadens the research done by the Vaal University of Technology on Class E amplifiers.

1.5 Delimitations

This study will not consider angle modulation, which includes frequency modulation and phase modulation. The only modulation which will be covered is double side band full carrier (DSBFC) amplitude modulation. Other forms of AM like single side band (SSB) and double sideband suppressed carrier (DSBSC) will not be considered.

The design of the audio amplifier which is used to amplify the low-level input signal to a high voltage wave, with the use of an additional step up audio transformer, will not form part of the research.

A 13,8 V direct current (DC) supply is used as a power source. The 13,8 V direct current power source will not form part of the research. Any existing, good quality power supply can be used.

1.6 Summary

This chapter provided information on:

- The importance of higher efficiency circuits
- The research methodology followed in this study on a high efficiency Class E amplifier with AM modulation
- The value added by the research
- The delimitations of the project

Chapter 2 Class E amplification

Class E amplification is the fundamental objective of this work. In order to use the Class E in a radio frequency amplifier, it is of utmost importance to understand the working of it thoroughly. In this chapter a comparison of the various non-high and high efficiency radio frequency amplifiers are given, followed by a theoretical analysis of the Class E amplifier.

2.1 Radio frequency amplifiers

There are different types of amplifier configurations. These can be separated from each other by the class of operation. The commonly known classes are A, B and C amplifiers. The high efficiency amplifier classes are D, E, F, G, H and S. All of the above mentioned amplifiers' efficiencies for ideal devices are given in Table 1 (Krauss *et al.*, 1980:472).

Table 1 Ideal efficiency of power amplifiers

Class of amplifier	Efficiency
A	50%
B	78,5%
C	85 - 90%
D	100%
E	100%
F	88,4 - 100%
G	84,2%
H	100%
S	100%

2.1.1 Non high efficiency amplifiers

These will include classes A, B and C as stated above. The difference between these amplifiers is the angle at which the output current flows in comparison to the input signal (Jansen van Vuren, 1994:244).

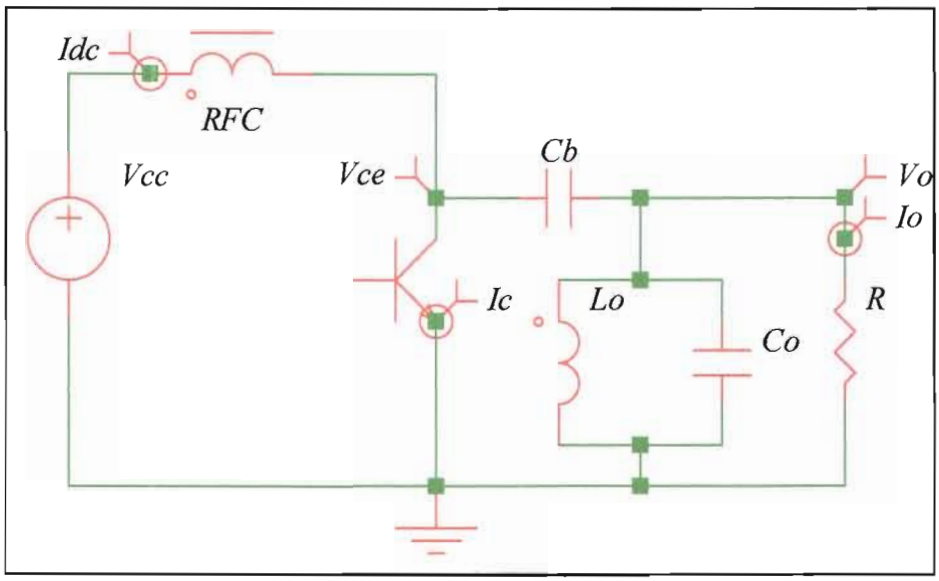

Figure 4 Class A amplifier circuit (Krauss *et al.*, 1980:353)

For Class A amplifiers, the output current flows for the whole 360° of the input signal. Figure 4 shows the typical Class A circuit diagram with the output current waveform in Figure 5.

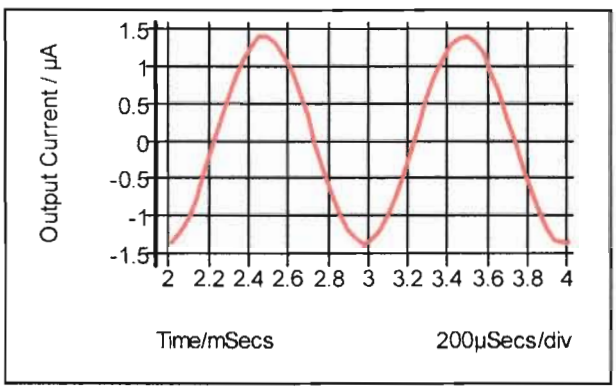

Figure 5 Class A output current

The efficiency of Class A will never be above 50 percent. If, in Figure 4, the maximum output voltage is *Vo* and the supply current is *Idc,* then the input power can be calculated using equation (1).

$$Pi = VccIdc = \frac{Vcc^2}{R} \text{ W} \qquad \textbf{(1)}$$

It is stated by Krauss *et al.* (1980:352) that the *Vo* must always be less than *Vcc* due to saturation effects. The root mean square (RMS) output voltage will be $Vo^2/2$. The output power is then defined by equation (2) with *Vom* as the peak value of *Vo*.

$$Po = \frac{Vom^2}{2R} \leq \frac{Vcc^2}{2R} \text{ W} \qquad \textbf{(2)}$$

The resultant efficiency (η) is given in equation (3):

$$\eta = \frac{Po}{Pi} = \frac{Vom^2}{2Vcc^2} \leq \frac{1}{2} \qquad \textbf{(3)}$$

In Class B the output current flows only 180° of the input signal. Class B amplifier operation is much more efficient than Class A. The push-pull configuration seen in

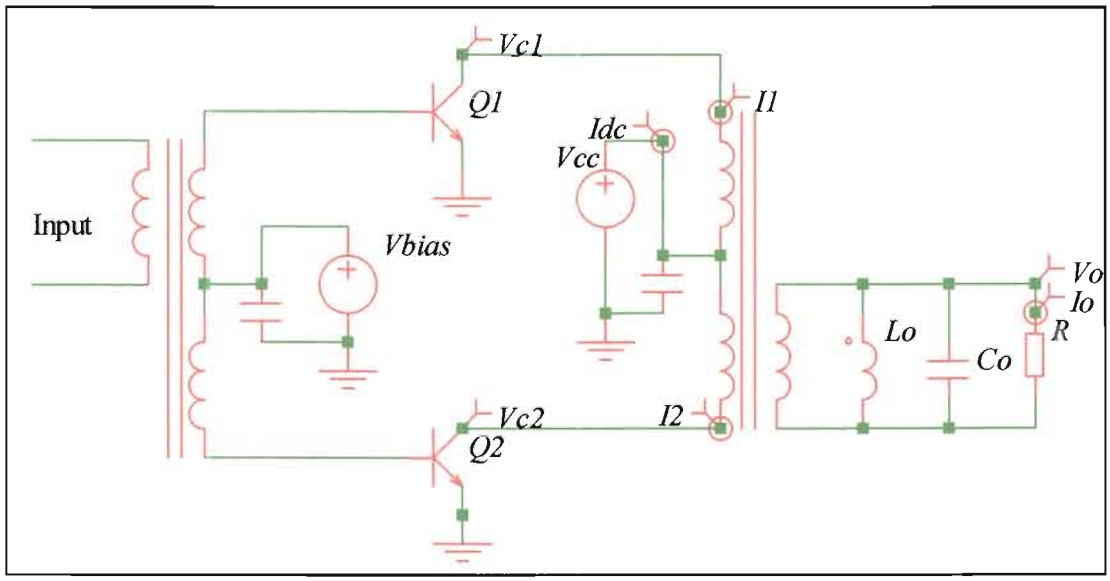

Figure 6 Class B amplifier circuit (Kennington, 2000:99)

Figure 6 employs two Class B stages operating in the opposite phase (Kenington, 2000:98). Each stage conducts a separate half of the input waveform. This opposite phase arrangement ensures that, whilst one device is conducting, the other is off and consumes no power.

Classical Class C power amplifier circuit topology is the same as that of the Class A amplifier (Krauss *et al.*, 1980:394). The active device is also driven to act as a current source. The difference is that the current waveform it produces is not the sinusoidal current desired in the load, but may be a variety of shapes. What makes it more efficient is that the output current flow is less than 180° of the input signal.

2.1.2 High efficiency amplifiers

Krauss *et al.* (1980:432) define high efficiency amplifiers as a power amplifier that achieves an efficiency greater than that normally achieved by a Class A, B or C amplifier in the same application.

Classes D, E and S are called switching mode power amplifiers. Here the active devices are used as switches, which eliminates voltages over it or current through it at the same time. This results in zero dissipated power in the device. According to Kenington (2000:124) Class S amplifiers are principally limited to low radio frequency applications because very wide bandwidth devices are required, but also due to the unavailability of radio frequency PNP transistors.

Other methods are used to obtain high efficiency in Classes F, G and H. Techniques such as harmonic resonators and multiple power supply voltages are used to reduce the collector voltage-current product. According to Kenington (2000:124) Classes G and H amplifiers are principally limited to audio frequency applications due to wide bandwidths required for the active components. Class G requires more than one supply

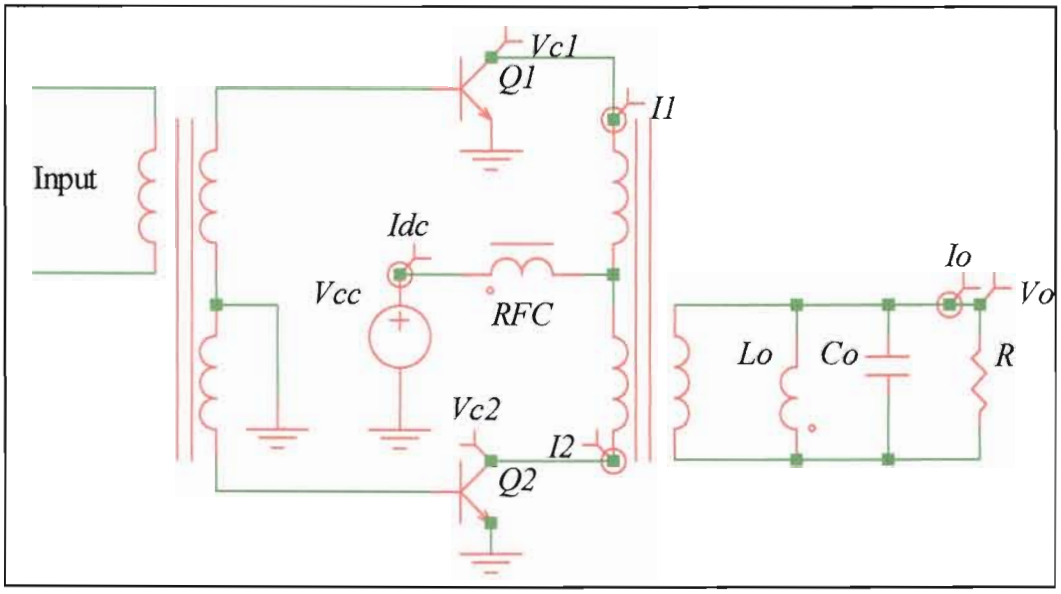

Figure 7 Class D amplifier circuit (Kennington, 2000:119)

voltage and at least two pairs of active devices. Class H also uses two amplifier stages, of which the one driving the main amplifier stage must be highly efficient.

The most basic Class D configuration is the Complementary Switching Amplifier. Figure 7 illustrates this setup. The two transistors, *Q1* and *Q2*, work together as a changeover switch between supply voltage and ground. This is managed via the splitter transformer which drives *Q1* and *Q2* 180° out of phase, thus when *Q1* is on, *Q2* is off and vice versa.

Class E amplifiers are described by Kenington (2000:121) as a single-ended switching configuration with a passive load network as illustrated in Figure 8. The fundamental configuration of a Class E amplifier consists of the series-tuned inductor-capacitor (*Lo-Co*) circuit and a shunt capacitance (*C1*) across the collector-emitter junction. In this case the emitter must be grounded. What makes this setup so advantageous is that this shunt capacitance may be composed of the inherent junction capacitance (*Ci*) of the transistor, as well as some additional capacitance to ensure correct circuit operation. Thus the transistor's inherent capacitance is no longer a source of power loss but becomes an essential part of the circuit's operation. The operation of Class E works on

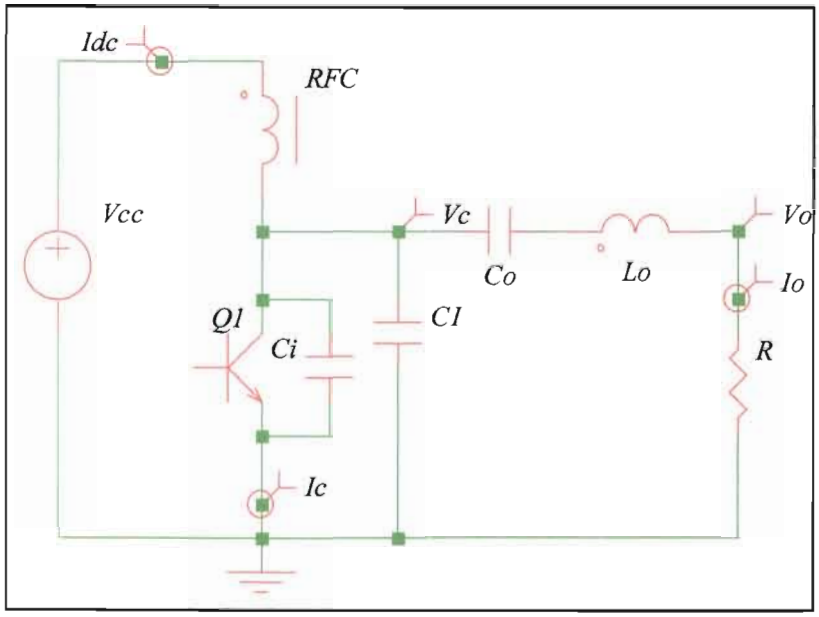

Figure 8 Class E amplifier circuit (Kennington, 2000:122)

the principal that the transistor is operated as an ideal switch with zero "on" resistance and infinite "off" resistance.

Class F is described by Krauss *et al.* (1980:454) as an amplifier characterized by a load network that resonates at one or more harmonic frequencies as well as at the carrier

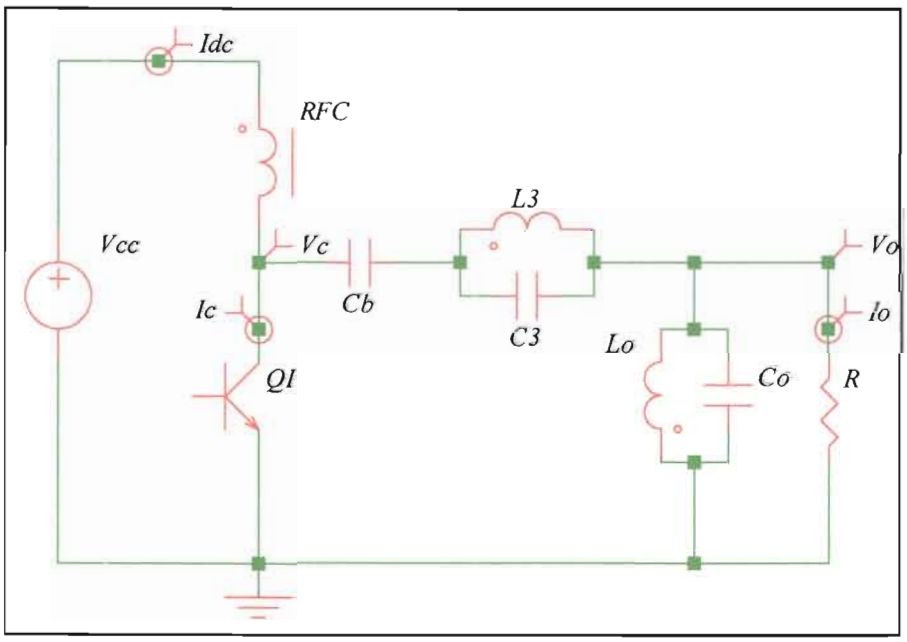

Figure 9 Class F amplifier circuit (Krauss *et al.*, 1980:455)

frequency. The active device usually operates primarily as a current source or a saturating current source, as it does in the classical Class C power amplifier. Figure 9 shows the third harmonic peaking amplifier. The transistor acts as a current source, producing the same half-sine wave as it would in Class B operation. The fundamental-frequency tuned-circuit bypasses the harmonics, producing a sinusoidal output voltage. The third harmonic resonator makes it possible for a third harmonic component in the collector voltage. This results in higher efficiency, but at the same time it also results in higher output capability.

2.2 Choice of amplifier

The choice of an appropriate radio frequency (rf) amplifier was made by taking all the relevant information of section 2.1 into consideration, as summarized in Table 2.

Table 2 Characteristics of different classes of amplifiers

Class of operation	Complexness of circuit	Frequency of operation	Ideal Efficiency
A	low	low level rf	50%
B	high	rf	78,5%
C	low	rf	85-90%
D	medium	low power hf	100%
E	low	rf	100%
F	medium	rf	88,4-100%
G	high	audio	84,2%
H	high	audio	100%
S	medium	low rf	100%

For this project a high efficiency amplifier was needed, which automatically disqualified

Classes A, B and C amplifiers. Although Class C has high efficiency, it is not comparable to the so called high efficiency amplifiers.

Amongst the high efficiency amplifiers of Classes D through to S, Classes G and H are not suitable for radio frequency applications, moreover the efficiency of Class G is not high enough. Amongst these classes only Class E and F are not limited by the operating frequency range.

The complexness of the circuit is determined by the number of active components, which are the transistors, the number of transformers needed, as well as the number of capacitor-inductor tuned circuits of the simplest design in the class. To rate the different classes of amplifiers, each is "allowed" one transistor, one transformer or radio frequency choke (RFC) and one tuned circuit. Everything extra will make it a step more complex. According to these criteria, Classes A, C and E have the least complex circuit configurations.

Taking all these factors into consideration, Class E appears to be the best choice. The complexness of its circuit configuration is low with only one transistor, one radio frequency choke and one inductor-capacitor tuned circuit. Class E is also very efficient and it is not limited by the operating frequency. This makes it more cost effective and simpler to use.

2.3 The Class E radio frequency amplifier

A good understanding of the operation of Class E amplifiers is required to deal with the rather complex formulae.

2.3.1 Class E operation

Recalling the basic principles of Class E amplifiers from section 2.1.2 it is clear that

Class E amplifiers employ a single transistor that is driven to act as a switch and connected to a passive load network (Krauss *et al.*, 1980:448) (Figure 10). This operation of maintaining a low product of transistor voltage and transistor current is used to obtain the high efficiency. The reasons why the voltage-current product is low throughout the radio frequency period are given by Sokal (1998:1109) as:

- In the "on" state the voltage is nearly zero when high current is flowing. The transistor acts as a low resistance "on" switch during this part of the radio frequency period.
- In the "off" state the current is zero when there is high voltage. The transistor acts as an "off" switch during this part of the radio frequency period.

Although the switching transitions are usually made as fast as feasible, a high efficiency technique must accommodate the transistor's practical limitation for radio frequency and microwave applications. The transistor switching times will, unavoidably, be noticeable fractions of the radio frequency period. Even though the switching times can be noticeable fractions of the radio frequency period, a high voltage-current product during the switching transition can be avoided by fulfilling two strategies in a suitable load network between the transistor and the load. These two strategies are:

- The rise of transistor voltage is delayed until after the current has reduced to zero.
- The transistor voltage returns to zero before the current begins to rise.

Two additional waveform features reduce power dissipation:

- The transistor voltage at turn-on time is nominally zero (or the saturation offset voltage for Bipolar Junction Transistor (BJT)). This means that the turning-on transistor does not discharge a charged shunt capacitance (C in Figure 10) thus avoiding dissipating the capacitor's stored energy of $CV^2/2$, at f times per

second. Where C is the capacitance value, V is the capacitor's initial voltage at transistor turn-on and f is the operating frequency.

- The slope of the transistor voltage waveform is nominally zero at turn-on time. Then the current injected into the turning-on transistor by the load network rises smoothly from zero at a controlled moderate rate, resulting in low i^2R power dissipation while the transistor conductance is building-up from zero during the turn-on transition, even if the turn-on transition time is as long as 30 percent of the radio frequency period.

Thus, the waveform never has high voltage and high current simultaneously. The voltage and current switching transitions are time-displaced from each other, to accommodate transistor switching transition times that can be substantial fractions of the radio frequency period. These fractions can be up to 30 percent for turn-on transition and up to 17 percent for the turn-off transition of the period.

Seeing the transistor as a switch, an equivalent circuit for Figure 8 can be drawn as seen

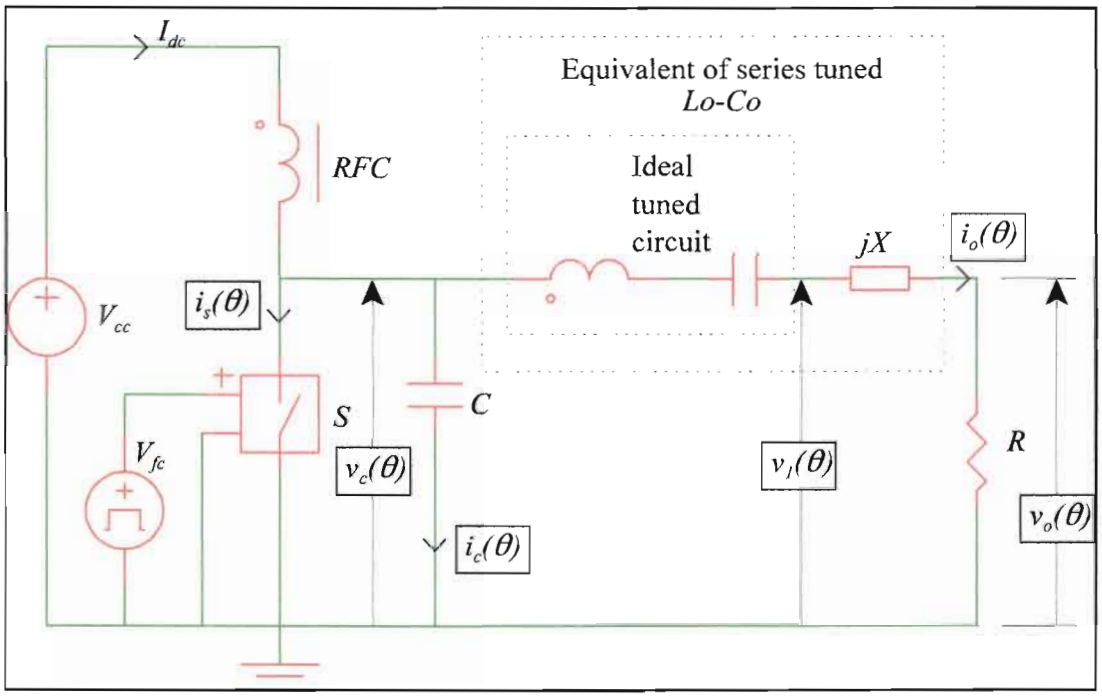

Figure 10 Class E amplifier equivalent circuit (Krauss *et al.*, 1980:449)

in Figure 10. The transistor (the switch) is connected to a passive load network. This load network is the series tuned *Lo-Co*. The reactance of this ideal-tuned circuit is zero at the operating frequency and infinite at the harmonic frequencies. Capacitor *C* in Figure 10 is composed of both capacitors *Ci* and *C1* in Figure 8.

Krauss *et al.* (1980:449) give four assumptions about the circuit which are used to analyse the operation of a Class E power amplifier (refer to Figure 10):

- The choke *RFC* has a reactance large enough so that the current I_{dc} flowing through it is constant.
- The quality factor (*Q*) of the series-tuned circuit (*Lo-Co*) is high enough so that the output current (hence the output voltage) is sinusoidal.
- The transistor *Q1* (from Figure 8) is driven to act as a switch S that is either "on" (with zero voltage across it) or "off" (with zero current through it) except for very brief periods of time during the transitions between "on" and "off" states.
- The capacitance *C* is independent of voltage. Thus, there is no varactor effect.

2.3.2 Class E formulae

From an understanding of the operation of the Class E amplifier (section 2.3.1), formulae can be derived that make it possible to obtain component values for the Class E amplifier design.

2.3.2.1 Principle formula

These formulae are gathered from Krauss *et al.* (1980:450). The total period of the Class E cycle can be divided into two parts, which are, when switch *S* in Figure 10 is on and when it is off.

When switch S is on, the following are relevant:

Voltage over capacitor C	$v_C(\theta) = 0$
Current in capacitor C	$i_C(\theta) = 0$
Current through switch S	$i_S(\theta) = I_{dc} - i_O(\theta)$ A

When the switch S is off, the collector voltage waveform is produced by charging of shunt capacitor C and the following are relevant:

current through the switch S	$i_S(\theta) = 0$
the capacitor current	$i_C(\theta) = I_{dc} - i_O(\theta)$ A

It is stated by Krauss *et al.* (1980:450) that when switch S changes from off to on, any charge in C is essentially instantaneously discharged; the discharge waveforms are unimportant, since the total energy involved depends upon only the capacitance and the voltage on it just prior to discharge.

The following determine the parameters of the voltage over the capacitor C when the switch is off:

- The magnitude I_{dc} of the dc (direct current) input current
- The amplitude $I_{om} = V_{om}/R$
- Phase Φ of the rf output current

Thus:

$$vc(\theta) = \left[\begin{array}{l} \frac{Idc}{B}\left(y - \frac{\pi}{2}\right) + \frac{Vom}{BR}\sin(\Phi - y) + \\ \frac{Idc}{B}\theta + \frac{Vom}{BR}\cos(\theta + \Phi) \end{array} \right] \text{V} \qquad \textbf{(4)}$$

In the above:

- y is the switch off-time (converted to radians).
- B is the susceptance of the shunt capacitance C at the frequency of operation.
- The fundamental frequency component of this voltage is $v_1(\theta)$, which is applied to $R+jX$ to determine the rf output current, voltage and power.
- The dc component of the capacitor C-voltage waveform must be Vcc.

The elements of the circuit in Figure 10 are all ideal. The only generated loss occurs when the switch closes. When this happens, the shunt capacitance C will discharge. In order to eliminate this loss, for optimum performance in Class E, the capacitor voltage should reach zero the moment the switch turns on. To achieve this, the values of B and X should be manipulated.

Another influence on the selection of B and X, for optimum performance, is the slope

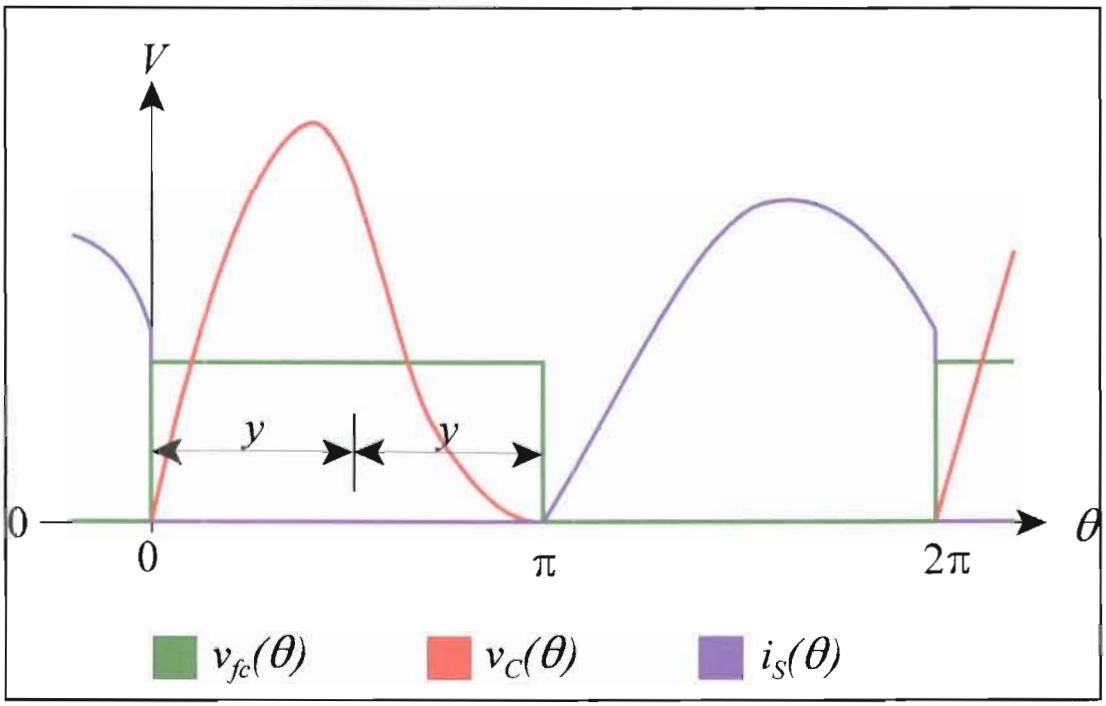

Figure 11 Waveforms for optimum Class E performance (Krauss *et al.*, 1980:451)

$dv_C(\theta)/d\theta$ of the capacitor C voltage waveform. This slope must be zero at the time the switch closes which implies that the current through the switch must be zero just after the switch closes.

It is clear that the dissipated power will be negligible if the capacitor C voltage as well as the current through the switch is zero the moment the switch closes. Figure 11 shows the relevant waveforms for optimum performance in Class E with reference to Figure 10. The function $v_{fc}(\theta)$ is the carrier frequency voltage, at which rate the switch is switching on and off, and y is the duty cycle. The duty cycle will be optimum where the duty cycle is equal to $\pi/2$.

2.3.2.2 Optimum performance

Krauss *et al.* (1980:450) explain that, to be able to calculate B and X for optimum performance, equation (4) and its derivative with respect to θ should be set equal to zero at $\pi/2+y$ or π for a 100 percent optimum performance. The results being:

- Phase of the rf output current:

$$\Phi = -32{,}48° \quad \textbf{(5)}$$

- Susceptance of the shunt capacitance C:

$$B = \frac{0{,}1836}{R}\ \text{S} \quad \textbf{(6)}$$

- Reactance for *Lo-Co* with very high Q:

$$X = 1{,}152R\ \text{Ohm} \quad \textbf{(7)}$$

- Output Voltage:

$$Vom = \frac{2}{\sqrt{1+\pi^2/4}} Vcc \approx 1{,}074 Vcc \text{ V} \quad \textbf{(8)}$$

- Output power:

$$Po = \frac{2}{1+\pi^2/4} \frac{V_{cc}{}^2}{R} \approx 0{,}577 \frac{V_{cc}{}^2}{R} \text{ W} \quad \textbf{(9)}$$

- Input current:

$$I_{dc} = \frac{V_{cc}}{1{,}734R} \text{ A} \quad \textbf{(10)}$$

- Peak voltage over capacitor C:

$$V_c = 3{,}56 V_{cc} \text{ V} \quad \textbf{(11)}$$

- Peak current through the switch:

$$I_s = 2{,}86 I_{dc} \text{ A} \quad \textbf{(12)}$$

- Normalized power output capability:

$$P_{\max} = 0{,}0981 \text{ W} \quad \textbf{(13)}$$

2.3.2.3 Practical consideration

For optimum performance the Q is very high. According to Krauss *et al.* (1980:452) this is usually in the range from three to ten in practise. This will allow some harmonic current to flow which will cause the capacitor C voltage to be non-zero or have a non-zero slope at the time the switch closes.

The inductor *Lo* in Figure 8 defines Q as (ideally tuned):

$$Q = \frac{\omega L_O}{R} \tag{14}$$

Note that for the tuned circuit

$$X_{Co} = X_{Lo}$$
$$\therefore Q = \frac{\omega L_O}{R} = \frac{1}{\omega C_O R} \tag{15}$$

Thus, with $Q < \infty$, optimum performance can be achieved by using the following empirically derived formulas where X_{LD} is the detune inductor (jX) in Figure 10:

$$X = \frac{1{,}110Q}{Q - 0{,}67} R \text{ Ohm} \tag{16}$$

$$B = \frac{0{,}1836}{R}\left(1 + \frac{0{,}81Q}{Q^2 + 4}\right) \text{S} \tag{17}$$

When Q is lowered, the harmonic frequencies should be filtered between *Co* and *R*.

2.3.2.4 Saturation voltage and resistance

Krauss *et al.* (1980:453) give effective voltages for the different transistors. When a BJT is used as a switch, the saturation voltage should be considered. The resulting effective voltage will be:

$$V_{eff} = V_{cc} - V_{sat} \text{ V} \tag{18}$$

V_{eff} should be used in all calculations instead of V_{cc}, except for input power. In the case of a FET (field effect transistor) switch the dissipation due to the resistance R_{on} could be estimated by assuming its effects on the overall circuit operation to be small and integrating over the time period over which the FET is on. The dissipation being $i_S^2(\theta)R_{on}$. For a 50 percent duty cycle this results in an effective voltage of:

$$V_{eff} = \frac{R}{R + 1{,}365R_{on}} V_{DD} \text{ V} \quad \textbf{(19)}$$

2.3.2.5 Transition time

Optimum Class E operation reduces the power dissipated at the moment the switch closes to a negligible level (Krauss *et al.*, 1980:453). The power dissipated in this time can be estimated by assuming a linear decrease in the current through the switch during the time required to complete the transition. This produces a parabolic voltage waveform over capacitor C during this time. Integration of the voltage-current product then yields a dissipated power of:

$$P_{dT} = \frac{1}{12}\theta_S^2 P_o \text{ W} \quad \textbf{(20)}$$

where θ_S is the transition time converted to radians. The efficiency, in the absence of saturation voltage or resistance, is then:

$$\eta = 1 - \frac{1}{12}\theta_S^2 \quad \textbf{(21)}$$

This may be combined with other effects by summing dissipated powers or by multiplying the efficiency given above by that produced by the other effects without transition-time losses.

2.3.2.6 Radio frequency choke value

As a rule of thumb, the reactance of the *RFC* should be at least ten times that of the load.

$$X_{RFC} = 10R \text{ Ohm} \quad \textbf{(22)}$$

For further details on the derivation of formulae, refer to the thesis by Pienaar (2002:51-66).

2.4 Summary

This chapter gave the choices of amplifiers available. Class E appears to be the best solution specifically because of the combination of high efficiency and simple circuit layout.

Detail concerning the theory and formulae necessary to design a Class E amplifier were given in this chapter to provide a thorough understanding of the Class E amplifier concept in preparation for the actual design of the amplifier in the chapter to follow.

Chapter 3 Design of the modulated Class E amplifier

In this chapter the design of the modulated Class E amplifier is discussed. The design of each of the various Class E stages is given in detail. These stages are simulated by using Simetrix 4.1 software. The modulation process of the Class E amplifier is also designed and simulated.

Figure 12 shows a block diagram of the various design stages. These are:

- Switch (Mosfet) and the carrier generator (Mosfet driver) combination
- Class E amplifier
- Harmonic filter
- Modulation process

The rest of the chapter will discuss the above mentioned stages.

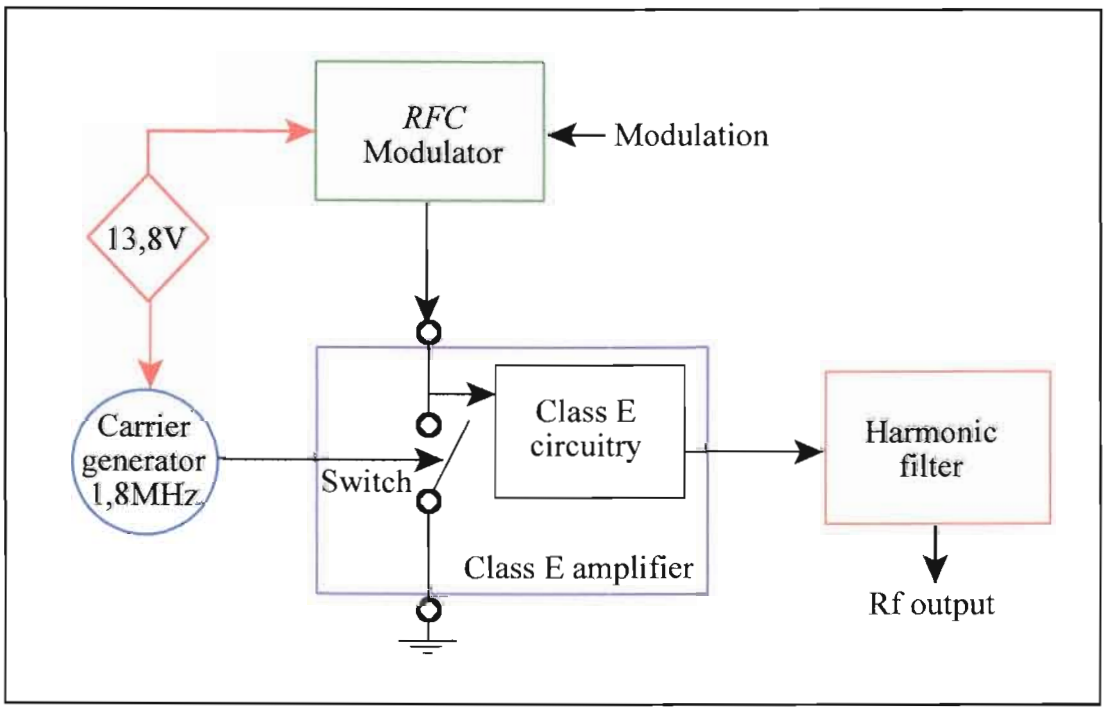

Figure 12 Block diagram of the modulated Class E amplifier

3.1 The switch and the carrier generator combination

The carrier generator will drive the Mosfet used to operate as a switch. Thus, it is important for the two elements to function as a unit, since the characteristics of the one will influence the other. The following will receive attention in this section:

- Carrier generator (Mosfet driver)
- The switching Mosfet

3.1.1 The carrier generator

In Mosfet terms, the carrier generator is generally known as a Mosfet driver. As part of the research, various options were looked into. The first option was to build a simple Mosfet driver, and the second to use a dedicated integrated circuit (IC) Mosfet driver.

To test the different Mosfet drivers, the commonly available IRFP250 Mosfet was used.

3.1.1.1 Simple Mosfet drivers

Three different options were tested:

- Micro power phase-locked loop
- Hex Schmitt Trigger
- Hex Schmitt Trigger driving into a buffer

Micro power phase-locked loop

The HCF4046BE is a micropower phase-locked loop IC available with an internal voltage controlled oscillator (VCO). This VCO can be used on its own. Typically the range of the operating frequency is up to 1.4 MHz according to the datasheet (see

Annexure B).

Figure 13 gives the functional diagram from the IC's datasheet which gives the functionality of the different pins. To use the IC as a VCO, the pins are connected as shown in Table 3.

Table 3 VCO connections for HCF4046BE

Pin	Application	Connection
4	output	Mosfet gate
5	inhibit	ground
6 & 7	frequency range	C1
8	Vss	ground
9	variable DC input to vary frequency output	DC voltage
11	frequency range	R1 to ground
16	V_{DD}	supply voltage

By manipulating R1 and C1 in Figure 13, it is possible to reach a frequency output well beyond 1,8 MHz. However, this setup proved not to work. The VCO output failed to drive the Mosfet. The output voltage was pulled to ground and no square wave was visible at all.

In this exercise an IRFP250 Mosfet was used with an input capacitance is 2,8 nF (Annexure I gives the datasheet for IRFP250 in detail).

If the input reactance of the Mosfet is calculated, the current requirement for the IRFP250 Mosfet can be determined. For an operating frequency of 1,8 MHz and an input capacitance of 2,8 nF, the following calculations can be made:

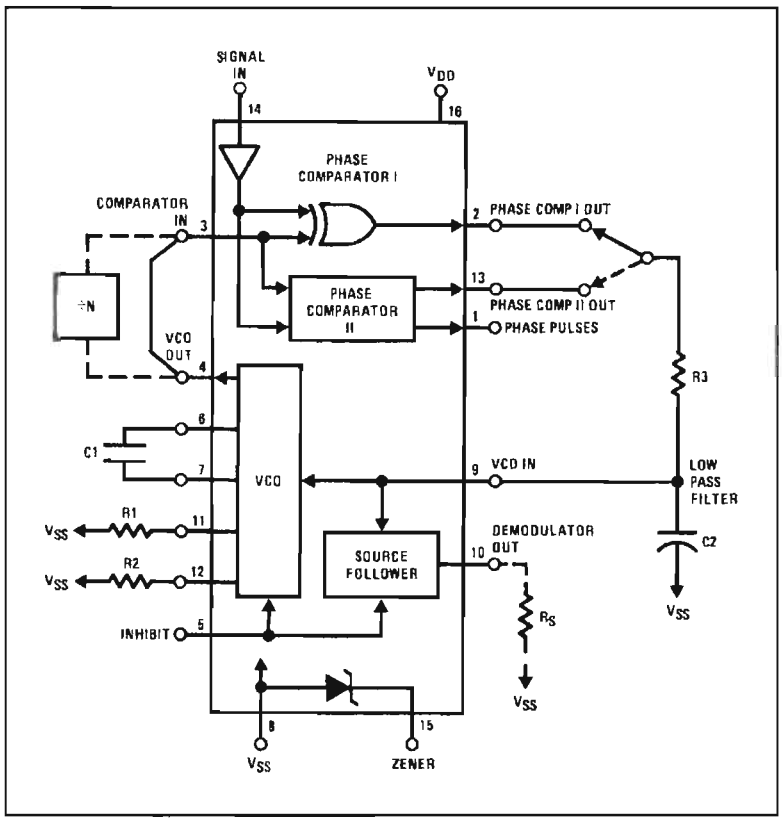

Figure 13 HCF4046B functional diagram (STMicroelectronics, 2001:5)

$$Xc = \frac{1}{2\pi fC}$$

$$= \frac{1}{2\pi 1{,}8 \times 10^{6} \times 2{,}8 \times 10^{-9}}$$

$$= 31{,}578 \text{ Ohm}$$

$$I = \frac{V}{R}$$

$$= \frac{10}{31{,}578}$$

$$= 316{,}673 \text{ mA}$$

The maximum source and drain current the VCO can supply is just below 1 mA, while the Mosfet requires 316,673 mA, clearly showing that this configuration will not be able to drive the Mosfet.

Hex Schmitt Trigger

The CD40106BC Hex Schmitt Trigger is a monolithic complementary MOS IC constructed with N and P-channel enhancement transistors. Figure 14 shows the internal layout and the connection diagram of the IC.

To generate an oscillating frequency of 1,8 MHz, a 100 pF capacitor can be connected to pin 13 to ground and a variable 10 kOhm resistor can be connected between pin 13 and 12. Pin 12 will also become the oscillator output. In order to increase the current capability the output of pin 12 can be connected to the inputs of the remaining triggers. The outputs of the remaining triggers can be combined so that there are five in parallel. This is to increase the current sourcing and draining capability.

The typical current sourcing and draining of each trigger are 8,8 mA for a 15 V supply voltage (see the datasheet in Annexure J). Since there are five triggers in parallel this

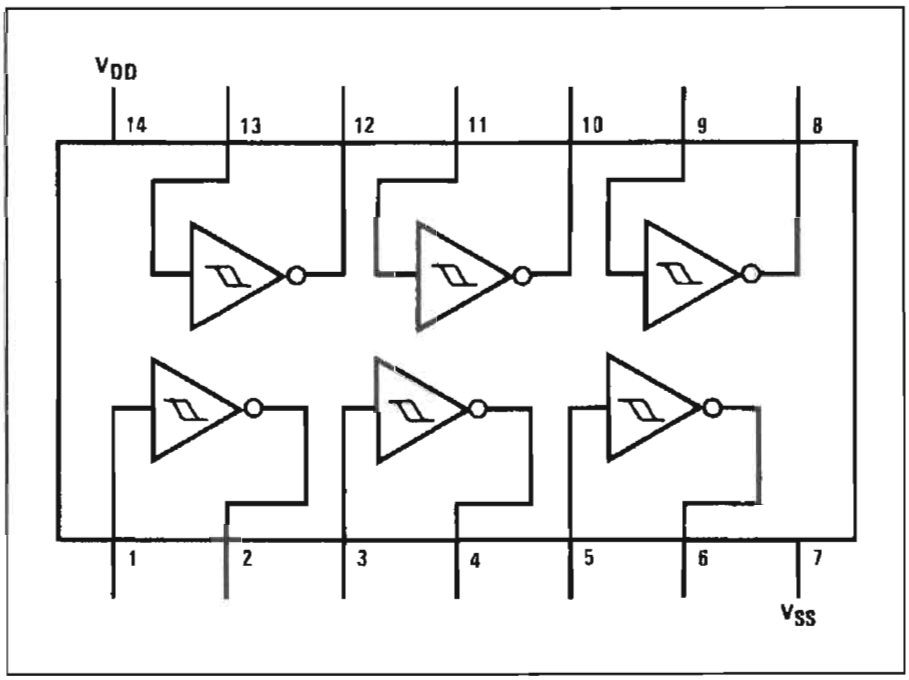

Figure 14 CD40106BC internal layout and connection diagram (Fairchild Semiconductor Corporation, 1987:1)

value will increase to a total current of 44 mA. The previously calculated current input requirement of 316,673 mA for the IRFP250 will increase to 475 mA for a 15 V supply. This is more than 10 times what the CD40106BC can deliver.

However this option will not work well enough, due to current shortage. Another drawback is that the square wave becomes noisy because of the parallel network of five triggers.

Hex Schmitt Trigger driving into a buffer

To create a buffer circuit which is fed from the CD40106BC's output, two transistors are used, one NPN and one PNP. These are used in a circuit as shown in Figure 15.

The NPN transistor is a BD139 and its PNP complement is a BD140. These are power transistors which are capable of maximum collector currents of 1,5 A and 2 A respectively. Both these transistors can handle transition frequencies up to 160 MHz. Concerning the collector-emitter voltages, both can handle up to 80 V. For more information on these two transistors, see Annexure K.

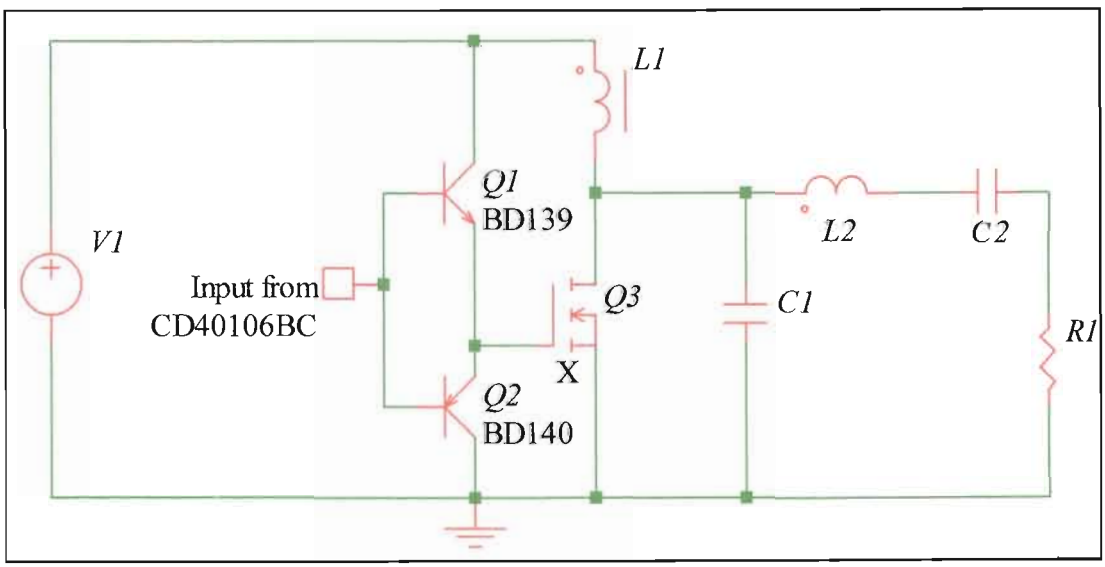

Figure 15 Buffer Mosfet driver circuit

Although these transistors are more than capable of supplying the necessary voltage and current to the Mosfet, the voltage drops too much on the gate of the Mosfet, so that it is too low to drive the Mosfet as a switch. The square wave output to the Mosfet's gate input is deformed to such an extent that the operating frequency generated by the CD40106BC is affected.

3.1.1.2 Dedicated Mosfet driver ICs

There are several of these Mosfet driver ICs available on the market. To mention a few:

- EL7182C: Two phase, high speed driver
- EL7457C: 40 MHz Non-inverting quad CMOS driver
- ICL7667: Dual Mosfet driver
- IR2125: Current limiting single channel driver
- IR4426: Dual low side driver
- MC34151: High speed dual Mosfet driver
- TC4421: 9 A high-speed Mosfet driver

Experiments were conducted on: IR2125, MC34151 and TC4421.

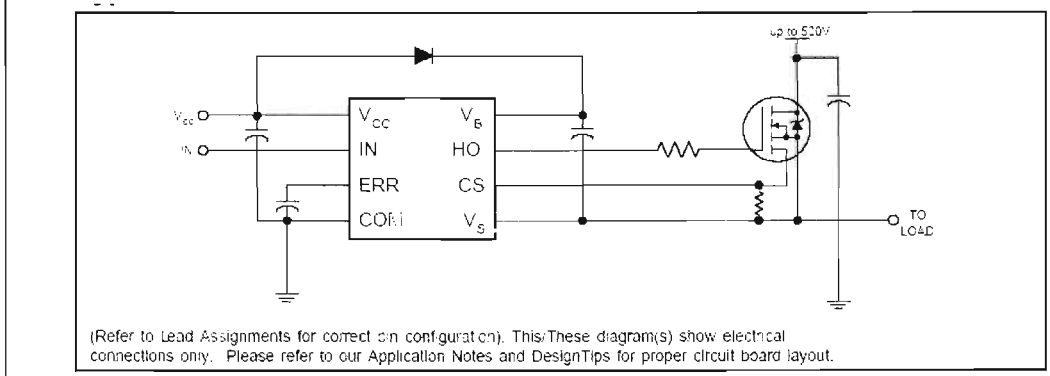

Figure 16 Typical connection diagram for IR2125 (International Rectifier, 2004:1)

IR2125: Current limiting single channel driver

This is a gate driver with a gate supply range of 12 V to 18 V. The output current is between one and two amperes. The datasheet in Annexure L give more information. Figure 16 gives the typical connection diagram, but the connection done for the Class E amplifier is somewhat different, because a Mosfet is used. This driver did not manage to drive the IRFP250 Mosfet successfully. A possibile reason could be that the impedance matching between the driver and Mosfet is problematic.

MC34151: High speed dual Mosfet driver

This driver has the following advantageous specifications stated in the datasheet (see Annexure M):

- Two independent channels with 1,5 A totem pole output each. See Figure 17 for pin connections.

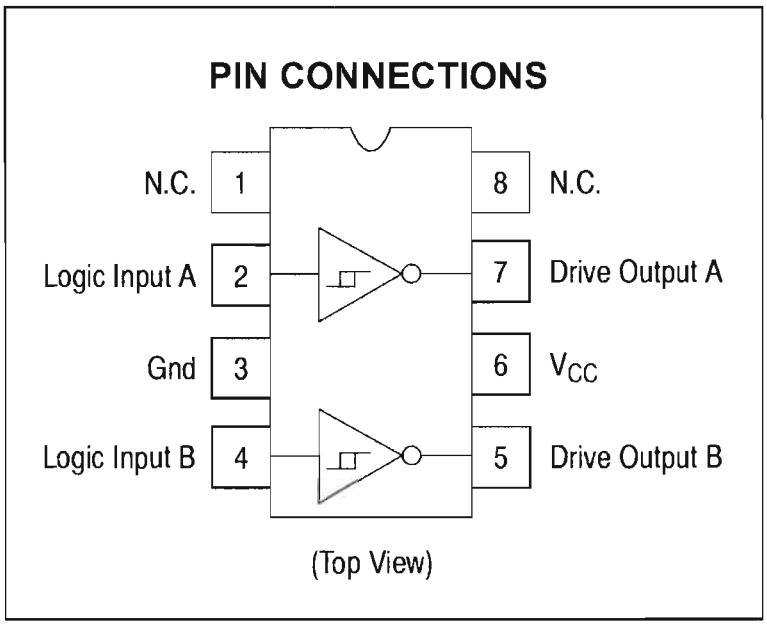

Figure 17 MC34151 pin connections (On Semiconductor, 2004:1)

- Output rise and fall times of 15ns with 1000 pF load
- Efficient high frequency operation.

From the above it can be seen that the speed and current supply to the Mosfet is sufficient. According to the graphs in the datasheet, an operating frequency of 2.9 MHz can easily be obtained. For this Class E application we need only 1,8 MHz.

Since it is a cheap option of only R19, it was tried without success.

TC4421: 9 A high-speed Mosfet driver

This driver has the following advantageous features:

- High peak output current of 9 A.
- Continuous output current of 2 A.
- Fast rise and fall times of 30 ns for 4700 pF
- Low output impedance.
- It can handle more than 1 A inductive current forced back into its outputs.
- All terminals are fully protected against up to 4 kV of electrostatic discharge.

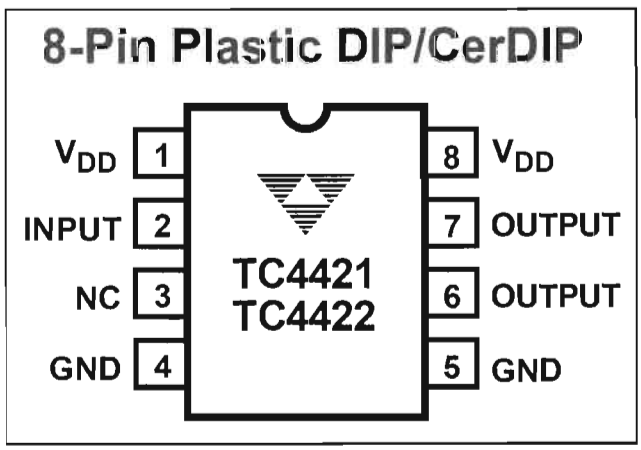

Figure 18 Pin configuration for TC4421 (Telcom Semiconductor, Inc, 1996:4-231)

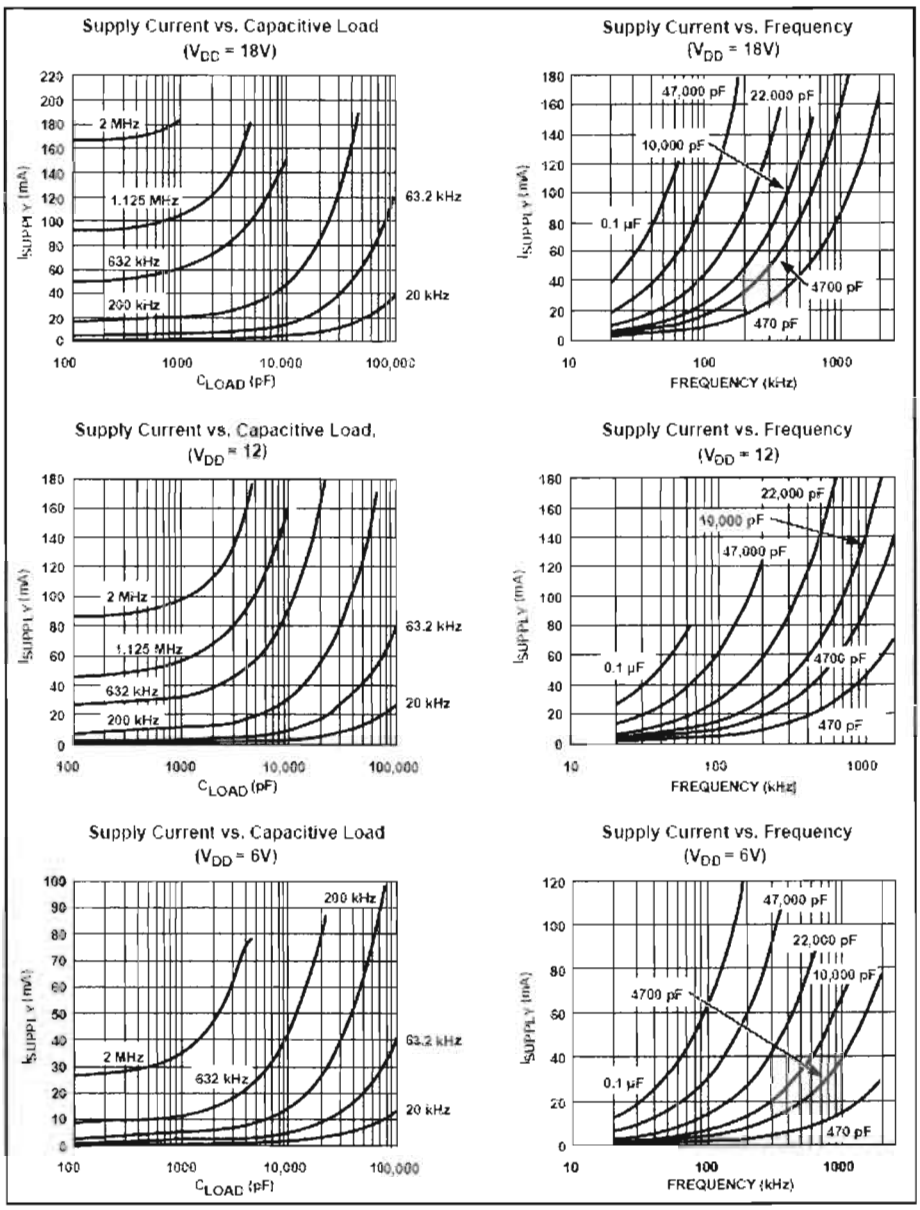

Figure 19 TC4421 current graphs
(Telcom Semiconductor, Inc, 1996:4-235)

The datasheet in Annexure C provides the pin configuration for Figure 18. This IC is successful in driving the IRFP250 Mosfet. The VCO configuration of the HCF4046BE is used to drive the input on pin two.

For the initial connection, the supply voltage used, was 13, 8 V which was the same as the supply to the Class E amplifier circuit. The TC4421 IC reached very high working

temperatures so that it was only possible to use it for very short periods. The first TC4421 was lost due to overheating which lead to an in depth look into the characteristics of the TC4421.

Since heat is the problem with the usage of the TC4421, the graphs depicting the current will be discussed (Figure 19). From these graphs it is clear that the following factors influence the supply current:

- The higher the capacitive load (Mosfet gate input capacitance) the higher the supply current.
- When the operating frequency is increased, the supply current increases as well.
- A lower supply voltage to the TC4421 will reduce the supply current.

Of the three above mentioned influences, two can be changed:

- The capacitive load can be reduced by using another Mosfet with a lower input capacitance.
- A voltage regulator can be used to supply the TC4421 with a supply voltage lower than that of the rest of the circuit.

The Supply Current versus Capacitive Load graph for a 6 V supply voltage (Figure 19) indicates that the needed 1,8 MHz at 2800 pF just makes the specification.

3.1.2 The switching Mosfet

The various options for switches for Class E amplifiers were researched by Pienaar (2002:78-85). The Mosfet was chosen as a switch for the following reasons:

- The output capacitance of the Mosfet can be used by the Class E amplifier

characteristics.

- Mosfets are low in price and readily available.
- In an application of a switch, it has no gain-bandwidth product.

The Mosfet used in the Class E amplifier is an important part of the design since it has an effect on the calculations seen in chapter two and changes the effective voltage as seen in equations (18) and (19). An important element for Class E amplification is the shunt capacitor *C1* of Figure 8. The switch's internal output capacitance, *Ci* in Figure 8, will also have a parallel effect on this capacitor.

The commonly available IRFP250 Mosfet was used for the initial tests. A Mosfet with lower input capacitance is needed to control the heat problem when used with the TC4421 Mosfet driver. The Mosfet chosen was the IRF540N. This Mosfet has a lower input capacitance of 1400 pF, although it still has good specifications for the Class E amplifier (these specifications and more are available in Annexure D). Table 4 compares the specifications found in the datasheets of IRFP250 to the IRF540N Mosfets.

Table 4 IRFP250 versus IRF540N

Characteristic	IRFP250	IRF540N
Drain to source breakdown voltage	200 V	100 V
Static drain to source on resistance	0,085 Ohm	0,052 Ohm
Maximum drain current	30 A	33 A
Maximum operating temperature	175°C	175°C
Switching	fast	fast
Fully avalanche rated	yes	yes
Input capacitance	2800 pF	1400 pF
Output capacitance	780 pF	330 pF

Thus, for an input capacitance of 1400 pF and a 6 V supply voltage to the TC4421, the supply current to the TC4421 is reduced to only 40 mA (Figure 19).

Additionally, a heatsink can be added to the TC4421 to further control the heat.

3.2 Design of the Class E rf amplifier

The purpose of this research project is to design and build an amplitude modulated, low power, Class E transmitter, in the Radio Amateur frequency range. The frequency chosen as such is 1,8 MHz.

The power for Class E transmitters relies very much on the DC supply as seen in equation (9). In order to keep the focus on AM and Class E, a readily available supply voltage of 12-13,8 V, will be used. This will result in an optimum power output of 2.198 W using equation (9).

Since the research is done for the use by commercial broadcasters and radio amateurs, the design will be a standard 50 ohm load resistance.

A practical Q factor of five will be chosen for the design. Since this will allow harmonic currents through to the load, an additional filter to the load will be designed to cater for these unwanted frequencies.

The switch which will be used is an IRF540N with an internal capacitance (*Ci* in Figure 8) of 330 pF (see the datasheet in Annexure D).

3.2.1 Calculation of component values

The formulae discussed in section 2.3.2 will be used to calculate the various elements of the Class E amplifier (Figure 8).

- The power output, using equation (9) is:

$$P_o = 0{,}577\frac{V_{cc}^2}{R}$$
$$= 0{,}577\frac{13{,}8^2}{50}$$
$$= 2{,}198 \text{ W}$$

- Input current, using equation (10) is:

$$I_{dc} = \frac{V_{cc}}{1{,}734R}$$
$$= \frac{13.8}{1{,}734 \times 50}$$
$$= 0{,}159 \text{ A}$$

- Peak voltage over capacitor C using equation (11) is:

$$V_c = 3{,}56V_{cc}$$
$$= 49{,}128 \text{ V}$$

- Peak current through the switch, using equation (12) is:

$$I_s = 2{,}86I_{dc}$$
$$= 2{,}86 \times 0{,}159$$
$$= 0{,}455 \text{ A}$$

- Susceptance of the shunt capacitor C for a $Q < \infty$, using equation (17) is:

$$B = \frac{0{,}1836}{R}\left(1 + \frac{0{,}81Q}{Q^2 + 4}\right)$$
$$= \frac{0{,}1836}{50}\left(1 + \frac{0{,}81 \times 5}{5^2 + 4}\right)$$
$$= 4{,}185 \text{ mS}$$

$$X_C = \frac{1}{B}$$
$$= \frac{1}{4{,}185 \times 10^{-3}}$$
$$= 238{,}959 \text{ Ohm}$$

$$C = \frac{1}{2\pi f X_C}$$
$$= \frac{1}{2\pi 1{,}8 \times 10^6 \times 238{,}959}$$
$$= 370{,}019 \text{ pF}$$

C1 in Figure 8 is the difference between *C* in Figure 10 and *Ci* in Figure 8:

$$C1 = C - Ci$$
$$= 370{,}019 \times 10^{-12} - 330 \times 10^{-12}$$
$$= 40{,}019 \text{ pF}$$

- Calculation of the inductor *Lo* (Figure 8) involves the use of equation (16) to determine X_{LD} (the reactance of the detune inductor) which in turn requires the calculation of X_L from the ideally tuned circuit (Figure 10) by the use of equation (14):

$$X_{LD} = \frac{1{,}110Q}{Q - 0{,}67} R$$
$$= \frac{1{,}11 \times 5}{5 - 0{,}67} 50$$
$$= 64{,}088 \text{ Ohm}$$

$$\omega L = QR$$
$$X_L = QR$$
$$= 5 \times 50$$
$$= 250 \text{ Ohm}$$

X_{Lo} can be calculated as the sum of X_L and X_{LD}

$$X_{Lo} = X_L + X_{LD}$$
$$= 250 + 64{,}088$$
$$= 314{,}088 \text{ Ohm}$$

$$L_o = \frac{X_{Lo}}{2\pi f}$$
$$= \frac{314{,}088}{2\pi 1{,}8 \times 10^6}$$
$$= 27{,}771 \text{ mH}$$

- *Co* can be calculated from equation (15):

$$Q = \frac{1}{\omega C_o R}$$

$$C_o = \frac{1}{Q\omega R}$$
$$= \frac{1}{5 \times 2\pi 1{,}8 \times 10^6 \times 50}$$
$$= 353{,}678 \text{ pF}$$

- The value of *RFC* according to equation (22) is:

$$X_{RFC} = 10R$$
$$= 10 \times 50$$
$$= 250 \text{ Ohm}$$

$$RFC = \frac{X_{RFC}}{2\pi f}$$
$$= \frac{500}{2\pi 1{,}8 \times 10^6}$$
$$= 44{,}210 \text{ mH}$$

A summary of the Class E amplifier's characteristics for the preceding calculations is given in Table 5. The calculated results are given in Table 6.

Table 5 Class E amplifier design characteristics

Characteristic	Symbol	Value
Operating frequency	f_c	1,8 MHz
DC voltage	V_{dc}	13,8 V
Load resistance	R	50 Ohm
Q factor	Q	5
Mosfet internal capacitance	Ci	330 pF

Note that the internal capacitance of the Mosfet as indicated in Figure 8, is also known as the output capacitance of the Mosfet, as it is expressed on the IRF540N Mosfet's datasheet.

A new circuit can be created by using the characteristics in Table 5 and the calculated results in Table 6 . This circuit of the Class E amplifier is shown in Figure 20.

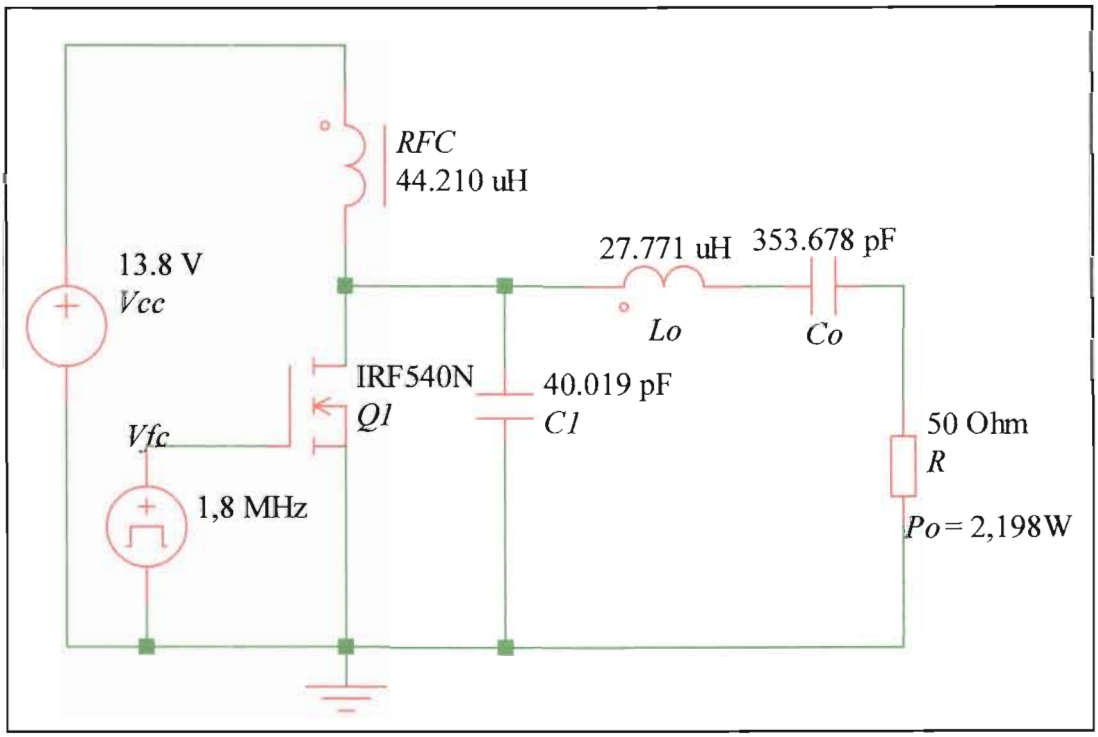

Figure 20 Class E amplifier with designed component values

Table 6 Calculated results for the Class E design

Element	Symbol	Value
Power output	P_o	2,198 W
Peak voltage over C	V_c	49,128 V
Input current	I_{dc}	0,159 A
Peak current through switch	I_S	0,455 A
Parallel capacitor	*C1*	40,019 pF
Series tuned inductor	*Lo*	27,771 uH
Series tuned capacitor	*Co*	353,678 pF
RF choke	*RFC*	44,210 uH

3.2.2 Concrete component values

For these values to be used on a printed circuit board (PCB) the actual values and component sizes of the components in Figure 20 have to be determined.

3.2.2.1 *Vcc* voltage supply

This is a 13,8 V direct current voltage supply. This will not form part of the circuit, but will be an external supply. For testing purposes a variable supply will be used that makes it possible to set it exactly to 13,8 V.

3.2.2.2 Carrier generator

As discussed in sections 3.1.1 and 3.1.2 the TC4421 Mosfet driver will be used. The HCF4046BE will be used as a VCO to generate the square wave at 1,8 MHz for the TC4421. The final circuit configuration, as prepared with the Eagle 4.09 software package, can be seen in Figure 21. The additional components were derived from the

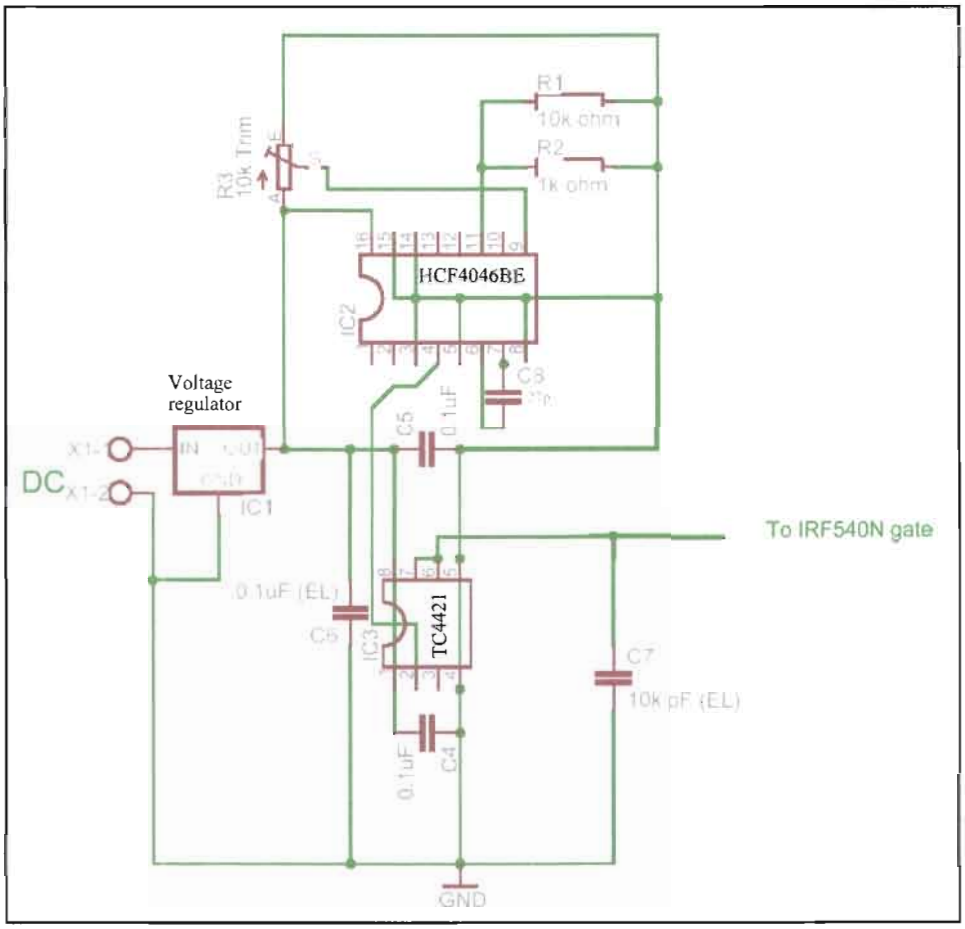

Figure 21 Carrier generator circuit configuration

guidelines in the datasheets in Annexures B and C.

A voltage regulator is connected to the main circuit supply which feeds the Class E amplifier. This is a low voltage regulator, 8 V, to keep the current in the TC4421 manageable.

The HCF4046BE (VCO) supply connection (pin 16) is connected to the voltage regulator output, while ground is connected to pins eight (the ground connection), three, five, 14 and 15. The additional connections to ground are unused pins and are connected for added stability. The parallel resistance of R1 and R2 results in 9 kOhm and is connected to pin 11, which, together with C8 with a value of 27 pF over pins six and seven, give a range of more than 2 MHz. This frequency can be tuned to the desired

value by using R3, which is a variable resistor used as a voltage divider. The resultant voltage is connected to pin nine (Figure 13).

The output of the VCO is directly connected to the TC4421 Mosfet driver. The supply voltage is commonly connected to pins one and eight, while ground is connected to four and five. All these dual points are connected for stability. Three capacitors of 0,1 uF are added for stability between ground and supply at pins one and four, five and eight and general supply and ground. Pin six and seven should also be combined as the output. C7, a 10 000 pF capacitor, is added for a smoother output driving square wave.

3.2.2.3 Radio frequency choke

According to equation (22) the reactance of the *RFC* shown in Figure 20, should be 10 times the load resistance, which results in an inductance of 44,210 uH.

Krauss *et al.* (1980:127) charted a rough guide for coil inductance versus resonant frequencies of the capacitive effect between turns in a coil. In this chart 1,8 MHz will resonate with an inductance between 600 uH and 4 mH. The use of frequencies above this resonant frequency should be prevented because the impedance will become capacitive.

The *RFC* should not be capacitive. The design of the *RFC* will be covered under the section on modulation because it forms part of a transformer for modulation purposes.

3.2.2.4 Mosfet

The Mosfet chosen was the IRF540N with a TO-220 casing on which it is easy to attach a heatsink. Although during normal operation the IRF540N will not produce heat, the heatsink is a built in safety aspect in case the carrier generator goes faulty.

3.2.2.5 Capacitors

The peak voltage over the shunt capacitor, *C1* in Figure 20, is 49,128 V with a calculated capacitance of 40,019 pF (Table 6). However a voltage rating of 100 V and a value of 39 pF were used for *C1* since the values are close enough.

For the series tuned capacitor, *Co*, a value of 353,678 pF was calculated. To obtain a value close to this, the following capacitors will be used in parallel: 0,18 nF, 0,1 nF, 68 pF and 10 pF. This will result in an actual value of 358 pF.

Another option is to install a 0,330 nF capacitor with a 50 pF variable capacitor. This can be tuned to 353,678 pF or it can be tuned according to performance to make up for the deviation in value of the series coil and other effects. To calculate the voltage rating, Hughes (1987:194) gives the equation:

$$Q = \frac{\text{voltage across } L \text{ or } C}{\text{Supply voltage}} \qquad \textbf{(23)}$$

$$\text{votage across } C = 5 \times 13{,}8$$

$$= 69 \text{ V}$$

Thus, a voltage rating of 100 V for the capacitors used for *Co* should be chosen.

3.2.2.6 Inductor *Lo*

Such coils are not commercially available. Each coil has to be hand made to obtain the required designed inductance. Calculation of the approximate inductance of a single-layer air-core coil can be done using equation (24) (Johns, 1997:6):

$$L = \frac{d^2 n^2}{18d + 40l} \qquad \textbf{(24)}$$

The definition and units of the symbols in equation (24) are given in Table 7.

Table 7 Defining equation (24)

Symbol	Definition	Unit
L	inductance of the coil	micro-Henry
d	coil diameter (wire centre to wire centre)	inches
l	coil length	inches
n	number of turns	-

The inductance needed for *Lo* is 27,77 uH. If we use a diameter of 2,032 cm (0,8 inch) for the coil and we make it 5,08 cm (2 inch) long then we can calculate the number of turns from equation (24).

$$L = \frac{d^2 n^2}{18d + 40l}$$

$$27{,}77 = \frac{0{,}8^2 n^2}{18 \times 0{,}8 + 40 \times 2}$$

$$n = 64 \text{ turns}$$

In this case wire with 0,65 mm in diameter should be used. The 64 turns will result in a length of 41,6 mm without spaces between the windings. The coil must be 50,8 mm long, which means the remainder of the length, 9,2 mm should be equally distributed among the 64 turns.

Achieving even distribution of the gaps can sometimes be troublesome. To eliminate these spaces, a new equation (25) can be derived. This equation can give the length of the coil in terms of the thickness of the wire. If the thickness of the wire, w, is given in millimetres then the new equation (25) can be represented as:

$$L = \frac{d^2 n^2}{18d + 40\frac{w}{25{,}4}n} \text{ uH} \qquad \textbf{(25)}$$

Using the same values as before, which was an inductance of 27,77 uH, a diameter for

the coil of 0,8 inches and wire with a diameter of 0,65 mm then equation (25) can be simplified to:

$$d^2n^2 - 1{,}575wnL - 18dL = 0$$

$$0{,}64n^2 - 28{,}426n - 399{,}888 = 0$$

$$\therefore n = 55.644$$

$$\approx 56 \text{ turns}$$

This result in a coil length of 56 times 0,65, which is 36,4 mm. Thus, the final choice of the *Lo* inductor will have the following characteristics:

- Approximately 20 mm in diameter
- Air wound coil
- 0,65 mm diameter wire
- 27,77 uH
- 56 turns without space between the turns
- Resultant length of 36,4 mm

3.2.2.7 Load *R*

The load in practice must be a 50 ohm antenna. For testing purposes it will either be a 50 ohm input port on a communications analyser or a 50 ohm dummy load.

The load voltage can be calculated from equation (8):

$$Vom = 1{,}074Vcc$$

$$= 1{,}074 \times 13.8$$

$$= 14{,}821 \text{ V}$$

Since the output current and voltage are in phase the peak load current can be calculated as:

$$Iom = \frac{V_{om}}{R}$$
$$= \frac{14,82}{50}$$
$$= 296,4 \text{ mA}$$

3.3 Harmonic filter

The Q factor of the *Lo-Co* series resonant circuit in Figure 20 has a designed Q factor of five. For practical reasons the Q factor is chosen to be between three and ten as noted by Krauss *et al.* (1980:452) and explained in section 2.3.2.3. If the Q had an infinite high value, no harmonic currents will flow past *Lo-Co*. In this design it is not the case. To prevent these harmonic currents from reaching the load, a low pass harmonic filter has to be included between the *Lo-Co* series resonant circuit and the load. The filter must pass the 1,8 MHz carrier frequency to the load and filter out the resultant harmonic frequencies.

Williams and Taylor (1995:2.1) state that frequency response is the most common specified requirement to characterize a filter's performance. The major categories of low pass filter responses are:

- Butterworth
- Chebyshev
- Linear phase
- Transitional
- Synchronously tuned
- Elliptic-function

With the exception of the elliptic-function family, these responses are all normalized to a three decibel (dB) cutoff of 1 rad/s. These are all-pole networks. There are three very important aspects when designing filters, namely:

- Frequency scaling factor (*FSF*)
- Steepness factor (A_S)
- Low pass normalization

Williams and Taylor (1995:2.2) give the definition for the *FSF*:

$$FSF = \frac{\text{desired reference frequency}}{\text{existing reference frequency}} = \frac{2\pi f \text{ rad/s}}{1 \text{ rad/s}} \quad \textbf{(26)}$$

Scaling of frequency and impedance is normally performed in one combined step rather than being performed sequentially. The denormalized values are then given by (Williams & Taylor, 1995:2.5):

$$R' = R \times Z \quad \textbf{(27)}$$

$$L' = \frac{L \times Z}{FSF} \quad \textbf{(28)}$$

$$C' = \frac{C}{FSF \times Z} \quad \textbf{(29)}$$

The first step according to Williams and Taylor (1995:2.5) in selecting a normalized design is to convert the requirement into a steepness factor, using equation (30):

$$A_S = \frac{fs}{fc} \quad \textbf{(30)}$$

where *fs* is the frequency which has the minimum required stopband attenuation and *fc* is the limiting frequency of the cutoff of the passband, usually the 3 dB point.

3.3.1 All-pole networks

The All-pole networks were the first trial for a low pass filter. The operating frequency was 1,8 MHz which gave a first harmonic of 3,6 MHz. The design for the filter will be for the attenuation at 3,6 MHz, although further down the spectrum, the attenuation will

increase to infinite rejection at the extremes of the stopband (Williams & Taylor, 1995:2.71). For the 3 dB, 1rad/s point, a frequency of 2 MHz was chosen to achieve a low attenuation at 1,8 MHz. The circuit is designed for a 50 ohm load, thus the impedance into and from the filter should be 50 ohm. To summarize the requirements:

- *LC* low pass filter
- 3 dB at 2 MHz
- 30 dB at 3,6 MHz
- Source impedance (R_S) = load impedance (R_L) = 50 Ohm
- A_S = ?
- (*FSF*) = ?

The reason for limiting the design to 30 dB attenuation was to keep the filter simple for the initial test. From equation (30) we can calculate the steepness factor:

$$A_S = \frac{f_S}{f_C}$$
$$= \frac{3,6}{2}$$
$$= 1,8$$

and from equation (26) we have *FSF* as:

$$FSF = \frac{2\pi f \text{ rad/s}}{1 \text{ rad/s}}$$
$$= 2\pi 2,4 \times 10^6$$
$$= 1,508 \times 10^7$$

The attenuation characteristics of Butterworth and Chebyshev filters, provided by Williams and Taylor (1995:2.37 & 2.46) are listed in Annexure E for comparison. For a steepness factor of 1,8, the Butterworth filter will be of the seventh order, while for the Chebyshev filter with 0,1 dB ripple, it will be of the fifth order.

Since the building of the fifth order filter is less complicated, that will be the choice. The normalized filter can be obtained by using the table for 0,1 dB Chebyshev *LC* element values from Williams and Taylor (1995:11.27 - 11.28). The corresponding circuit is shown in Figure 22 and the normalized values are given in Table 8.

Table 8 Normalized values (Williams and Taylor, 1995:11.28)

Element	Value
RS	1 Ohm
C1	1,3013 F
L2	1,5559 H
C3	2,2411 F
L4	1,5559 H
C5	1,3013 F
RL	1 Ohm

With the information gathered, using equations (27), (28) and (29) the denormalized values can be calculated:

$$\begin{aligned} R'S &= R \times Z \\ &= 1 \times 50 \\ &= 50 \text{ Ohm} \\ &= R'L \end{aligned}$$

$$\begin{aligned} C'1 &= \frac{C1}{FSF \times Z} \\ &= \frac{1{,}3013}{1{,}257 \times 10^{7} \times 50} \\ &= 2{,}071 \text{ nF} \\ &= C'5 \end{aligned}$$

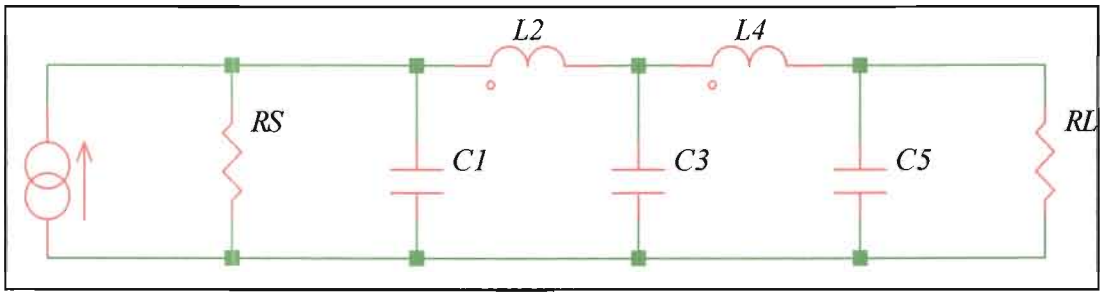

Figure 22 Normalized Chebyshev filter

$$C'3 = \frac{C3}{FSF \times Z}$$

$$= \frac{2{,}2411}{1{,}257 \times 10^{7} \times 50}$$

$$= 3{,}567 \text{ nF}$$

$$L'2 = \frac{L2 \times Z}{FSF}$$

$$= \frac{1{,}5559 \times 50}{1{,}257 \times 10^{7}}$$

$$= 6{,}191 \ \mu\text{H}$$

$$= L'4$$

With these actual calculated component values, the resultant denormalized Chebyshev filter circuit is presented in Figure 23.

When this filter was tested on the bench, it only gave 10 dB attenuation at 3,6 MHz, instead of the designed 30 dB attenuation. This shows this type of filter will need a very

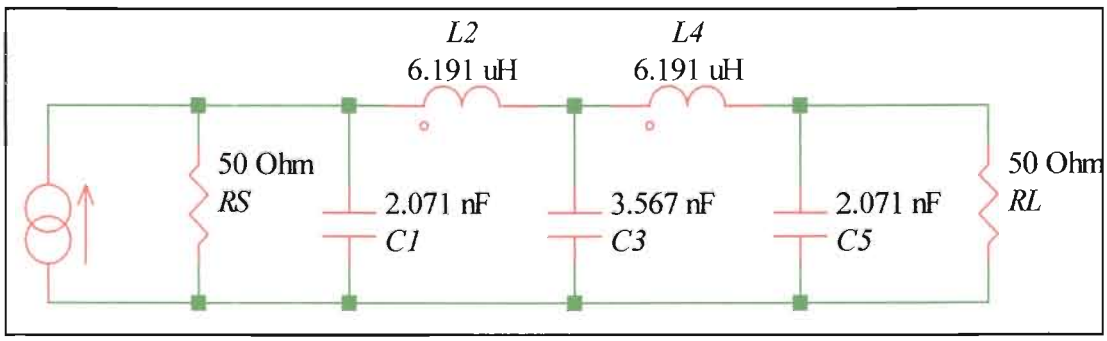

Figure 23 Denormalized Chebyshev filter

high order for the attainment of the desired 60 dB attenuation at the 3,6 MHz harmonic. According to the graphs given by Williams and Taylor (1995:2.37) the Butterworth filter will be more than a tenth order, which is not catered for. The Chebyshev filter would require at least an eighth order filter (Williams and Taylor, 1995:2.46), provided the filter behaves according to the design.

3.3.2 Elliptic-function filter

These filters are not part of the all-pole network filters. Elliptic-function filters have zeros as well as poles at finite frequencies. Finite transmission zeros in the stopband reduce the transition region so that extremely sharp roll-off characteristics can be obtained. The introduction of these transmission zeros allows the steepest rate of descent theoretically possible for a given number of poles (Williams and Taylor, 1995:2.71).

The response in the passband is similar to that of Chebyshev filters except that the attenuation at 1rad/s is equal to the passband ripple instead of 3 dB. Improved performance is obtained at the expense of return lobes in the stopband. Elliptic-function filters are more complex than all-pole networks. There are a few definitions which are needed when designing an Elliptic-function filter. These are explained in Figure 24 by the use of a low pass filter, and definitions are given in Table 9.

The requirements for designing an Elliptic-function filter are as follows:

- *LC* low pass filter
- R_{dB} (zero to 2 MHz) = 0,25 dB
- *Amin* = 75 dB @ 3.6 MHz and above
- $R_S = R_L$ = 50 Ohm

Table 9 Elliptic-function filter definitions

Element	Definition
R_{dB}	passband ripple
Amin	minimum stopband attenuation in decibels
Ω_S	lowest stopband frequency at which Amin occurs
θ	modular angle which describes the sharpness of the roll-off, thus the sharper, the less bandwidth is used to obtain Amin
$\Omega_{4,6,2}$	branch resonant frequencies which correspond to the transmission zeros

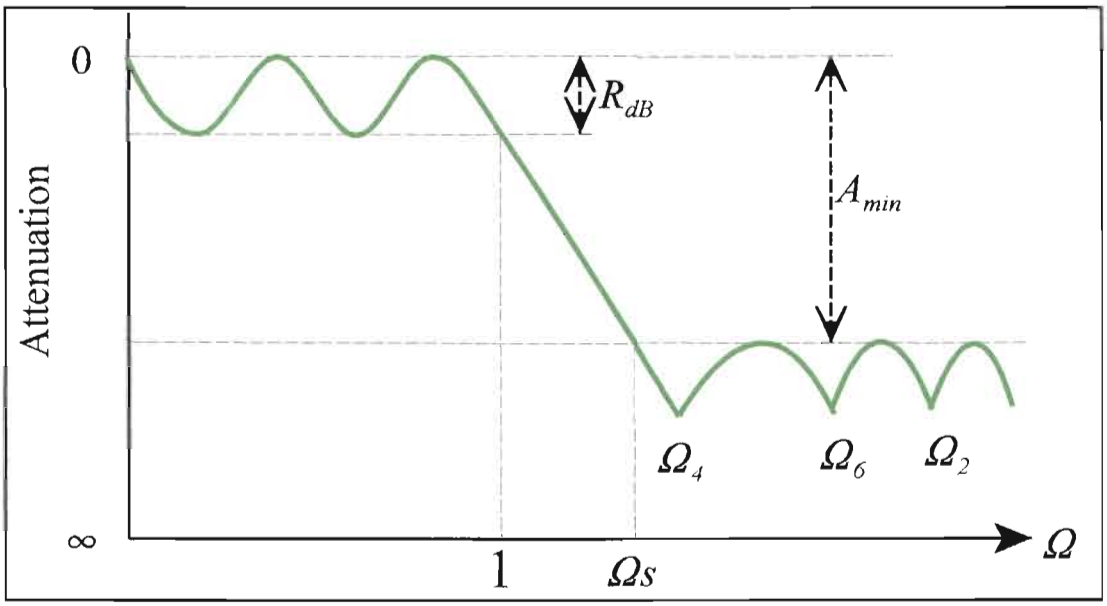

Figure 24 Normalized Elliptic-function low pass response (Williams & Taylor, 1995:3.3)

The low pass steepness factor can be calculated from equation (30):

$$A_S = \frac{f_S}{f_C}$$

$$= \frac{3{,}6}{2}$$

$$= 1{,}8$$

Using Table 10, which is adopted from Williams and Taylor (1995:2.77), a ripple factor of equal or less than 0,25 dB represents a reflection coefficient (ρ) of 20 percent. This table also includes the voltage standing wave ratio *(VSWR)* and the return loss A_ρ of the filter's input impedance and the load or source. Thus a reflection coefficient of 20 percent will result in a return loss of 13,9 dB.

Table 10 ρ versus R_{dB}

ρ	R_{dB}	*VSWR*	A_ρ	**ripple factor**
10 %	0,04365	1,2222	20,0 dB	0,1005
15 %	0,09883	1,3529	16,5 dB	0,1517
20 %	0,1773	1,5000	13,9 dB	0,2041
25 %	0,2803	1,6667	11,7 dB	0,2582
50 %	1,249	3,0000	4,78 dB	0,5774

Figure 25 plots $Amin + A_\rho$ versus Ωs. This is used to determine the order (n) needed for the filter.

Calculation of $Amin + A_\rho$ for use in the graph in Figure 25 gives:

$$A_{min} + A_\rho = 75 + 13{,}9$$
$$= 88{,}9 \text{ dB}$$

The steepness factor $As = 1{,}8 = \Omega s$. When using these values for Ωs and $Amin + A_\rho$ an Elliptic-function filter of the seventh order is needed. The sharpenss is defined by θ. This is illustrated in Annexure F.

The values of the Elliptic-function *LC* element values for the seventh order filter with a 20 percent reflection coefficient and using equal terminations, determined from the table and graph in Annexure F, that will be used in this study are listed in Table 11.

Table 11 Elliptic-function element values

(Williams and Taylor, 1995:11.90)

θ	Ω_s	*Amin*	*C1*	*C2*	*L2*	Ω_2	*C3*
34	1,788292	88,3	1,292	0,0511	1,335	3,829016	2,002
C4	***L4***	Ω_4	***C5***	***C6***	***L6***	Ω_6	***C7***
0,2404	1,247	1,826511	1,916	0,1702	1,204	2,209625	1,184

The normalized seventh order, 20 percent reflection coefficient low pass filter can be seen in Figure 26.

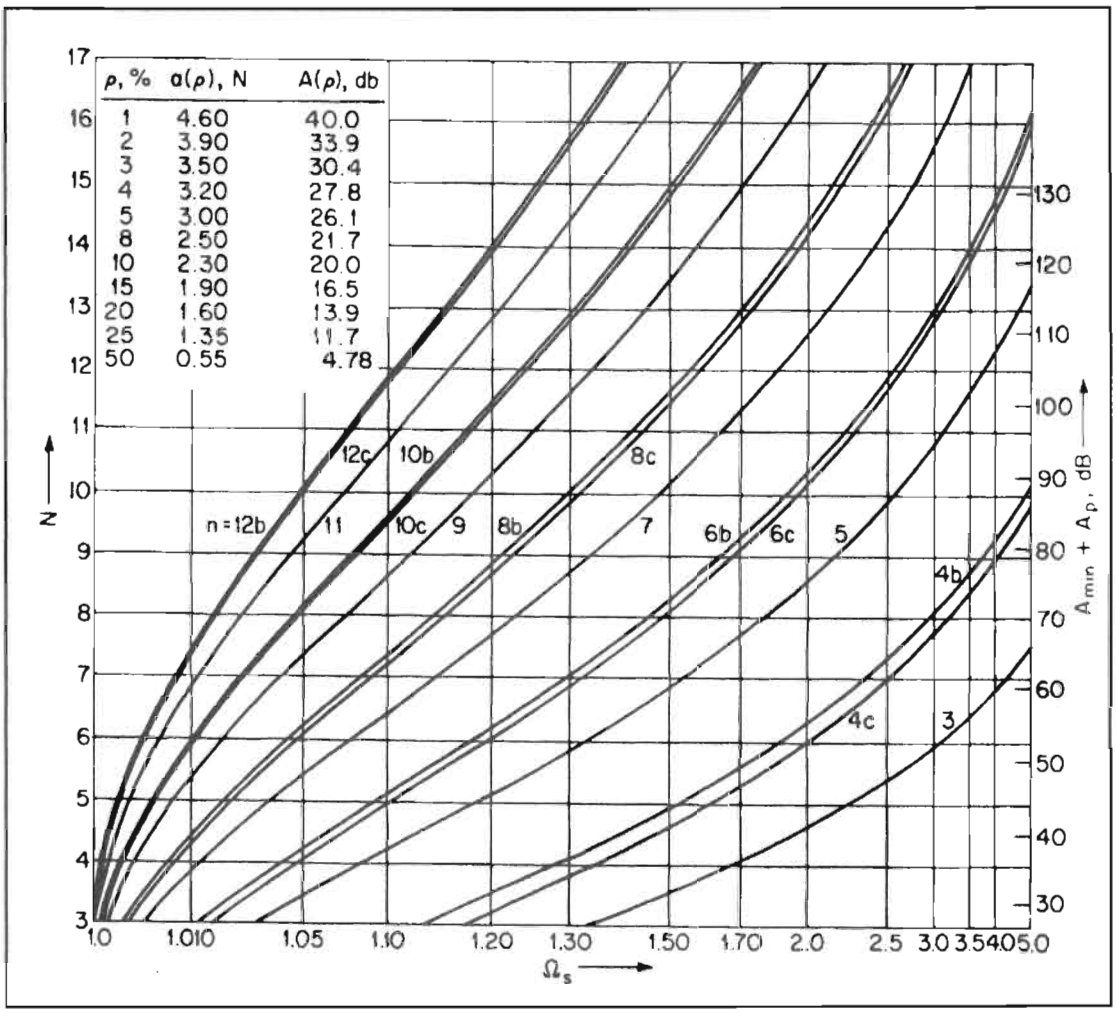

Figure 25 Curves estimating the order of Elliptic-function filters
(Williams and Taylor, 1995:2-80)

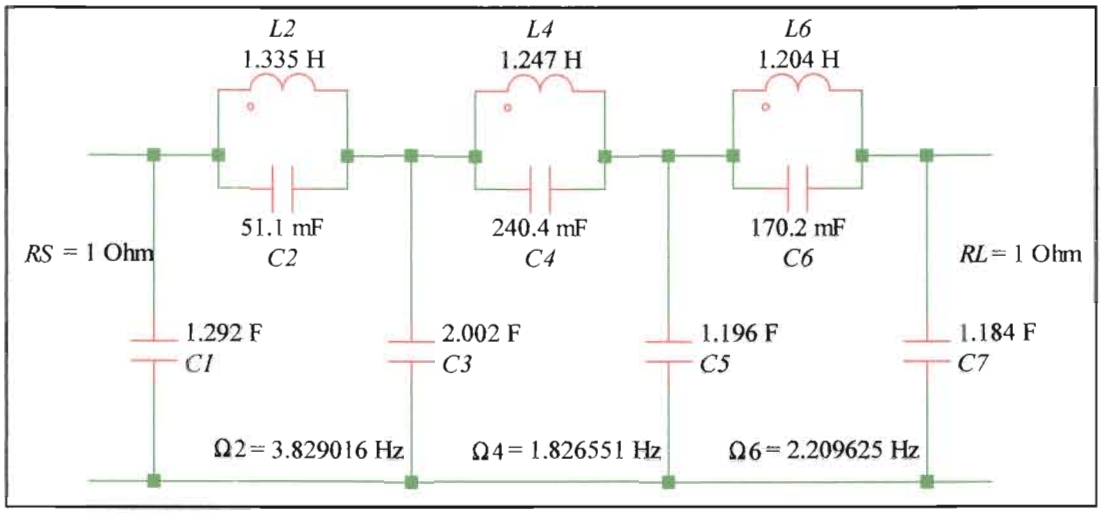

Figure 26 Normalized low pass filter for Table 11

To denormalize the filter we use the $RS = RL = 50$ Ohm. The FSF can be calculated from equation (26):

$$FSF = \frac{2\pi f \text{ rad/s}}{1 \text{ rad/s}}$$

$$= 2\pi 2 \times 10^6$$

$$= 1{,}257 \times 10^7$$

Form equation (29) the capacitor values can be determined:

$$C'1 = \frac{C1}{FSF \times Z}$$

$$= \frac{1{,}292}{1{,}257 \times 10^7 \times 50}$$

$$= 2{,}056 \text{ nF}$$

$C'2 = 81{,}328$ pF

$C'3 = 3{,}186$ nF

$C'4 = 382{,}608$ pF

$C'5 = 3{,}049$ nF

$C'6 = 270{,}882$ pF

$C'7 = 1{,}884$ nF

and from equation (28) the inductor values can be determined as follows:

$$L'2 = \frac{L2 \times Z}{FSF}$$

$$= \frac{1{,}335 \times 50}{1{,}257 \times 10^{7}}$$

$$= 5{,}312 \text{ uH}$$

$$L'4 = 4{,}962 \text{ uH}$$

$$L'6 = 4{,}793 \text{ uH}$$

The resonant frequencies of each parallel tuned circuit can be calculated by multiplying the design cut off frequency by $\Omega 2$, $\Omega 4$ and $\Omega 6$. This gives:

$$f2 = f_c \times \Omega 2$$

$$= 2 \times 10^{6} \times 3{,}829016$$

$$= 7{,}658 \text{ MHz}$$

$$f4 = 3{,}653 \text{ MHz}$$

$$f6 = 4{,}419 \text{ MHz}$$

The resultant denormalized filter is given in Figure 27. The final stage of the filter design is to calculate the actual values which will be used for the physical components. Firstly the inductors' specifications were calculated so that it could be turned. Secondly the capacitor values and ratings were calculated before the capacitors were purchased.

Inductors

As stated in section 3.2.2.6 the coils are hand made. For these coils the following characteristics were used:

- Air wound coil
- $d = 1{,}1$ cm $\approx 0{,}44$"
- 1 mm diameter wire
- No spaces between windings

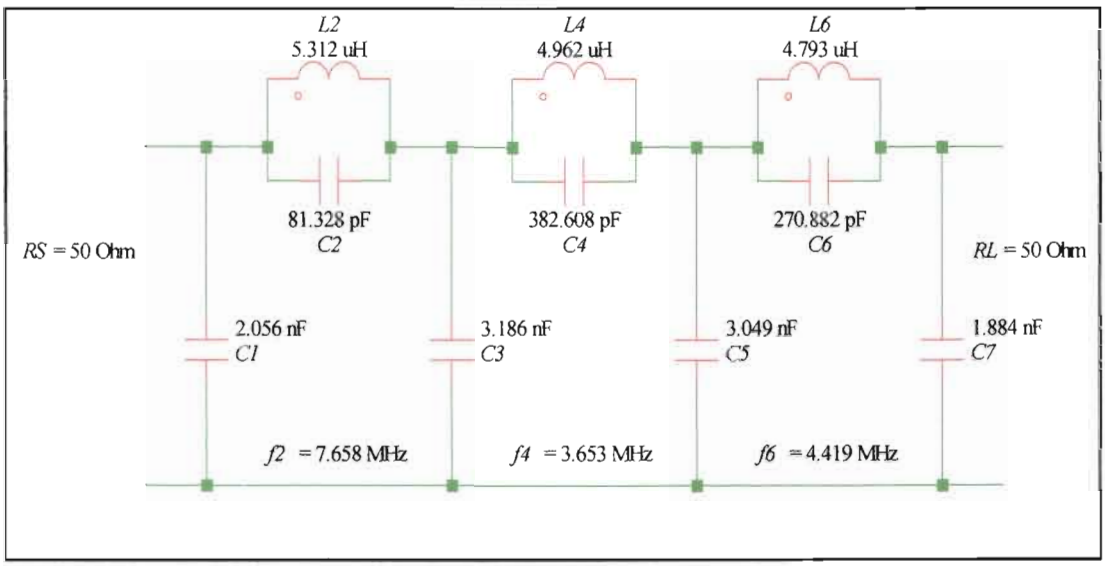

Figure 27 Denormalized Elliptic-function filter

Equation (25) was used to calculate the number of turns for these coils:

$$L_2 = \frac{d^2 n_2^2}{18d + 40\frac{w}{25,4}n_2}$$

$$d^2 n_2^2 - 1,575 w n_2 L_2 - 18dL = 0$$

$$n_2^2 - 1,575\frac{L_2 n_2}{0,44^2} - 18\frac{L_2}{0,44} = 0$$

$$n_2^2 - 1,575\frac{5,312 \times 10^{-6} n_2}{0,44^2} - 18\frac{5,312 \times 10^{-6}}{0,44} = 0$$

$$n_2 = 47,764 \text{ turns}$$

$$n_4 = 44,890 \text{ turns}$$

$$n_6 = 43,500 \text{ turns}$$

These turns were rounded off to 48, 45 and 44 respectively. The length of the coil is calculated by multiplying with the diameter of the wire, which is 1 mm. Thus, the coil lengths will be 48 mm, 45 mm and 44 mm respectively. Table 12 summarizes the actual coil information which were used for the filter.

Table 12 Summarizing the filter coil information

Coil	*L*	*n*	*l*	*w*	*d*
L1	5,312 uH	48	48 mm	1 mm	11 mm
L2	4,962 uH	45	45 mm	1 mm	11 mm
L3	4,793 uH	44	44 mm	1 mm	11 mm

Capacitors

From equation (8) the output voltage was calculated:

$$\begin{aligned} Vom &= 1{,}074Vcc \\ &= 1{,}074 \times 13.8 \\ &= 14{,}821 \text{ V} \end{aligned}$$

The output voltage is supplied to the filter, but resonance is present in the filter, thus 63 V should be sufficient to cater for these resonant voltage peaks.

The closest actual capacitor values are given in Table 13 as well as the respective voltage ratings.

3.4 Class E simulation

Simulations were conducted on the Class E amplifier design that was presented in sections 3.1 to 3.3. This portion was simulated independently before the modulation process was designed for the circuit. These simulations were aimed at proving the design to a certain extent to give reassurance that the design would behave satisfactorily.

The following simulations were done:

- Class E rf amplifier.

- Class E rf amplifier including the harmonic filter.

Table 13 Actual capacitor values

Capacitor	Value	Actual value	Voltage rating
C1	2,056 nF	2 nF	63 V
C2	81,328 pF	82 pF	63 V
C3	3,186 nF	3 nF	63 V
C4	382,608 pF	390 pF	63 V
C5	3,049 nF	3 nF	63 V
C6	270,882 pF	270 pF	63 V
C7	1,884 nF	1,8 nF	63 V

The software simulation package that was used throughout the simulation process was Simetrix 4.1. Since the VCO and Mosfet driver are integrated circuits, these were not part of the simulation, however, the function of the carrier generator was simulated by a voltage generator in Simetrix.

3.4.1 Class E rf amplifier

The circuit as simulated in Simetrix can be seen in Figure 28. As stated in the next section, section 3.5, the modulation is implemented by the use of a transformer. Thus a transformer, of which the primary winding inductance is equal to that of the calculated *RFC*, was used. The high value resistor, *R2* is to prevent current flowing in the transformer's secondary winding. The very low resistor value, *R3*, creates a point to place the current probe.

The following probes were inserted on the circuit:

- *Vcc* - supply voltage

- *Idc* - supply current
- *Is* - current through the Mosfet
- *Vfc* - carrier generator voltage
- *Vc* - voltage over the capacitor *C1*
- *Vo* - output voltage
- *Io* - output current

3.4.1.1 *Vcc*, *Vfc* and *Idc* simulations

The supply voltage is an external connection. This should be adjusted to 13.8 V.

Vfc must be between 4 V and 20 V to switch the Mosfet IRF540N. Appendix D gives the gate to source threshold voltage as 4 V maximum and the absolute maximum rating as 20 V.

In section 2.3.1 it was noted that the *RFC* inductance should be large enough so that the

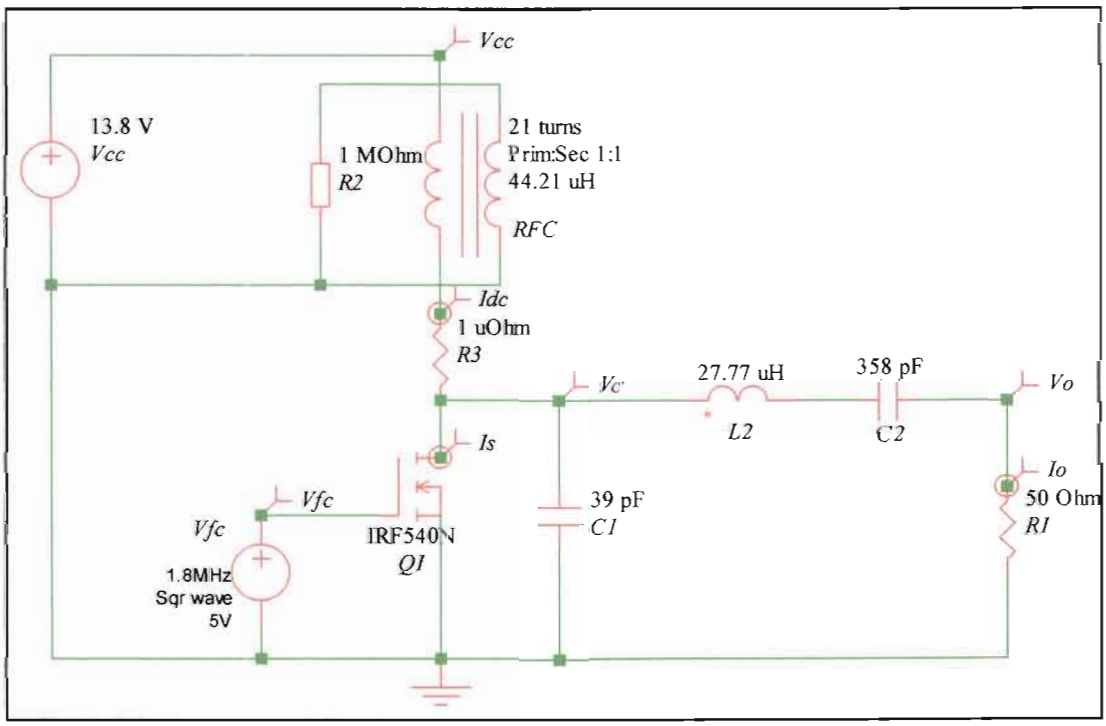

Figure 28 Class E amplifier with 44,21 uH *RFC*

current through it is constant. To see whether this assumption is satisfied by the design, *Vcc*, *Idc* and the *Vfc* was analysed with the simulation of Figure 28. The resultant curves are shown in Figure 29.

The calculated value of *Idc* is 159 mA, a DC value. The graph shows a value of 149,5 mA with an alternating current (AC) component of 38,2 mA at a frequency of 1,8 MHz, which is more than 25 percent of the RMS value. The peak to peak variation of *Idc* is 120,5 mA. Thus, *Idc* in this circuit is far from a pure DC supply. The value for *RFC* can be increased to reduce the AC component of *Idc*. When the *RFC* inductance is increased to 1,8 mH, the following will be affected:

- AC component of *Idc* will decrease to only 851,8 uA
- *Idc* RMS value will also decrease to 120 mA
- as *Idc* decreases, the power output will decrease from 1,902 W to 1,62 W

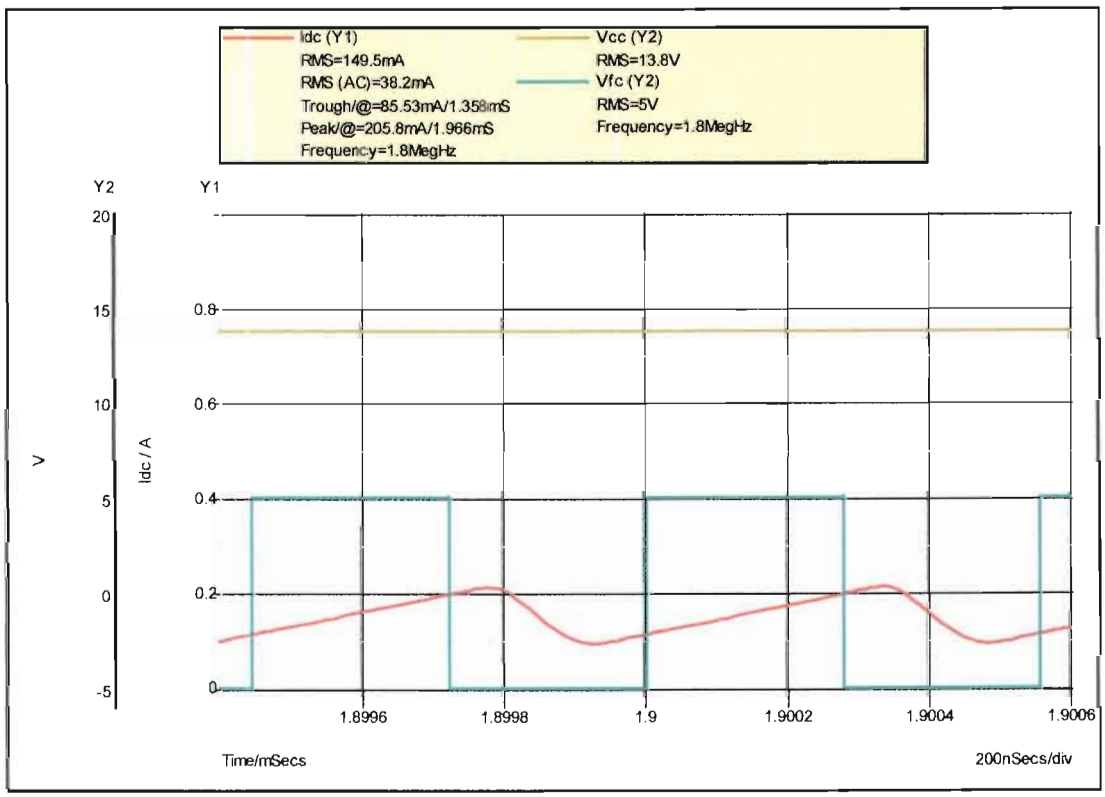

Figure 29 *Vcc*, *Vfc* and *Idc* graphs for Figure 28.

- modulation will be affected as will be seen in the modulation design process

For the simulation of the Class E and harmonic filter, the value of *RFC* was left as is, although it was changed for the modulation purposes.

3.4.1.2 *Vc* and *Is* simulations

In Table 6, the peak values of *Vc* and *Is* are given respectively as 49,128 V and 455 mA. From Figure 30 the simulated peak values for *Vc* and *Is* are 74,17 V and 489,7 mA respectively. If the spike on top of the current waveform is discarded, the peak value for *Is* is 419 mA.

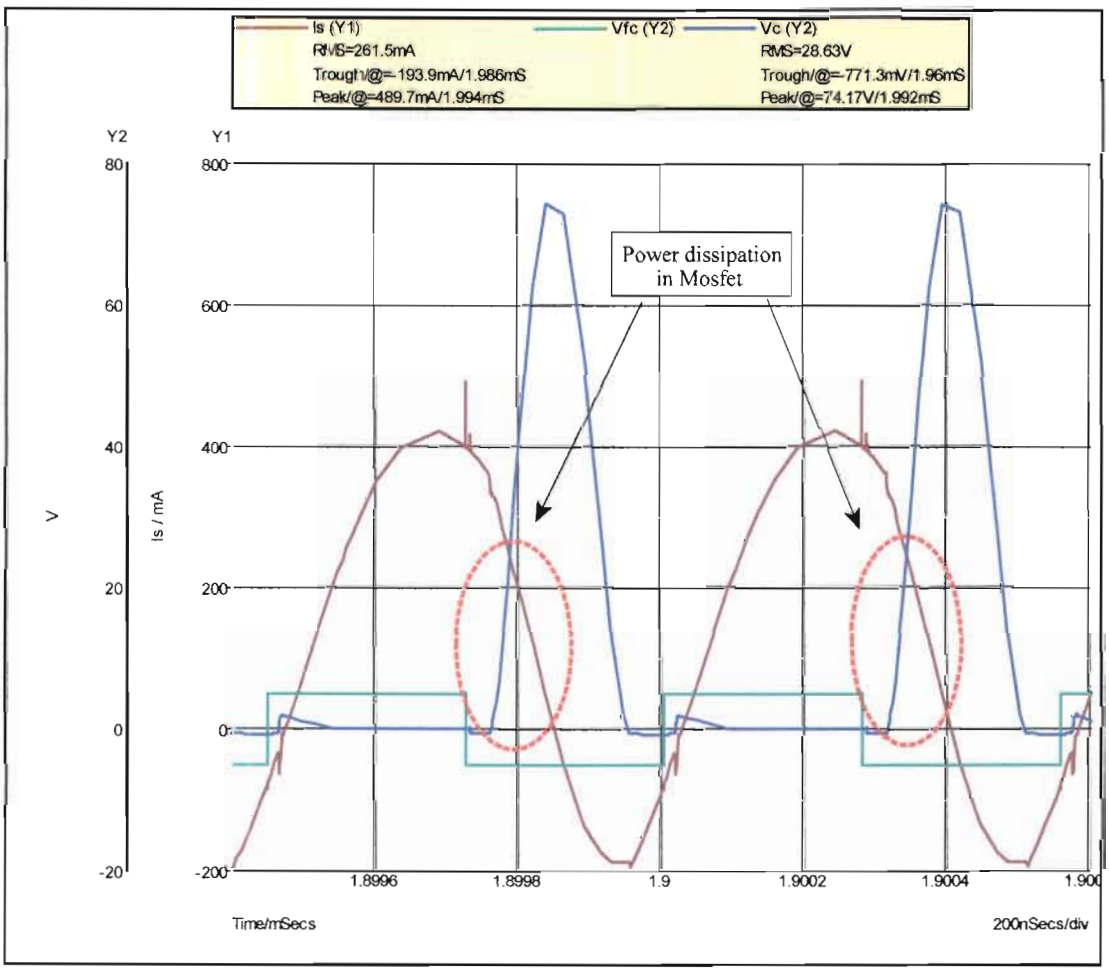

Figure 30 *Vc* and *Is* graphs for Figure 28

In section 2.3.1 it was explained that the switch should be driven in such a way that there can be voltage over it without current, or current flowing through it with no voltage across it. This would result in no power dissipation in the switch. This can be seen in Figure 30 where, when *Vfc* is high (switching the Mosfet on) the current flows through it, and when *Vfc* is low (switching the Mosfet off) the voltage grows over it.

In Figure 30 the red dotted circles indicate the portion of the cycle where the voltage v_c and the current i_s overlap, resulting in power dissipation in the Mosfet. Therefore, it is clear that the waveform for the current through the switch does not change the instant the switch changes state. Furthermore, the current keeps on flowing into the negative, thus changing direction. Pienaar (2002: 96 & 97) gives two reasons why:

- The detune inductor causes the current to keep on flowing after the Mosfet switched off.
- The parasitic diode in the Mosfet is reverse biased during the off period and this causes the negative flow of current due to the varactor effects. If varactor effects are taken into account, the diode acts like a capacitor that charges during the period the switch is off. It is the voltage across capacitor *C1* that charges the "diode capacitor".

Although power dissipation is present in the Mosfet, it is only for a short portion of the cycle. When one of the waves approaches the maximum values, the other is at a zero or low value, which results in high efficiency.

3.4.1.3 *Vo*, *Io* and *Po* simulations

Figure 31 depicts the resultant output waves from the simulation of the circuit depicted in Figure 28. For an easier comparison of the simulations with the calculated values, the results presented in section 3.2.2.7, Table 6 and Figure 31 are summarized in Table 14.

Table 14 Output values

	Calculated			Simulated		
Output	**Peak**	**RMS**	**Mean**	**Peak**	**RMS**	**Mean**
Vo	14,8 V	10,5 V	-	17,3 V	10,8 V	-
Io	296,4 mA	209,6 mA	-	346,3 mA	215 mA	-
Po	-	-	2,2 W			2,3 W

All the RMS values of the simulation compare very well to the calculations as well as the power measurements. The reason for the higher simulated peaks is the asymmetry of *Vo* and *Io*, as seen in the resultant *Po* wave (Figure 31). The mean power output values compare satifactory.

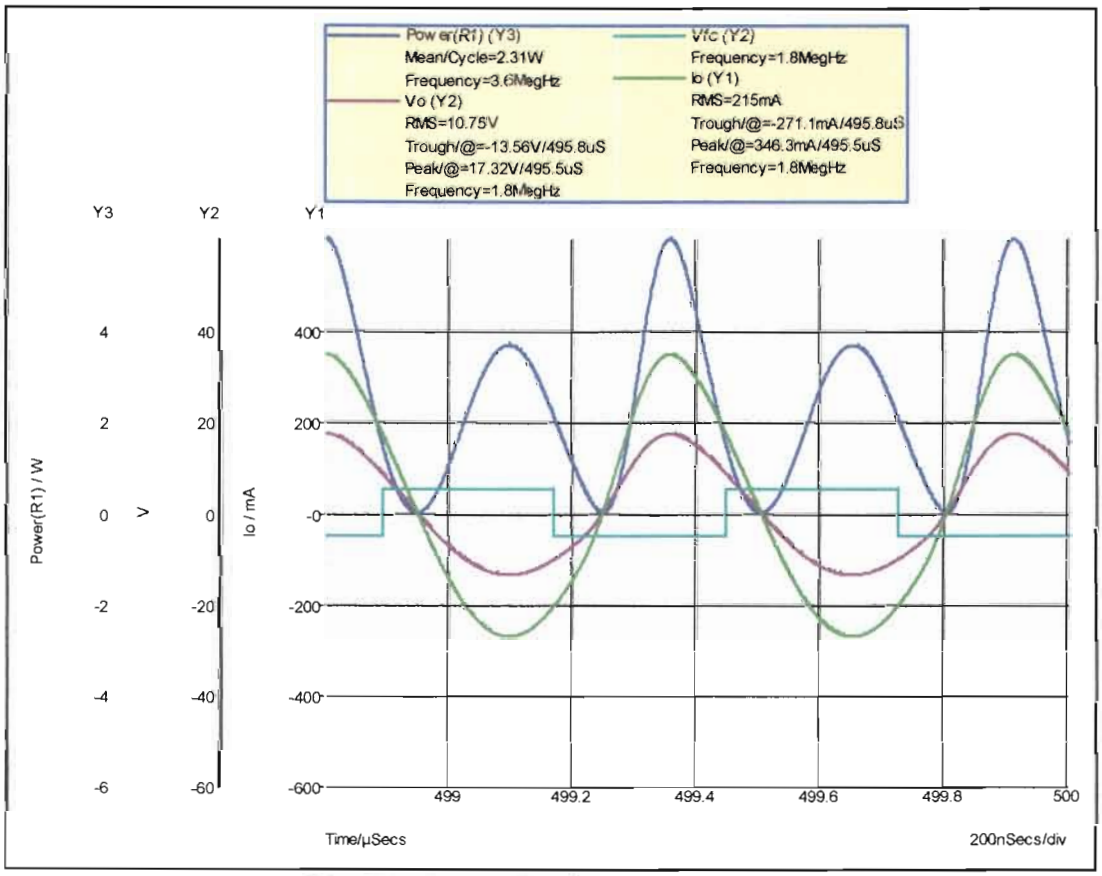

Figure 31 *Vo*, *Io* and *Po* simulations for Figure 28

3.4.2 Harmonic filter simulation

Two aspects were considered when simulating the harmonic filter:

- Effect of the filter on output waves
- Fourier analysis on harmonic frequencies

These simulations were done on the circuit shown in Figure 32, which is basically that of Figure 28, but including the filter.

3.4.2.1 Effect of the harmonic filter on output waves

To determine the effect of the filter on the output waves, *Vo*, *Io* and *Po* in Figure 31, the simulation of the circuit without the filter, was compared to the same elements as those in Figure 33, which depicts the simulated results of the circuit shown in Figure 32. Table 15 summarizes the comparison.

The data in Table 15 shows that, although the peak values are lower, the RMS values

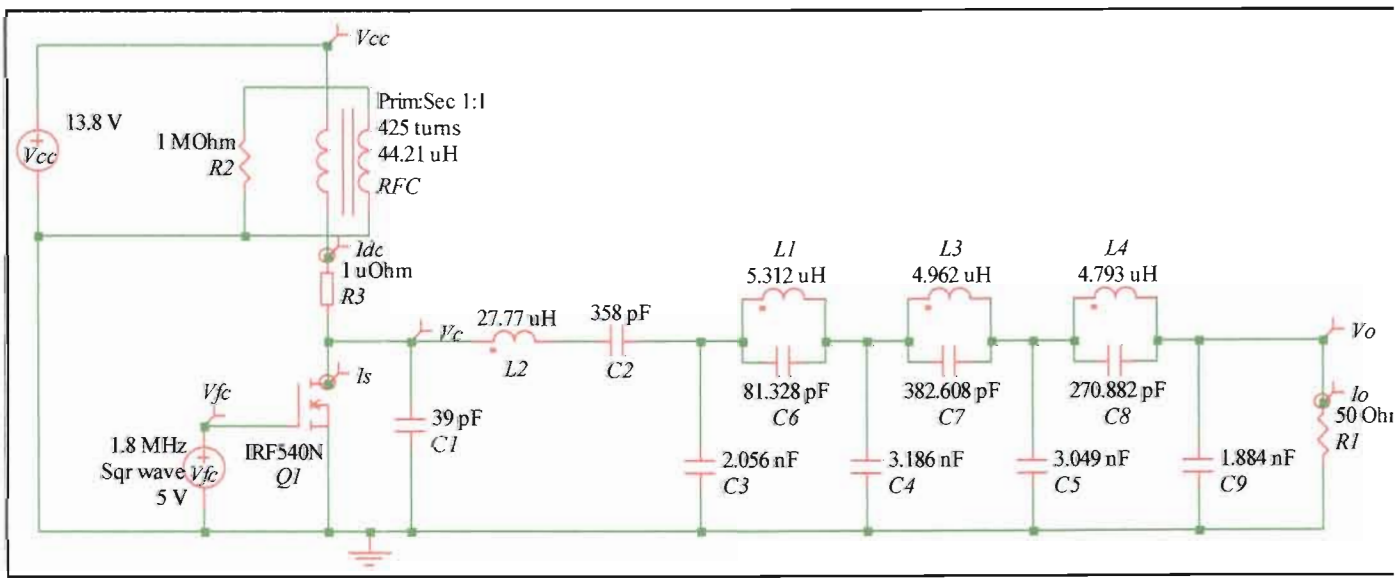

Figure 32 Class E amplifier including harmonic filter

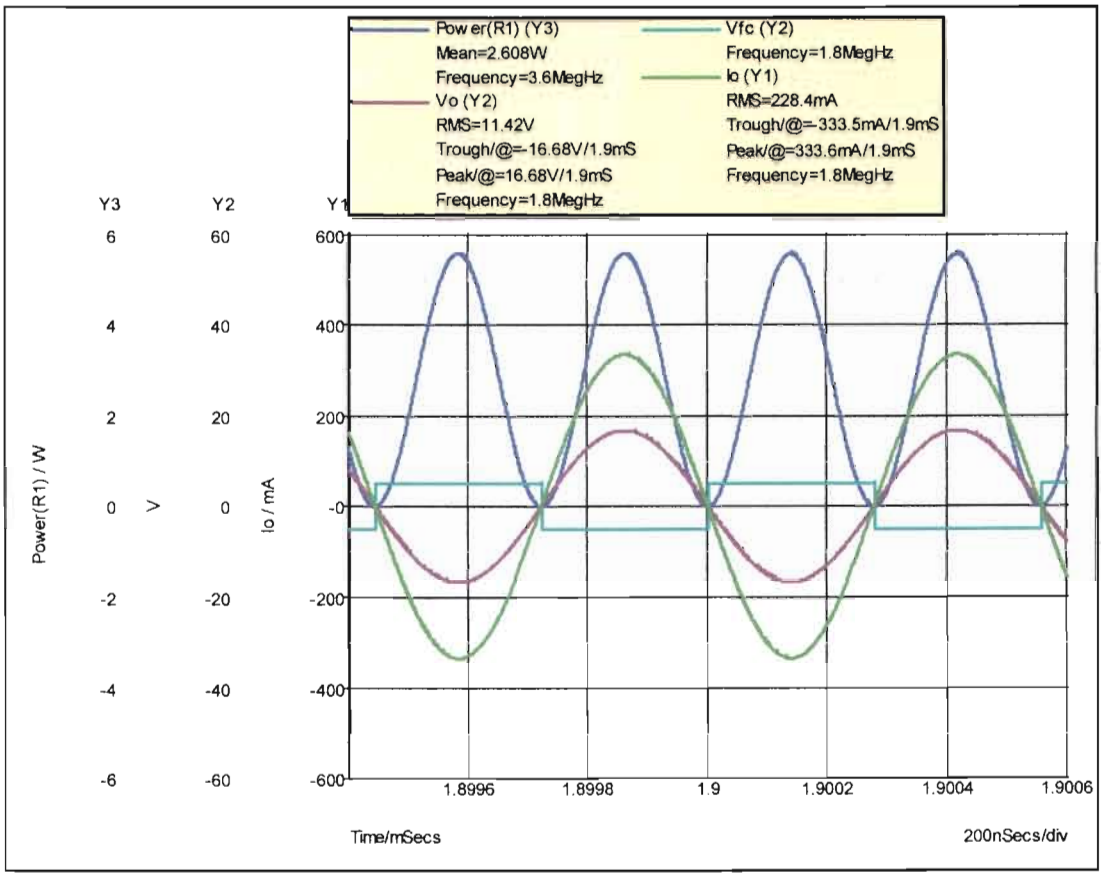

Figure 33 *Vo*, *Io* and *Po* simulations for Figure 32

are higher. This is because *Vo* and *Io* are both very close to being symmetrical waves (Figure 33). Thus a higher and more consistent *Po* value is obtained when Figure 33 is compared to Figure 31. Hence the effect of the harmonic filter on the output waves is to make the waves more symmetrical.

Table 15 Output comparison

	Without filter			With filter		
Output	**Peak**	**RMS**	**Mean**	**Peak**	**RMS**	**Mean**
Vo	17,3 V	10,8 V	-	16,7 V	11,4 V	-
Io	346,3 mA	215 mA	-	333,6 mA	228,4 mA	
Po			2,3 W	-	-	2,6 W

Note that the frequency for the *Po* curve in Figure 31 and Figure 33 is double that of the voltage *Vo* and current *Io* curves. This is due to the $P = VI$ effect of multiplying of two negative values. Thus the fundamental frequency of the carrier (*Vfc*) which is 1,8 MHz, will result in a *Po* frequency of 3,6 MHz.

3.4.2.2 Fourier analysis on harmonic frequencies

To prove that the harmonic filter is functioning according to the design, a Fourier analysis conducted on the waveforms depicted in Figures 28 and 32, and shown in Figures 34 and 35, are compared with each other in Table 16.

To make the comparison easier, the results are given in dBm, which is decibel related to 1 mW. To calculate the power in dBm (P_{dBm}) where P_W is the power measured in Watt, the following equation was used:

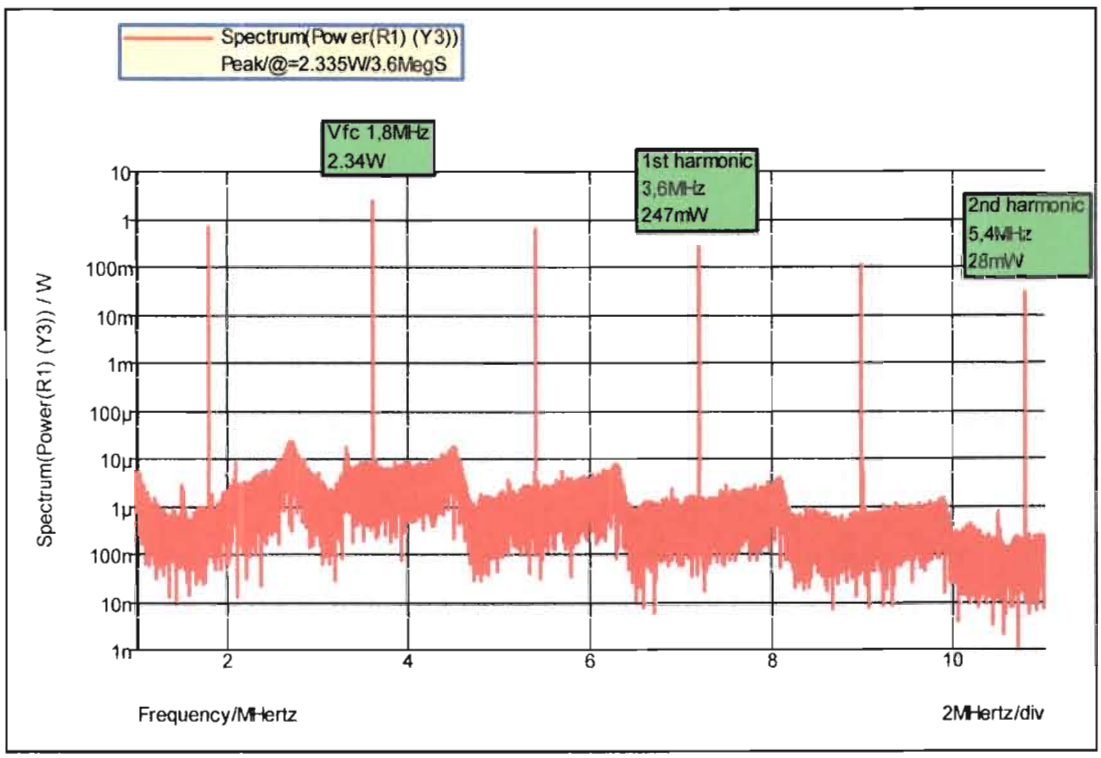

Figure 34 Fourier analysis of the circuit in Figure 28

$$P_{dBm} = 10 \log \frac{P_W}{1mW} \quad (32)$$

In Figure 34 there is a drop of 9,8 dB from the carrier frequency to the first harmonic. From the carrier to the second harmonic there is a drop of 19,2 dB. This attenuation is not sufficient according to the standard. With the harmonic filter installed, Figure 35 displays a drop of 59,2 dB from the carrier frequency to the first harmonic. To the second harmonic the drop is 68,5 dB.

Table 16 Comparison of the Fourier analysis of Figure 34 and Figure 35

Scenario	Carrier frequency *Vfc* = 1,8 MHz	1st harmonic 3,6 MHz	2nd harmonic 5,4 MHz
Without LPF	33,7 dBm	23,9 dBm	14,5 dBm
With LPF	34,4 dBm	-24,8 dBm	-31,1 dBm

The design of the harmonic filter gives a minimum attenuation of 75 dB (see section

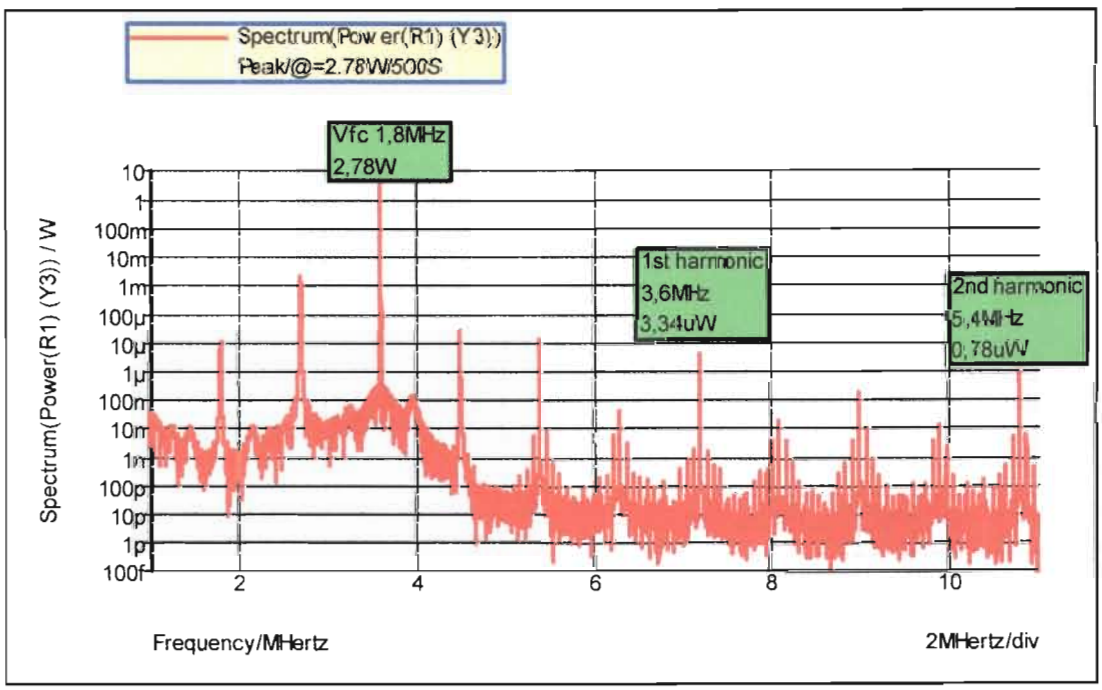

Figure 35 Fourier analysis of the circuit in Figure 32

3.3.2), which is 15.8 dB short. Usually only 60 dB attenuation is prescribed, to which the 59,2 dB compares very well.

3.5 Modulation of the Class E amplifier

As stated in chapter one, only Amplitude Modulation with double side band and full carrier wave will be considered, also known as double side band full carrier (DSBFC). Figure 36 shows a typical oscilloscope view of an amplitude modulated carrier. Where V_{cr} is the carrier voltage and V_m the modulation voltage.

General AM theory was applied in the modulation design process of the Class E amplifier. This theory is well known by most radio engineering enthusiasts. Although the theory was used for the design, it does not form part of the scope of work and was not dealt with in the text. Nevertheless the AM theory, is presented in Annexure H.

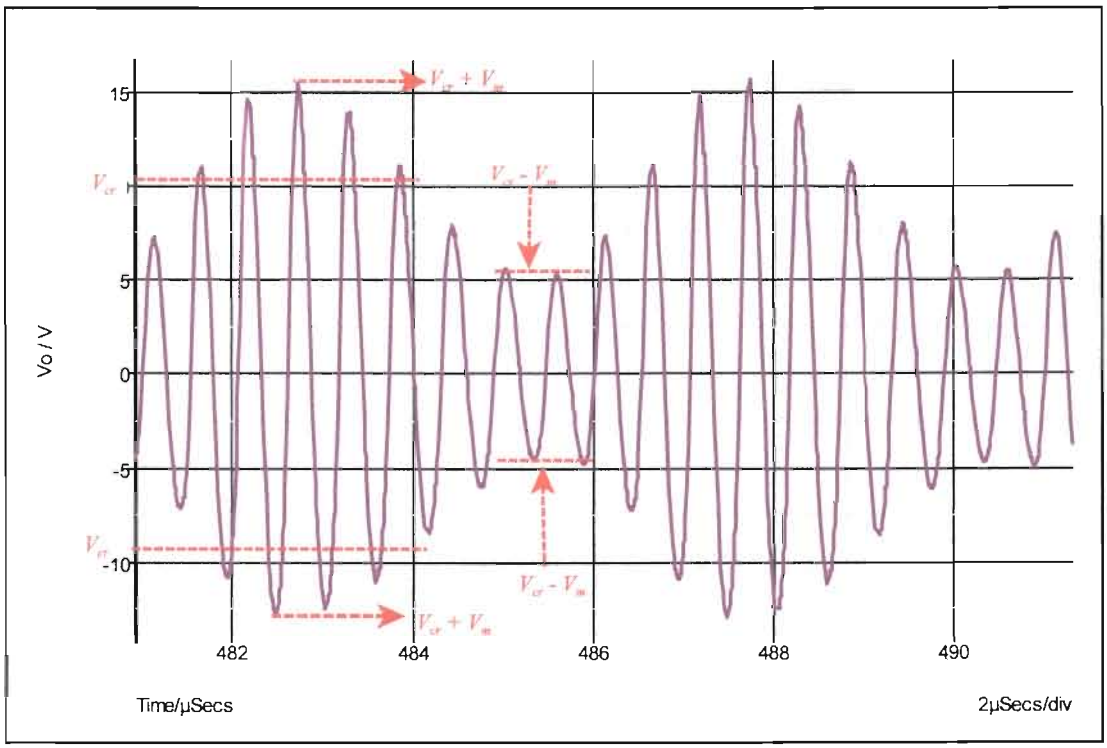

Figure 36 An amplitude modulated wave

First, the best modulation method was chosen. The AM modulated circuit as whole was simulated and compared to the simulations presented in section 3.4.

3.5.1 Modulation method

The majority of double side band (DSB) amplitude modulated radio transmitters use an anode or collector modulated Class C rf tuned power amplifier circuit. Other DSB modulators utilize the nonlinear relationship between applied voltage and resulting current of a transistor or other electronic devices (Green, 1985:35).

These two types were tested with the Class E configuration and the most suitable was chosen.

3.5.1.1 Collector or drain modulation

This form of AM can be generated by placing the modulating voltage in series with the

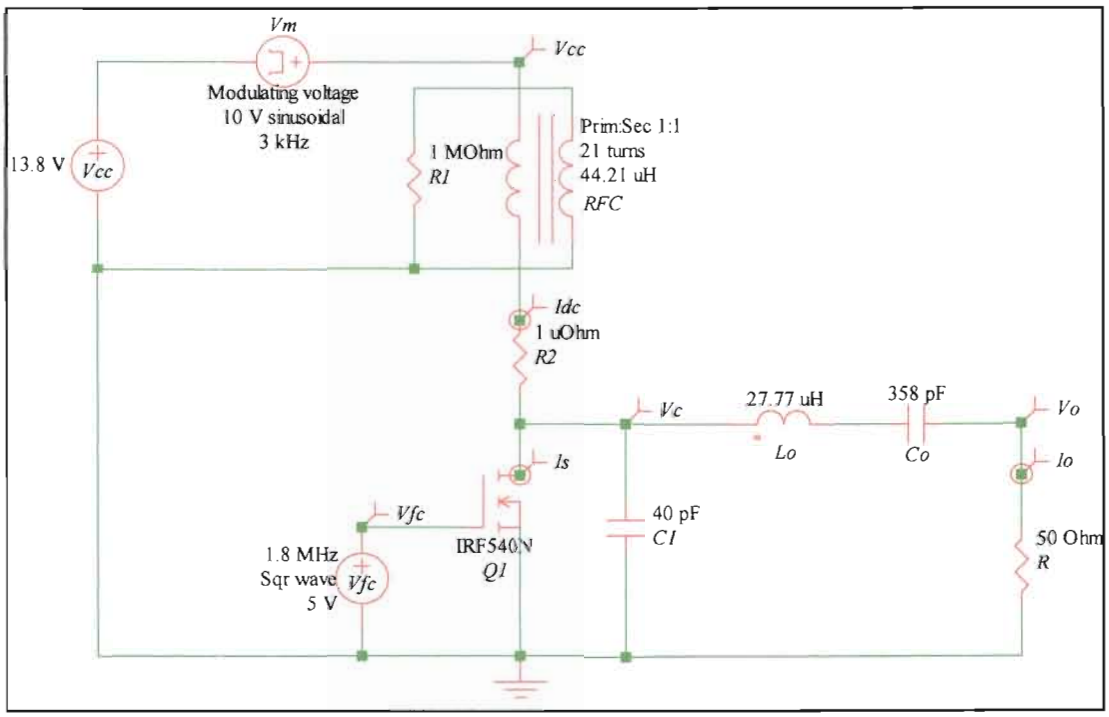

Figure 37 Drain modulation method

drain supply of the Mosfet. When the modulating voltage is positive, the amplifier receives a larger drain voltage and the output signal is increased. When the modulating voltage is negative, the drain voltage and the output are smaller than without modulation. Figure 37 shows the Class E amplifier with the modulation in series with the drain supply.

This is the circuit shown in Figure 28, with 10 V sinusoidal 3 kHz modulation added. This circuit's simulation is shown in Figure 38. If the results of the output voltage shown in Figure 38 are compared to those in Figure 31, it is clear that the peak and minimum values have the modulation added. The 3 kHz envelope is clearly visible in Figure 38, although the 1,8 MHz frequency is too high for the wave lines to be seen.

The spectrum analysis depicted in Figure 39 indicates that the generated modulation is DSBFC. The two side bands are on each side of the carrier wave and are 1,8 MHz ± 3 kHz, since 3 kHz modulation is used. Note that, since the modulation is just less than

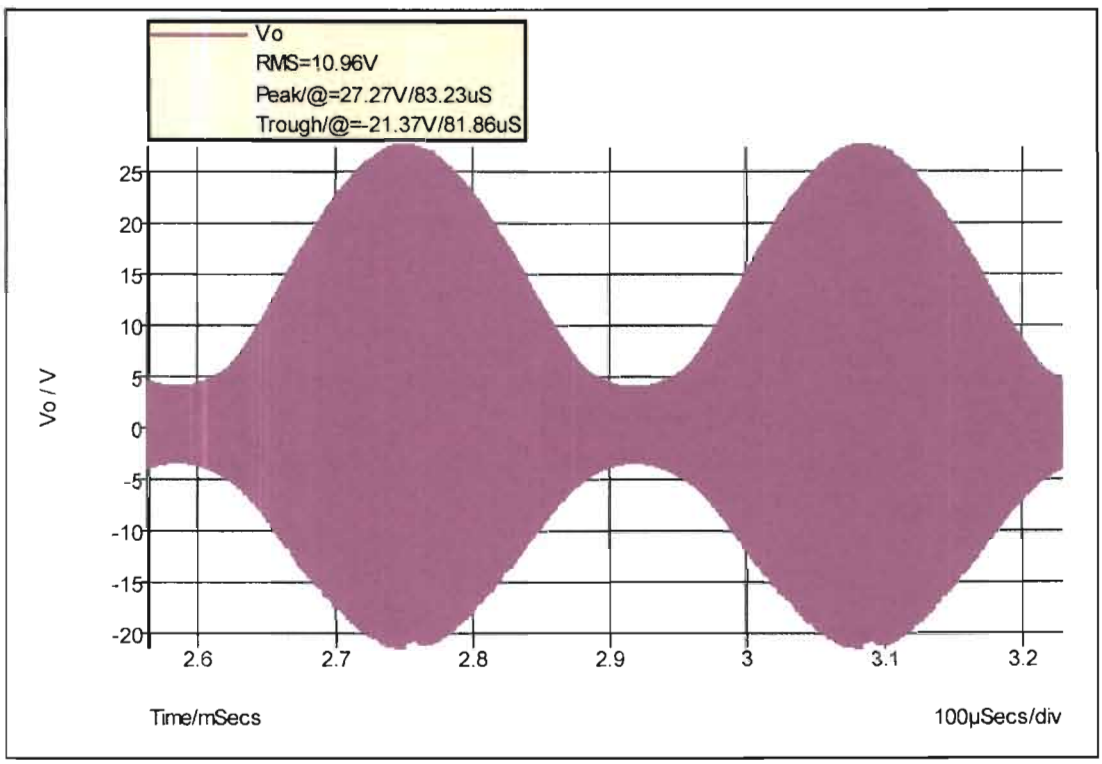

Figure 38 Simulation of circuit in Figure 37

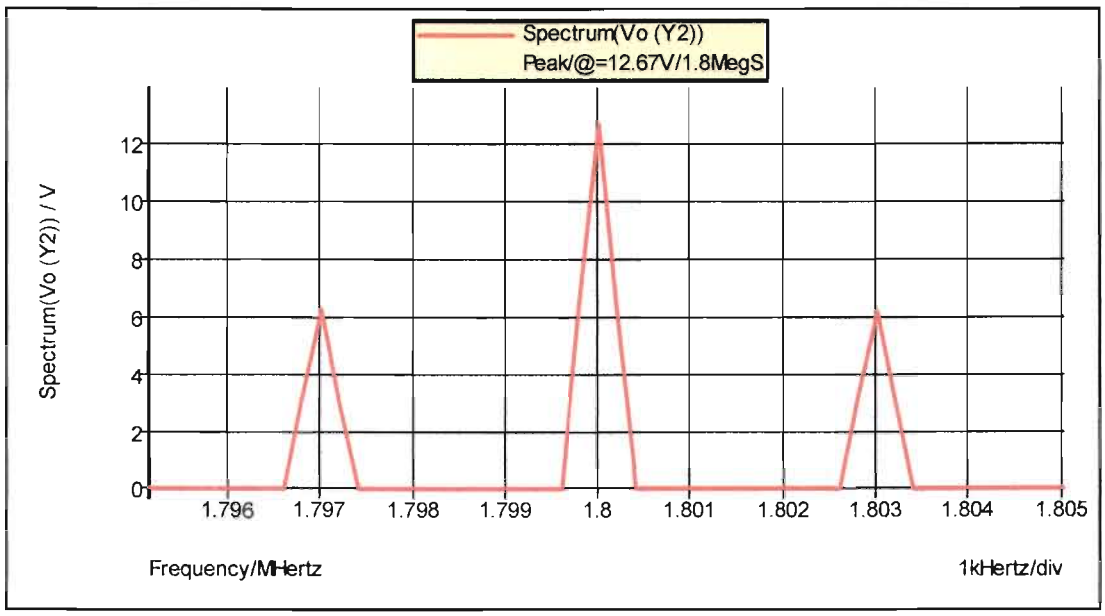

Figure 39 Spectrum analysis of circuit in Figure 37

100 percent, the side band voltages are just below 50 percent of the carrier wave voltage. This method of modulation seems to work very well with Class E modulation.

3.5.1.2 Nonlinear voltage - current method

If a carrier wave at a frequency f_{cr} and a sinusoidal modulating signal at a frequency f_m are applied in series to a transistor, the resultant current will contain components at various frequencies. These will include, f_{cr} and $f_{cr} \pm f_m$. Such a configuration can be seen in Figure 40 where the carrier and modulating signal voltages are introduced into the gate-source circuit of the Mosfet (Green, 1985:36).

The drain current contains the wanted carrier frequency as well as, amongst others, the side band components. According to Green (1985:36) this modulation method is restricted to low power applications because the method has the disadvantages of low efficiency and a high percentage distortion level.

Figure 41 shows the simulation of the circuit depicted in Figure 40. Note the 1,25 V modulating voltage, compared to the 10 V in Figure 37. Any voltage above this causes

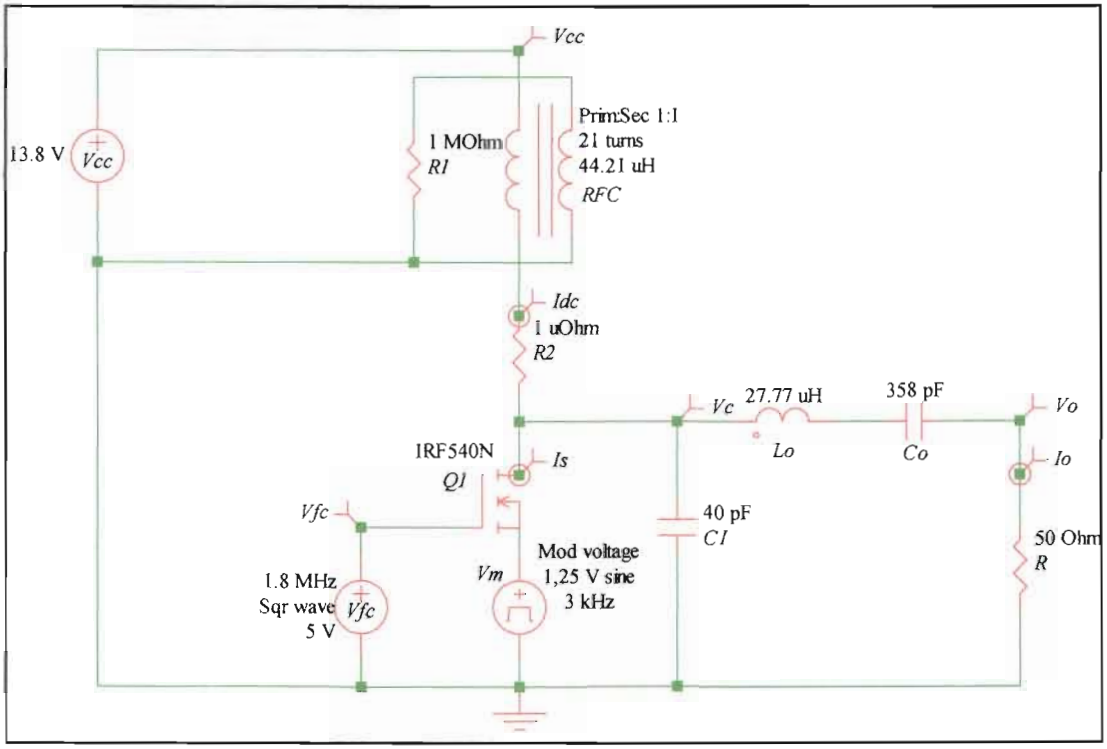

Figure 40 Nonlinear voltage - current method

over modulation. Although the modulation is clearly visible, it is not sinusoidal like the modulation voltage. The spectrum analysis of Figure 40 for the output voltage is given in Figure 42. In Figure 41 the modulation seems to be close to 100 percent, but in Figure 42 the side bands are not even close to 50 percent of the carrier voltage.

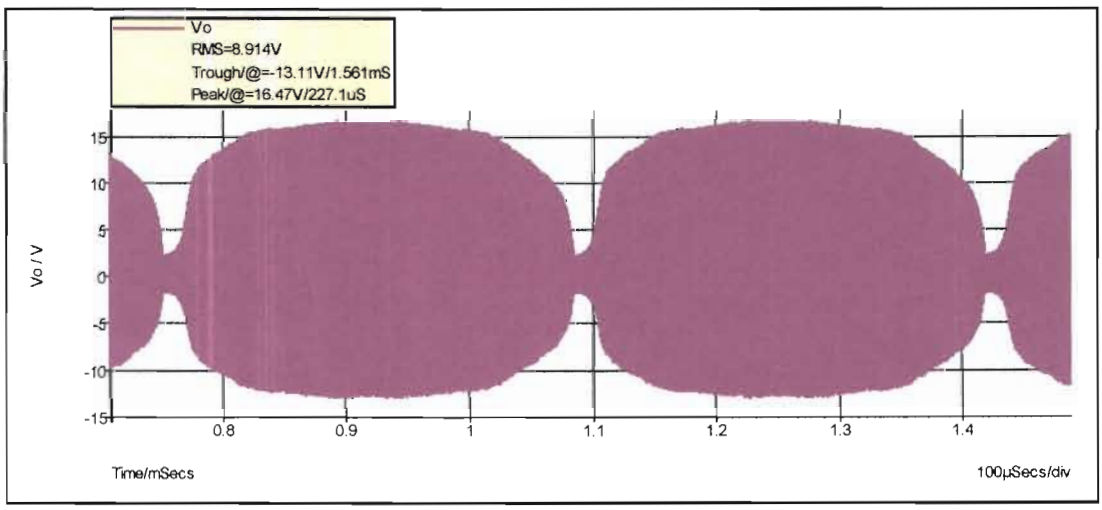

Figure 41 Simulation of circuit in Figure 40

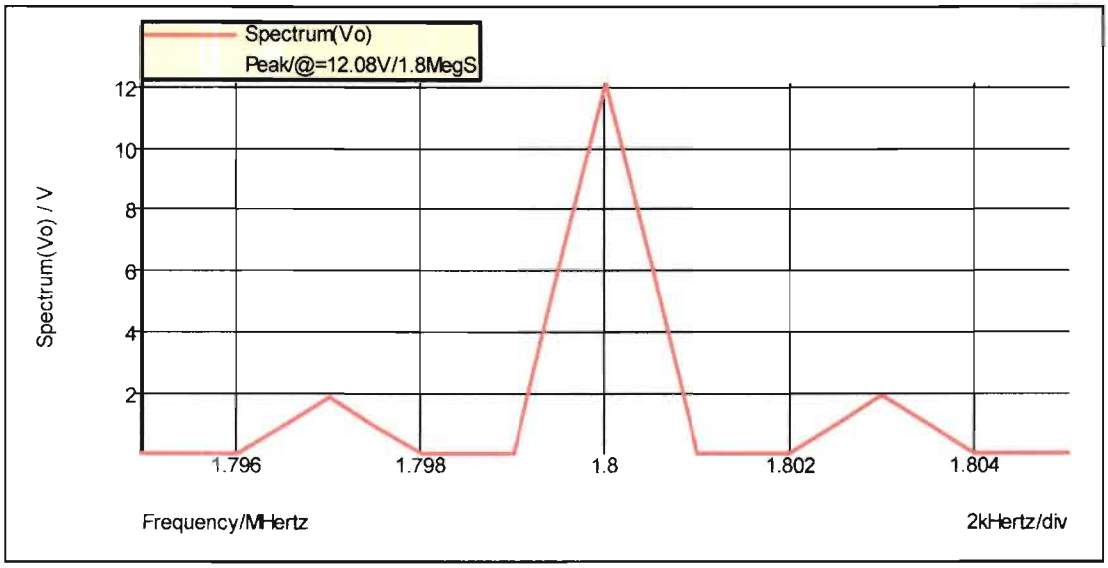

Figure 42 Spectrum analysis of circuit in Figure 40

This modulating technique does not seem to be successful with Class E modulation.

3.5.1.3 Choice of modulation

Of the above two methods of modulation in Class E rf amplifiers, the drain modulation method works successfully. This is the method that was be used further for this project.

3.5.2 Design of modulation implementation

As seen in equation (35) in Annexure H, the modulated signal is the carrier frequency voltage, V_{cr}, with an alternating frequency voltage, the modulation V_m, added to it. This results in a waveform as seen in Figure 36.

A simple way of modulating the generated radio frequency signal is by varying the direct current supply voltage with the modulating signal (Figure 37). In practice this can be done by using a transformer.

A fundamental part of the Class E amplifier is the *RFC* which supplies the constant

current to the circuit. Since the *RFC* coil is already part of the circuit, it is possible to incorporate the *RFC* as part of the transformer to be used for the modulation. This circuit configuration is shown in Figure 43.

Choosing a transformer which will successfully operate as a modulator and a *RFC* is important. With this in mind, the possible values for the transformer's characteristics for both applications need to be looked at.

The following characteristics were considered:

- Rf feedback from the IRF540N affecting the audio generator
- DC resistance of the *RFC* winding affecting *Idc*
- Audio frequency transferring characteristics of the transformer
- Audio power transferred

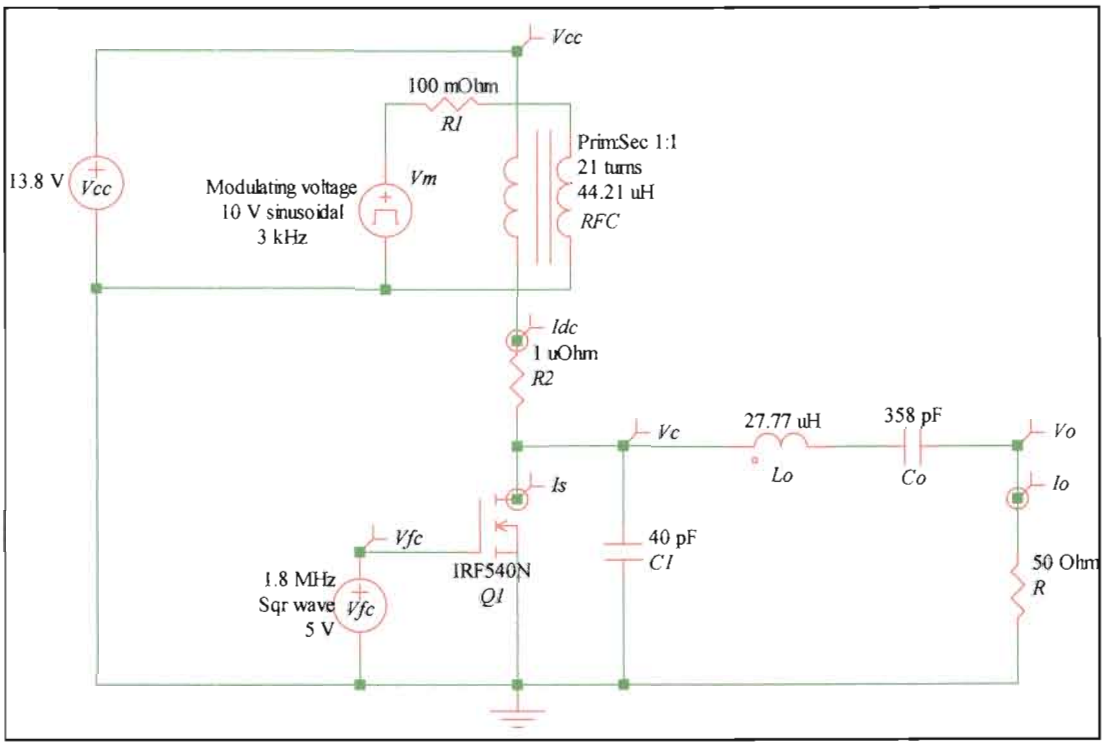

Figure 43 Modulation by using a transformer

3.5.2.1 Rf feedback

The purpose of the transformer is to transfer the audio voltage to the *RFC* side of the transformer in order to vary the supply voltage. This will cause a variation of *Vc* in Figure 43 which will impose the varying voltage on the carrier voltage. Unfortunately the transformer will also transfer a part of the rf frequency generated in IRF540N to the side of the audio supply. This problem could be solved by two methods. It is possible to place a low pass filter (LPF) on the output of the audio supply, which will pass the audio but filter the rf. Such a circuit can be seen in Figure 44, using a second order Butterworth filter.

The other option is to increase the inductance of the transformer's coils so that it will have a high impedance for the rf frequency of 1,8 MHz, but low enough for the audio frequency to operate satisfactorily. Table 17 gives a few inductance values with the corresponding impedances.

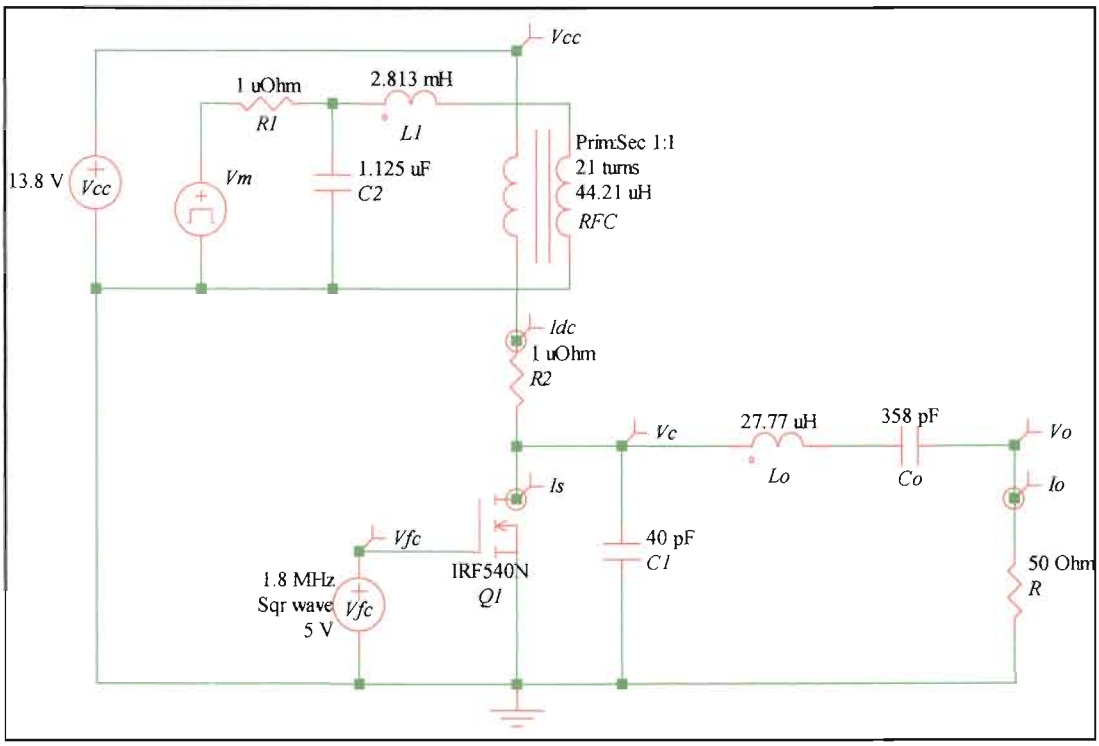

Figure 44 Modulated circuit with audio low pass filter

Table 17 Impedance for two operating frequencies

	Impedance per frequency under test	
Inductance	**4 kHz**	**1,8 MHz**
44,2 uH	1 Ohm	500 Ohm
600 uH	15 Ohm	6,8 kOhm
3 mH	75 Ohm	33,9 kOhm
18 mH	452 Ohm	203 kOhm
70 mH	1,8 kOhm	792 kOhm

From the Table 17 it can be seen that even for 18 mH inductance the audio impedance is only 452 Ohm, which is acceptable. With the same configuration the rf will reach an impedance of 203 kOhm, which will prevent a significant quantity of rf from passing through to the audio supply.

3.5.2.2 DC resistance of the radio frequency choke

According to equation (9) the output power is directly proportional to the supply voltage. With an extra resistance directly in line with the supply voltage the output power will be reduced.

Table 18 gives the typical series resistance for the inductances mentioned in Table 17 as measured with a Philips PM 6303 RCL meter. It also states the voltage over the 50 Ohm load using a simple voltage dividing rule. These are only typical values, since the thickness of the wire also has an effect. The measurements are taken from transformers suitable for audio.

The 62,3 Ohm (Table 18) is totally unacceptable due to the power loss it will cause. The 3 mH's 6,4 Ohm has only an 11 percent reduction in output power, but will lack in rf feedback resistance. The 18,4 Ohm will pass 73 percent of the voltage to the load, which

could be acceptable considering the high resistance to rf feedback.

Table 18 Typical DC resistance of transformers

Transformer winding inductance	Series resistance	50 Ohm load voltage
44 uH	1,7 Ohm	13,3 V
600 uH	2,4 Ohm	13,2 V
3 mH	6,4 Ohm	12,2 V
18 mH	18,4 Ohm	10,1 V
70 mH	62,3 Ohm	6,1 V

3.5.2.3 Audio frequency properties

If the number of windings on the transformer are not enough, the modulation voltage will not successfully be carried over to the supply voltage. The output voltage was simulated using the *RFC* transformer with 21 turns to obtain 44 uH (Figure 43). The

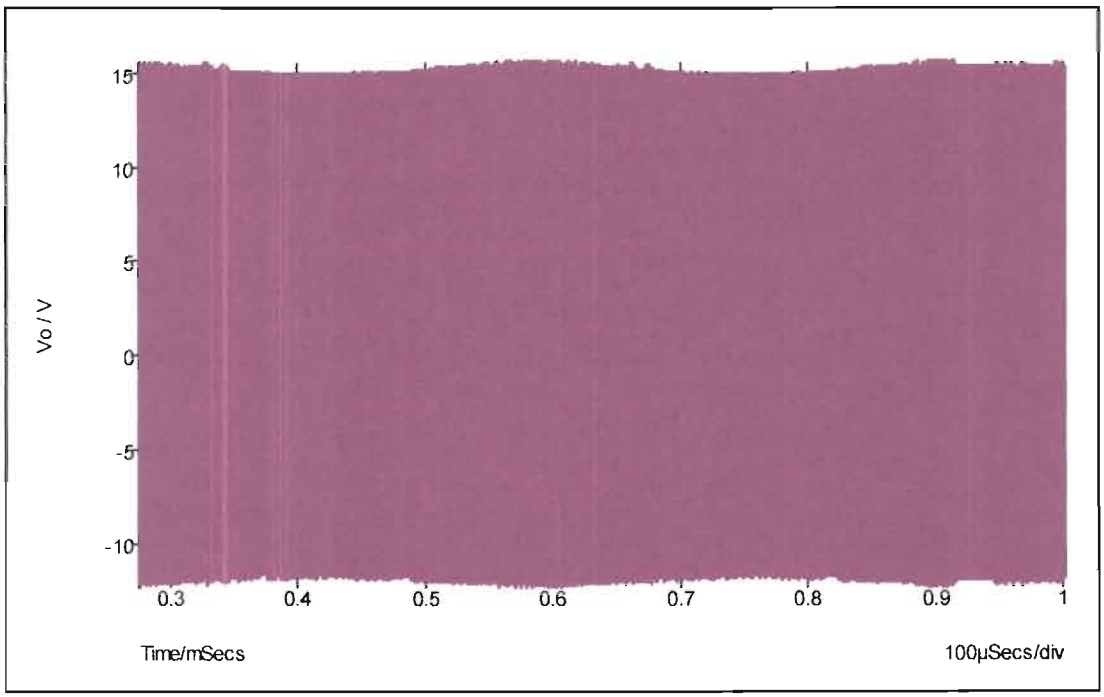

Figure 45 Voltage output simulation for a 21 turn 44 uH winding

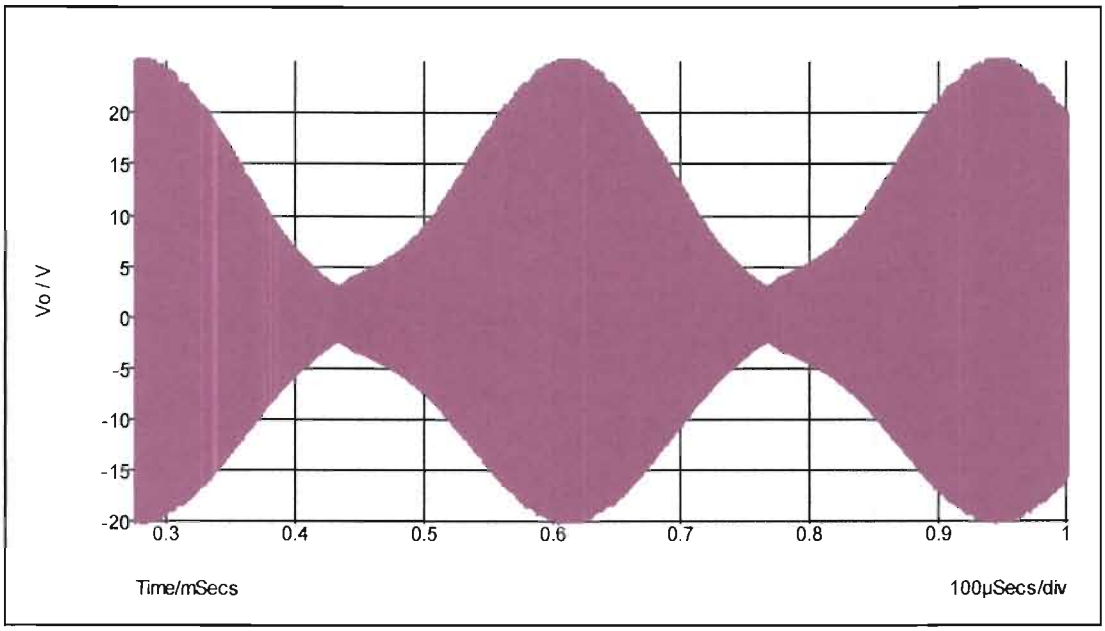

Figure 46 Voltage output simulation for a 425 turn 18 mH winding

results are depicted in Figure 45 and compared to the output voltage simulation results using a transformer with 425 turns to obtain 18 mH as shown in Figure 46. In both cases the supply voltage was 13,8 V with a modulation voltage of 13 V.

As can be seen in the above comparison, there is hardly any modulation shown in Figure 45, while the modulation shown in Figure 46 approaches 100 percent. Although the 44 uH is suitable for the *RFC*, it is not suitable for use with modulation.

3.5.2.4 Audio power transferred

Equation (41) in Annexure H can be used to calculate the quantity of the modulation or audio power (P_m) used in the circuit (for 100 percent modulation m is equal to one):

$$\begin{aligned} P_t &= P_c(1+\tfrac{1}{2}m^2) \\ &= P_c(1+\tfrac{1}{2}1^2) \\ &= \tfrac{3}{2}P_c \text{ W} \end{aligned}$$

To find the modulation power in terms of the carrier power:

$$\begin{aligned} P_t &= P_c + P_m \\ P_m &= P_t - P_c \\ &= \frac{3}{2}P_c - P_c \\ &= \frac{1}{2}P_c \text{ W} \end{aligned}$$

From equation (9) the carrier power can be calculated to determine the modulation power:

$$\begin{aligned} Po &= 0{,}577\frac{V_{cc}^{\,2}}{R} \\ &= 0{,}577\frac{13{,}8^2}{50} \\ &= 2{,}198 \text{ W} \end{aligned}$$

thus the modulation power can be calculated:

$$\begin{aligned} P_m &= \frac{1}{2}P_c \\ &= \frac{1}{2}2{,}198 \\ &= 1{,}099 \text{ W} \end{aligned}$$

This means that the audio supply must be able to generate 1,099 W additional to the specific losses of the transformer used.

3.5.2.5 Choice of a transformer

Taking the above four sections into consideration, a transformer with an inductance of about 18 mH on the *RFC* winding was chosen. The transformer should be able to transfer the 1,099 W to the rf circuit and vary the DC supply voltage with 13,8 V alternating voltage as seen in Figure 36. The chosen transformer was able to:

- Give high resistance to rf feeding back to audio supply, thus eliminating the necessity of using a LPF with the audio supply.
- Provide a reasonably low DC resistance so as not to affect the output power drastically.
- Modulate the DC supply voltage.

3.5.2.6 Final circuit layout

Figure 47 shows the complete solution for the AM modulated Class E amplifier. This is basically simular to that shown in Figure 32 but, with the added transformer specifications as well as the audio generation portion simulated by using *Vm* in Figure 47.

Note that the winding resistance of the transformer is indicated as an external resistance for both the primary and secondary windings.

The frequency for the audio generator could be any frequency between 300 Hz and 3.4 kHz. The voltage indicated in Figure 47 for the audio generator is peak voltage.

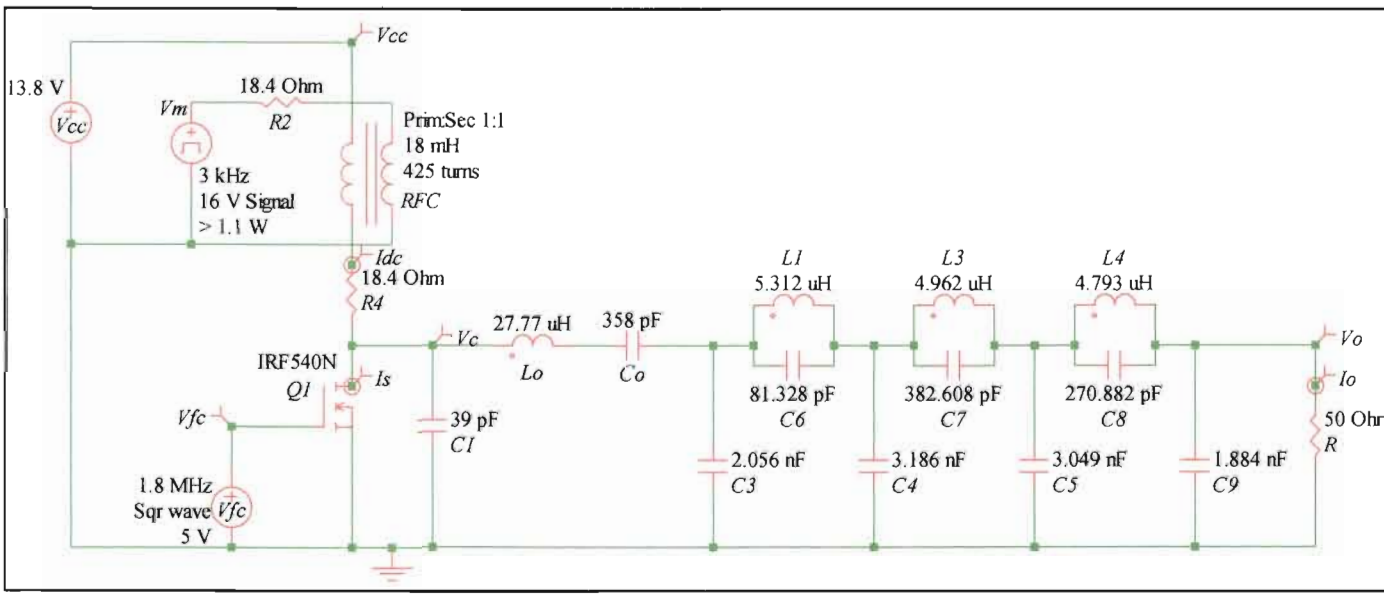

Figure 47 Final circuit layout

3.5.3 Simulation of the final circuit

Once again Simetrix 4.1 was used as a software package for the simulations. For the simulation process, an audio frequency of 3 kHz was used, since it makes the modulation more visible for shorter time periods than what lower frequencies would.

The following parameters were simulated:

- new values of *Vc*, *Is* and *Idc* with the modified *RFC* value
- Class E and audio input power
- output power
- efficiency of the circuit.

3.5.3.1 *Idc* simulation

Comparing the results of Figure 48 and that of Figure 29, it is clearly visible that the AC component of *Idc* is much lower in Figure 48. This is the result of the prominently larger *RFC* value in Figure 47. As stated in section 2.3.1, the *RFC* is used to keep the current-flow constant. Thus, with the larger *RFC* value the AC component is smaller.

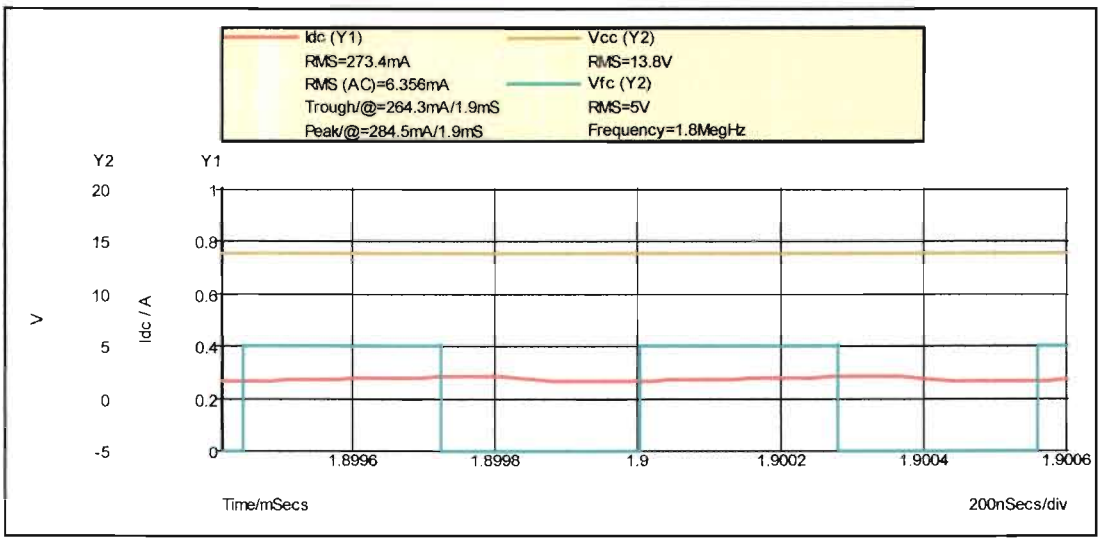

Figure 48 Simulation of *Idc*

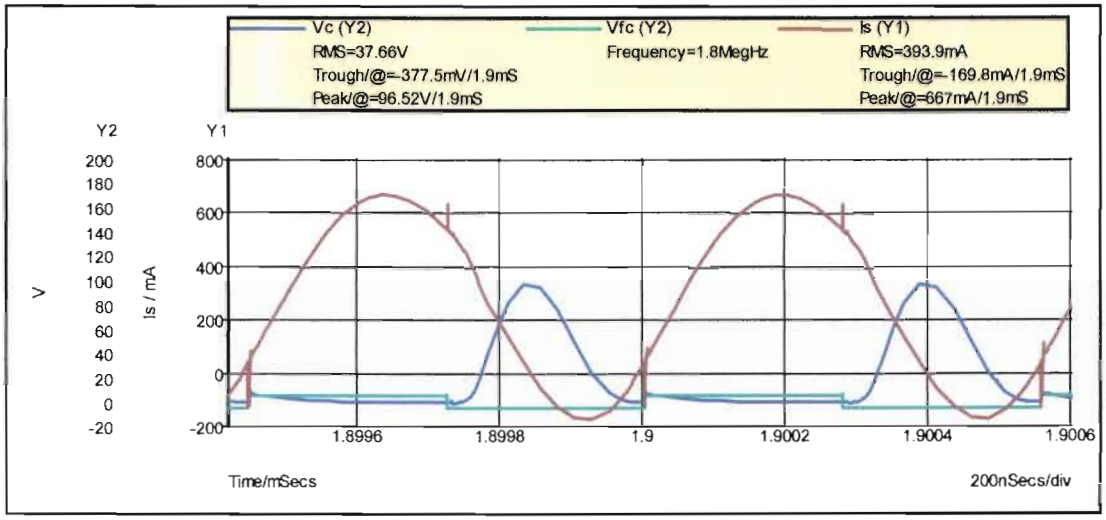

Figure 49 Simulaton of *Vc* and *Is*

The higher RMS value is due to the modulation which is added on top of the normal *Vcc* power supply (Figure 48). This value varies according to the position in the modulation time cycle the snapshot is taken.

3.5.3.2 *Vc* and *Is* simulation

The result of the simulation for *Vc* and *Is* is shown in Figure 49. If this is compared to the results shown in Figure 30, it can be seen that the waves are smoother. This is also

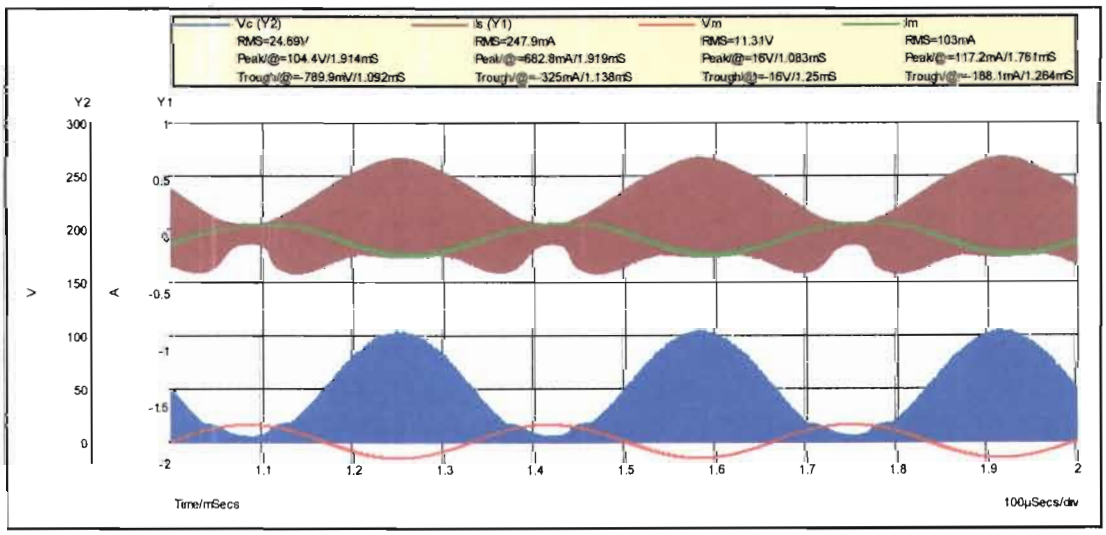

Figure 50 Modulation effect on *Vc* and *Is*

the influence of the larger *RFC* value, suppling a more constant current.

The values for both *Is* and *Vc* are higher. This is due to the modulation process which varies the voltage *Vc* as well as the supply current *Idc* (Figure 47). In Figure 50, *Im* represents the current supply from the modulation generator and *Vm* represents the voltage supply of the modulation generator, *Vm*. The waves are 180° out of phase due to the transformer, but the graph shows very clearly how the amplitudes of both *Vc* and *Is* vary as the modulation waves vary.

3.5.3.3 Input power simulation

Figure 51 show two power plots. These are for *Vcc*, the DC source, and *Vm*, the modulation source, as indicated in Figure 47. It is clearly visible how the modulation influences the power sources. If these two powers are summed together, they result in a total input power of 2,890 W.

3.5.3.4 Output power simulation

The output power plot, including the output voltage and current plots, for Figure 47 are

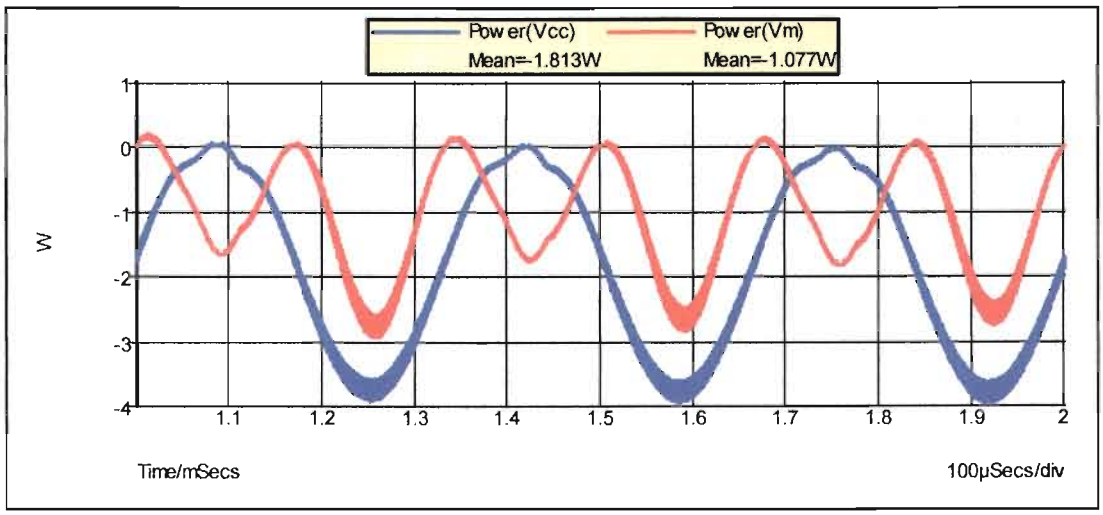

Figure 51 Input power simulations

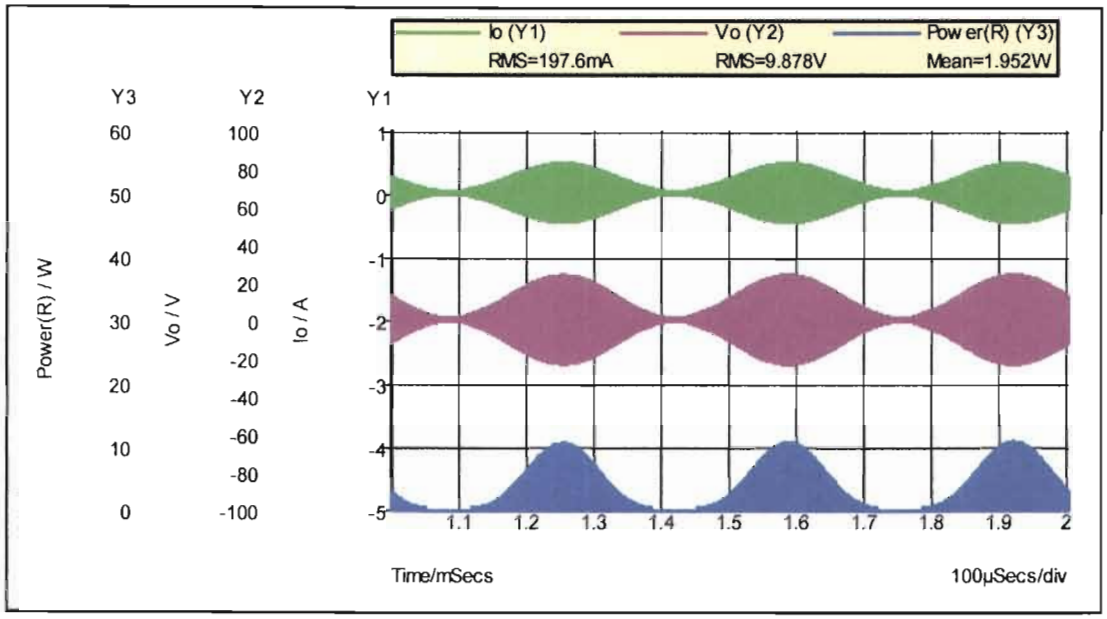

Figure 52 Output power simulation

shown in Figure 52, which shows that the modulation on output current *Io* and the output voltage *Vo* are in phase, thus resulting in an output power wave, *Po*, in load *R* in which the modulation wave can be seen.

3.5.3.5 Efficiency of the circuit

In order to obtain the modulation efficiency, equation (43) is manipulated so that the modulation power is defined by:

$$\begin{aligned} P_t &= P_{cr} + P_m \\ P_m &= P_t - P_{cr} \\ &= P_t - \frac{2}{3}P_t \\ &= \frac{1}{3}P_t \ \text{W} \end{aligned}$$

The average power of 1,952 W (Figure 52) should be the result of 0,651 W modulation power when the modulation is 100 percent. Figure 51 indicates a modulation power of 1,077 W which allows for some losses in the transformer coupling and series resistance

losses in the windings of 0,426 W.

The overall efficiency of the circuit can be calculated as the ratio of the output power to the input power. The total input power is the sum the power supplied by the direct current voltage source, *Vcc*, and the power supplied by the modulation source, *Vm*. The output power is the power at load *R*.

The overall efficiency can be calculated as:

$$\eta = \frac{P_o}{P_i}$$
$$= \frac{1{,}952}{1{,}813 + 1{,}077}$$
$$= 0{,}6754$$
$$= 67{,}5\ \%$$

Figure 32 depicts the circuit with the modulation process taken out of the equation. Without modulation, the winding resistance, *RFC* series resistance and the transformer losses can be ignored. Then total input power is the *Vcc* input power of 2,209 W, as seen

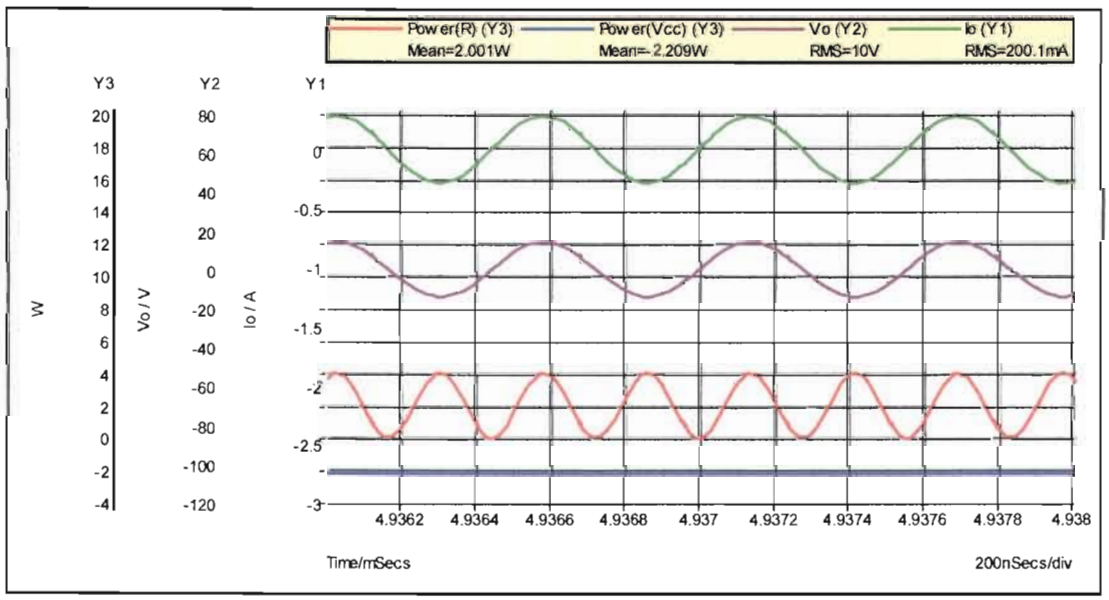

Figure 53 Simulation without modulation

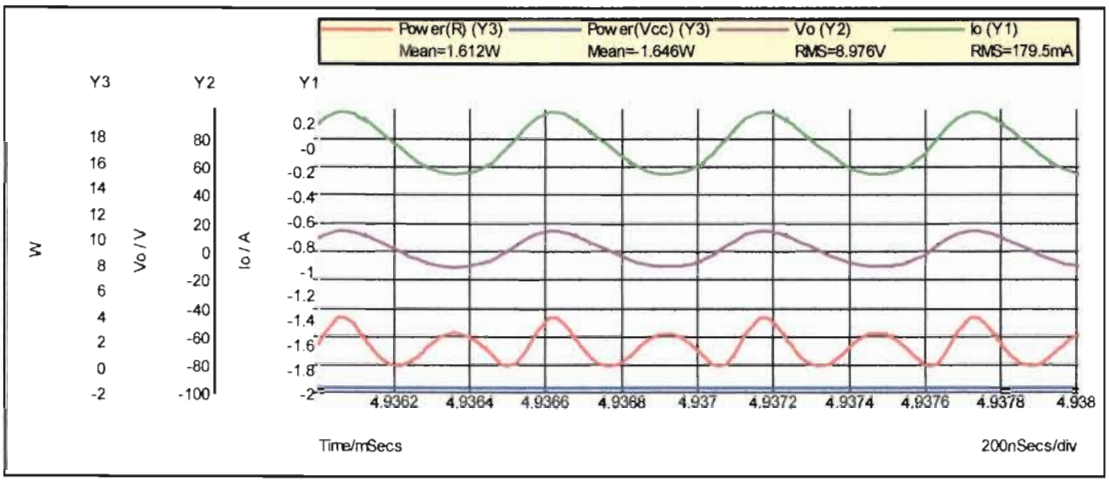

Figure 54 Simulation without modulation and harmonic filter

in Figure 53. The output power through load *R* is 2,001 W. The resulting efficiency is 90,6 percent, which represents the Class E efficiency including the harmonic filter. This means that 23,1 percent efficiency is lost due to the modulation process.

With these results it is possible to calculate the modulation efficiency, since the overall efficiency is a product of the modulation and DC source efficiencies:

$$\begin{aligned} \eta &= \eta_{fig32} \times \eta_m \\ 0{,}675 &= 0{,}906 \times \eta_m \\ \eta_m &= 0{,}7450 \\ &= 74{,}5\ \% \end{aligned}$$

The circuit in Figure 28 was used to simulate the Class E amplifier on its own. This circuit excludes the modulation process as well as the harmonic filter. The simulation is shown in Figure 54 with an output power through load *R* of 1,612 W and an input power from source *Vcc* of 1,646 W.

The Class E efficiency (circuit without modulation and harmonic filter) can be calculated as:

$$\eta = \frac{P_o}{P_i}$$
$$= \frac{1{,}612}{1{,}646}$$
$$= 0{,}9793$$
$$= 97{,}9\ \%$$

This simulated efficiency of 97,9 percent for the Class E amplifier indicates a very satisfactory value for a high efficiency amplifier.

3.6 Summary

A suitable switch, the IRF540N Mosfet, was chosen together with the TC4421 Mosfet driver as the carrier generator. The characteristics of these components were used as part of the Class E rf power amplifier design.

The simulations done in this chapter confirm that a successful Class E rf power amplifier was designed. These data will be compared with the practical test results in chapter four.

The design of the filter fell short according to the simulation, but since the design was done according to very high standards, the result is satisfactory for the Class E rf amplifier.

AM was implemented into the Class E amplifier by means of the drain modulation method with a suitable transformer. Various elements of the final solution to the high efficiency modulated Class E amplifier were simulated. The efficiencies were calculated from the simulations as:

- 97,9 percent for the Class E circuit

- 74,5 for the modulation process
- 67,5 for the overall circuit

Chapter four will reflect the results of the built circuit. Physical measurements will be compared to the theory and simulations done.

Chapter 4 Measured results

The complete solution to the high efficiency modulated Class E amplifier is shown as a block diagram in Figure 55. The audio amplifier is additional to the circuit shown in Figure 47. This makes it possible to use the amplifier with a low-level audio source, as for instance a compact disc player.

Another addition is the step up transformer which is used to effectively modulate the *RFC* and modulation transformer, since the audio amplifier's output voltage is not high enough.

An eight volt regulator is shown which supplies the carrier generator. This regulator keeps the current drawn by TC4421, as discussed in section 3.1.1.2, under control. It also assists with keeping the input to the carrier generator stable for a better quality

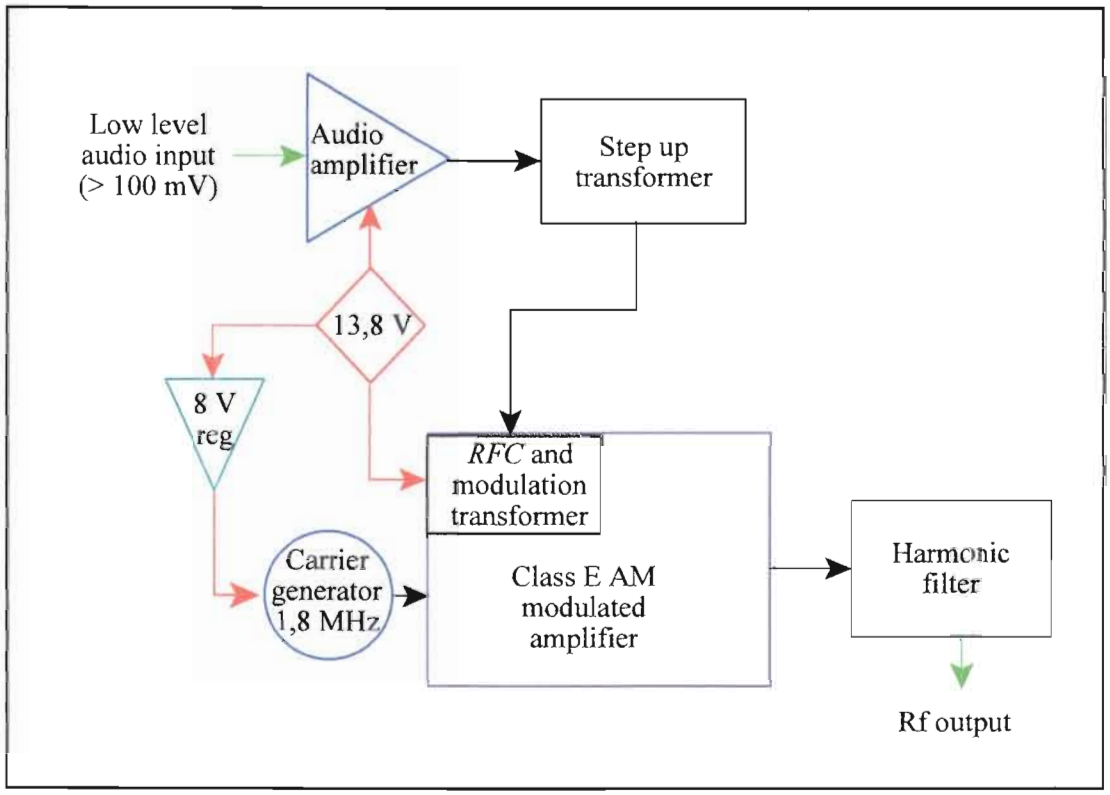

Figure 55 Block diagram of the complete circuit

carrier input to the Class E amplifier.

Annexure A provides a schematic diagram, printed circuit board layout and a photograph of the built PCB of the block diagram shown in Figure 55. The power supply, audio amplifier and step-up transformer are not included.

In chapter three various Class E parameters and other parameters were simulated. These simulations were tested with realtime measurements. The following measurements were done:

- Supply current *Idc*
- Capacitor voltage *Vc* and switching current *Is*
- Output parameters: *Vo*, *Io* and *Po*
- DC input power *Pidc*, modulation input power *Pim*, efficiency
- Filter characteristics: attenuation and harmonic analysis
- Modulation distortion and AM envelope

The abovementioned measurements were done with the aid of the following instruments and accessories:

- Tektronix TDS520A digitizing oscilloscope
- IFR 2945A communications service monitor
- Tektronix TX3 true RMS multimeter
- In line 1:5 current probe (see Annexure G)
- Fluke VP200 10:1 voltage probe

4.1 Supply current *Idc*

The simulation done in Figure 48 is a snapshot of the modulation period. Figure 56 depicts a simulation of *Idc* over a time period of three modulation cycles, so that the

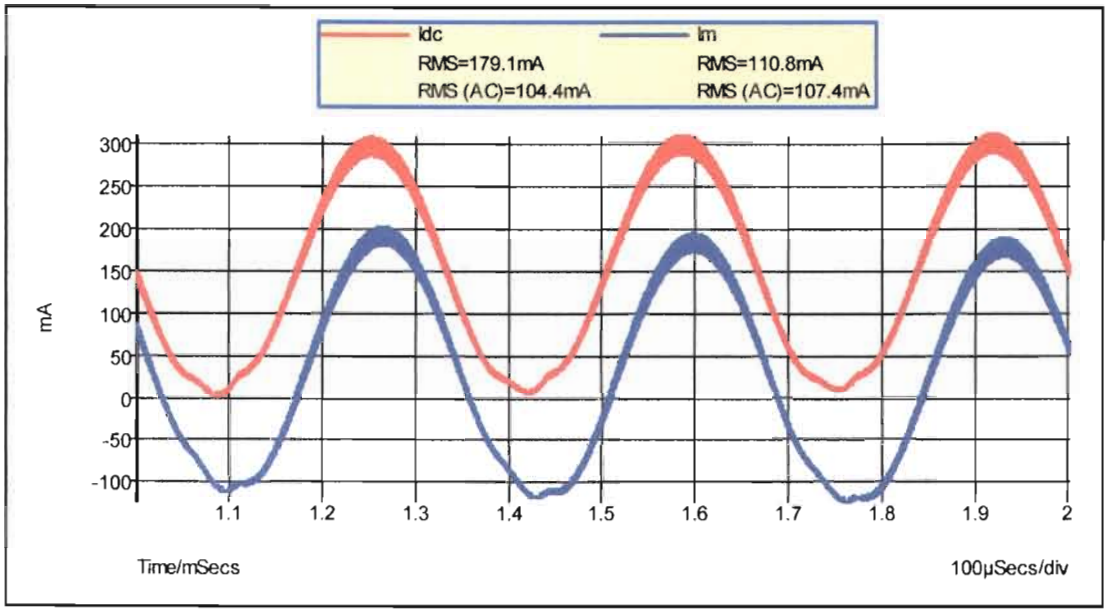

Figure 56 Simulation of *Idc* over three modulation cycles

variation of *Idc* due to modulation is accounted for. The measurements were done with the Tektronix TX3 multimeter. See the results in Table 19. It shows that the DC value (171,8 mA) is 95,9 percent of the simulated value (179,1 mA), which compares very well.

Table 19 Measured values for *Idc*

Instrument	Measurement	Measured value	Simulation
multimeter	RMS DC current	171,8 mA	179,1 mA
multimeter	RMS AC current	121 mA	104,4 mA

The AC component, which is due to modulation current *Im*, has a 16,6 mA difference. This also compares satisfactorily. A reason for the difference could be the percentage modulation difference between the simulation and the real measurements.

4.2 Capacitor voltage *Vc* and switching current *Is*

Vc and *Is* were measured with the oscilloscope and reported in Figure 57, where Ch1

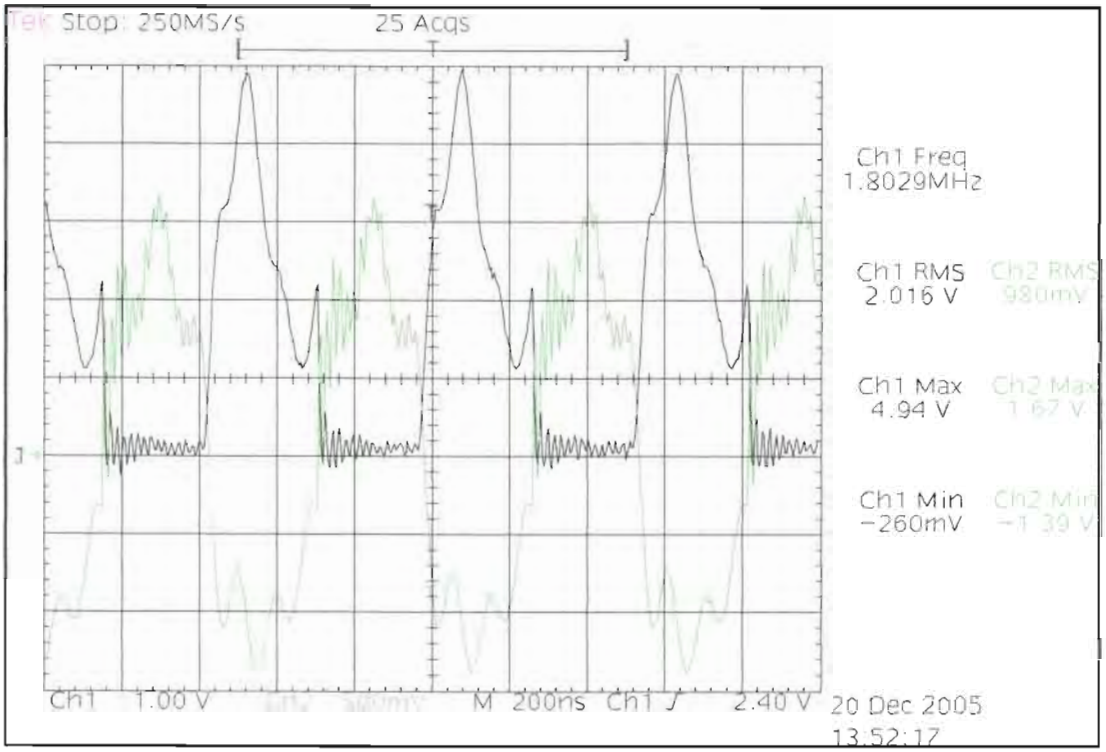

Figure 57 Measured oscilloscope results of *Vc* and *Is*

represents *Vc*, while Ch2 represents *Is*. As previously stated the measurements on the oscilloscope are done with the aid of a 10:1 ratio voltage probe and a 1:5 ratio current probe. Thus, the actual measured values of the measured results in Figure 57 are given in Table 20. The simulated values from Figure 58 are also given in Table 20.

Table 20 Measured values for *Vc* and *Is*

	Measured results		**Simulation**	
Measurement	***Vc***	***Is***	***Vc***	***Is***
RMS	20,16 V	196 mA	18,91 V	212 mA
Max	49,40 V	334 mA	46,38 V	401,1 mA
Min	-2,60 V	-278 mA	-750,8 mV	-233,8 mA

Comparing the measured results in Table 20 with the simulated values obtained in Figure 58, it is seen that the RMS value of the measured voltage is 1,25 V higher while

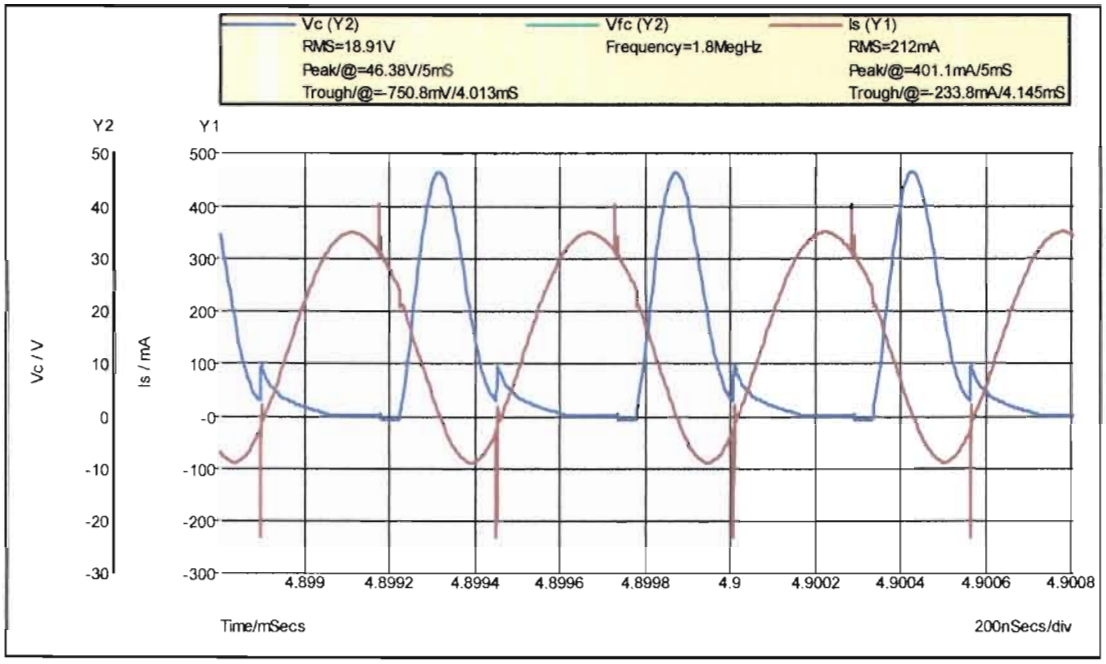

Figure 58 Simulation of *Vc* and *Is*

the measured current is 16 mA lower. Respective percentage differences of six and eight percent. Although the measured current waves are more noisy than the simulated waves, the measured results are a sound comparison.

Since modulation has a phenomenal effect on both *Vc* and *Is*, the simulation and measurement were done without modulation.

4.3 Output parameters: *Vo*, *Io* and *Po*

The simulated efficiency was tested for:

- The complete circuit (Figure 47)
- The circuit without modulation (Figure 32)
- The circuit without both modulation and harmonic filter (Figure 28)

Thus, the output parameters were measured accordingly. The output parameters were measured with an oscilloscope over three modulation cycles. A 3 kHz modulation tone

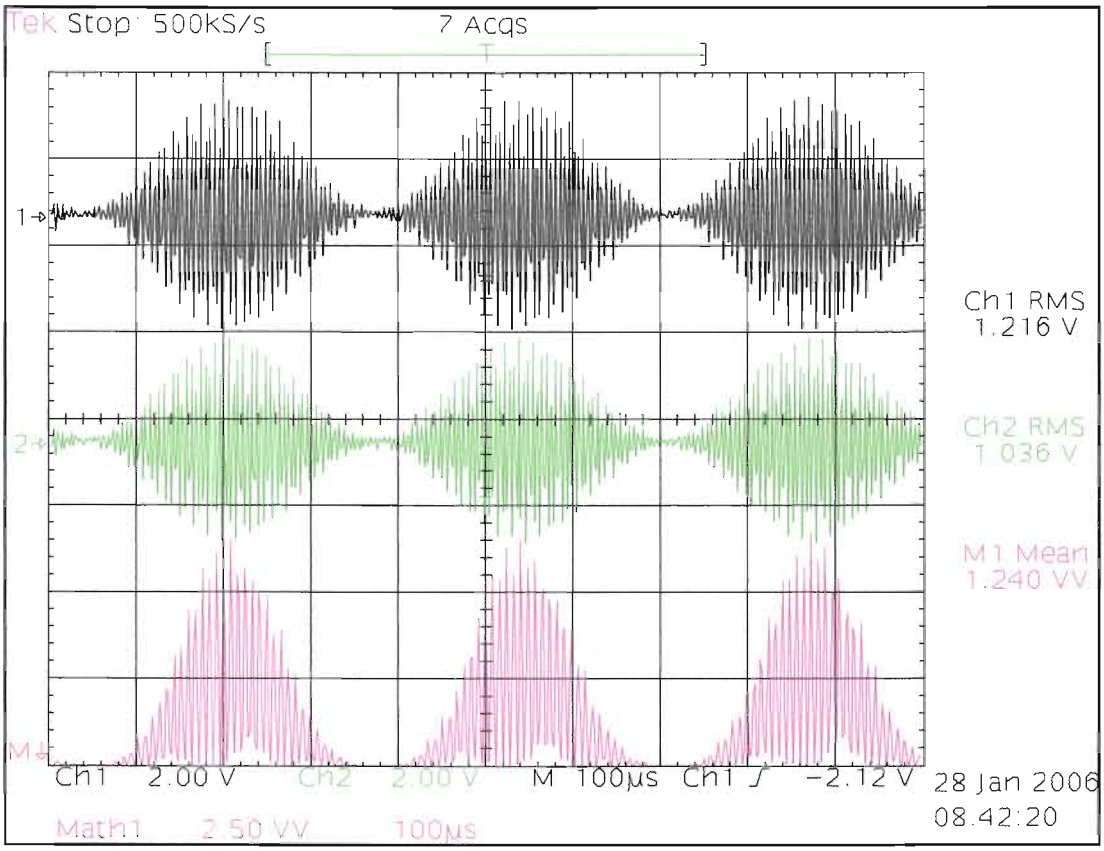

Figure 59 Measured oscilloscope results for *Vo*, *Io* and *Po*

(1 ms span) was used at 100 percent modulation. The results are given in Figure 59. In Figure 59 Ch1 represents the output voltage *Vo*, Ch2 represents the output current *Io* and M1 represents the output power *Po*. Taking the respective ratios into consideration, the actual measured values are given in Table 21 together with the simulated values which are depicted in Figure 52.

Table 21 Measured values for Figure 59

Parameter	Measured value	Simulation	Measurement
Vo	12,16 V	9,878 V	RMS
Io	207.2 mA	197,6 mA	RMS
Po	2,480 W	1,952 W	average

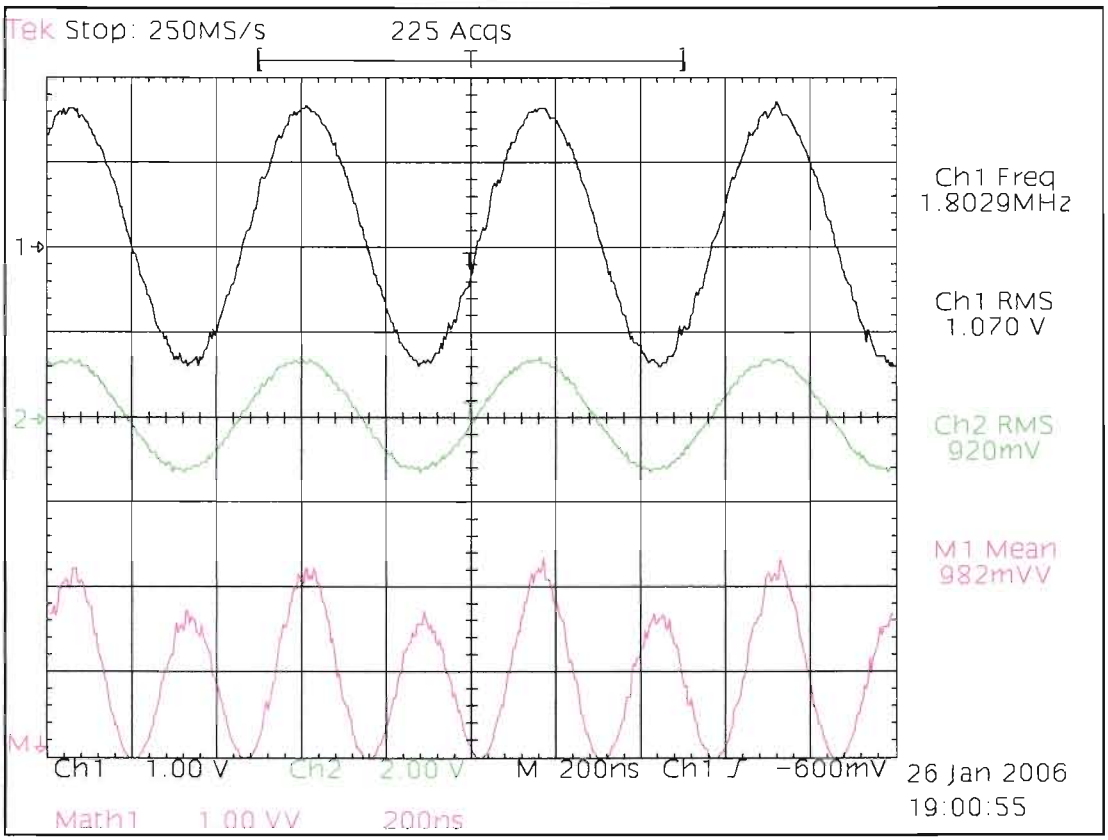

Figure 60 Measured oscilloscope results without modulation

When the comparison is made between the simulated and actual measured parameters, it can be seen that all the values are similar, although the obtained measured results are better than expected by a small margin.

Figure 60 gives the oscilloscope results without modulation. The resultant measured values for Figure 60 are given in Table 22, together with the simulations in Figure 53. Ch1, Ch2 and M1 represent *Vo*, *Io* and *Po* respectively.

Table 22 Actual values for Figure 60

Parameter	Measured value	Simulation	Measurement
Vo	10,70 V	10,0 V	RMS
Io	184 mA	200,1mA	RMS
Po	1,969 W	2,401 W	average

Figure 60 shows that for the negative cycle of *Vo* and *Io,* the *Po* value is lower than that for the positive cycle. This is due to the *Vo* wave which is not completely symmetrical. It tends to have small positive offset.

Figure 61 shows the output parameters without modulation and without the low pass or harmonic filter. This circuit is basically the Class E amplifier on its own. The resultant measured values for Figure 61 are given in Table 23 together with the corresponding simulated values from Figure 54. Ch1, Ch2 and M1 represent *Vo*, *Io* and *Po* respectively.

It is apparent from Figure 61, that the power wave is more affected for the positive and negative cycles of the *Vo* and *Io* waves. Thus, the absence of the filter causes additional positive offset.

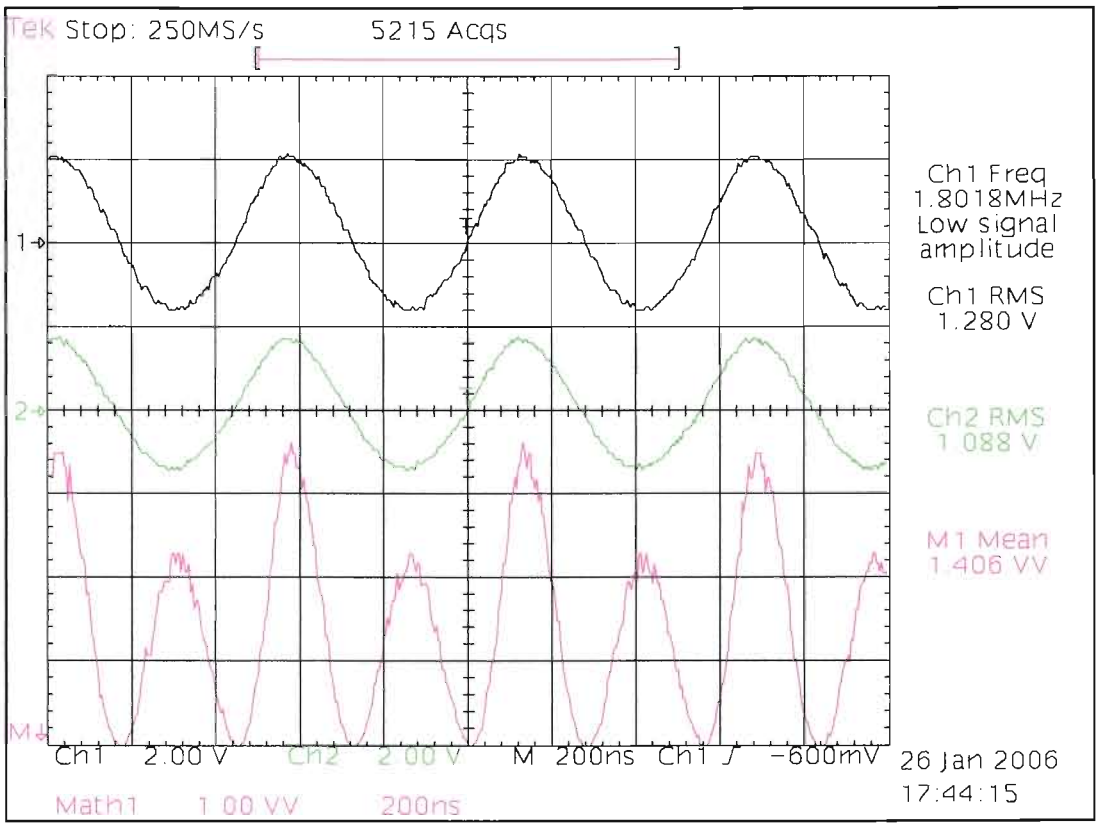

Figure 61 Measured oscilloscope output results without modulation and LPF

Table 23 Actual values for Figure 61

Parameter	Measured value	Simulation	Measurement
Vo	12,80 V	8,976 V	RMS
Io	217,6 mA	179,5 mA	RMS
Po	2,812 W	1,612 W	average

4.4 DC Input power *Pidc*, modulation input power *Pim*, efficiency

For this setup the audio source is taken as the input supplied to the *RFC*. Thus, the audio amplifier and the step up transformer are not considered for the efficiency measurements.

The 8 V regulated part of the circuit was not part of the input power simulations reported in section 3.5.3.3. The carrier generator has a separate supply as indicated in Figure 47. The measured DC current supply is the current through the *RFC*. As for the output measurements, the input measurements will also be done for the complete circuit, the circuit without modulation, and the circuit without modulation and *LPF*.

The modulation input voltage and current, *Vm* and *Im,* as well as the DC input voltage and current, *Vdc* and *Idc*, were measured with the Tektronix TX3 true RMS multimeter. The calculated power results are the input modulation power (*Pim*) and the DC input power from *Vcc (Pidc)*. The results are given in Table 24 and Table 25.

Table 24 Modulation input measurements

Parameter	Measurement
Vm	77,1 V
Im	20,71 mA
Pim	1,597 W

Table 25 DC input measurements

Parameter	Measurement		
	Complete circuit	**Without modulation**	**Without modulation and LPF**
Vdc	13,8 V	13,8 V	13,8 V
Idc	181,6 mA	187,1 mA	205,6 mA
Pidc	2,506 W	2,582 W	2,837 W

The efficiency of the circuit can now be calculated. This will be done by using the oscilloscope-measured power outputs shown if Figure 59, Figure 60 and Figure 61 and the calculated input power given in Table 24 and Table 25.

The efficiency for the complete circuit can be calculated with the output results from Figure 59. *Pi* is the sum of *Pim* and *Pidc*:

$$\eta = \frac{P_o}{P_{im} + P_{idc}}$$
$$= \frac{2{,}480}{1{,}597 + 2{,}506}$$
$$= 0{,}6044$$
$$= 60{,}4\ \%$$

Without modulation, the efficiency can be calculated by using the output oscilloscope results from Figure 60:

$$\eta = \frac{P_o}{P_{idc}}$$
$$= \frac{1{,}969}{2{,}582}$$
$$= 0{,}7626$$
$$= 76{,}3\ \%$$

To calculate the efficiency of the modulation process, the overall efficiency and the efficiency without modulation are used:

$$\begin{aligned} \eta &= \eta_{\text{no mod}} \times \eta_m \\ 0{,}604 &= 0{,}763 \times \eta_m \\ \eta_m &= 0{,}7916 \\ &= 79{,}2\ \% \end{aligned}$$

The efficiency for the circuit in Figure 28 where the modulation process and the low pass filter are excluded, ie the Class E amplifier on its own, can be calculated:

$$\begin{aligned} \eta &= \frac{P_o}{P_{idc}} \\ &= \frac{2{,}812}{2{,}837} \\ &= 0{,}9911 \\ &= 99{,}1\ \% \end{aligned}$$

The simulated and measured efficiencies are compared in Table 26.

Table 26 Efficiency comparison

Setup	Simulation	Actual measurement
Complete circuit	67,5 %	60,4 %
Modulation	74,5 %	79,2 %
Without modulation	90,6 %	76,3 %
Class E	97,9 %	99,1 %

The data in Table 26 show that the measured efficiency for the modulation is more effective than that of the simulation. The Class E circuit (the circuit without modulation and harmonic filter) is very effective, more so than the modulation. The complete circuit and the circuit without modulation are less effective because the harmonic filter has a

bigger measured loss than when simulated. This is illustrated below.

4.5 Filter characteristics: attenuation and harmonic analysis

To determine the attenuation, the measured output power after the harmonic filter will be compared to the measurement just before the harmonic filter. These measurements are given in Figures 60 and 61 with the values presented in Tables 22 and 23.

Using equation (32) the output power of Figures 60 and 61 can be calculated and expressed in decibels.

$$P_{dBm} = 10\log\frac{P_W}{1mW}$$

$$P_{Fig60} = 10\log\frac{1{,}969}{0{,}001}$$

$$= 32{,}942 \text{ dBm}$$

$$P_{Fig61} = 10\log\frac{2{,}812}{0{,}001}$$

$$= 34{,}490 \text{ dBm}$$

Thus, the attenuation is 1,548 dB. This a reasonable acceptable attenuation value for a filter, although the simulated value according to Table 15 shows a gain of 0,7 dB, which is not practical. According to the measurements made with the setup in Figure 62, as presented in Table 27, the attenuation is 1,1 dB, which is quite satisfactory.

To determine the harmonic analysis, the IFR communications service monitor will be used together with the oscilloscope. Readings will be taken before and after the harmonic filter. Figure 62 gives the test setup. The Math function is used on the oscilloscope to calculate the power measurement from the voltage and current measurements in Figure 62. The measured values and the calculated attenuation at the various frequencies are given in Table 27.

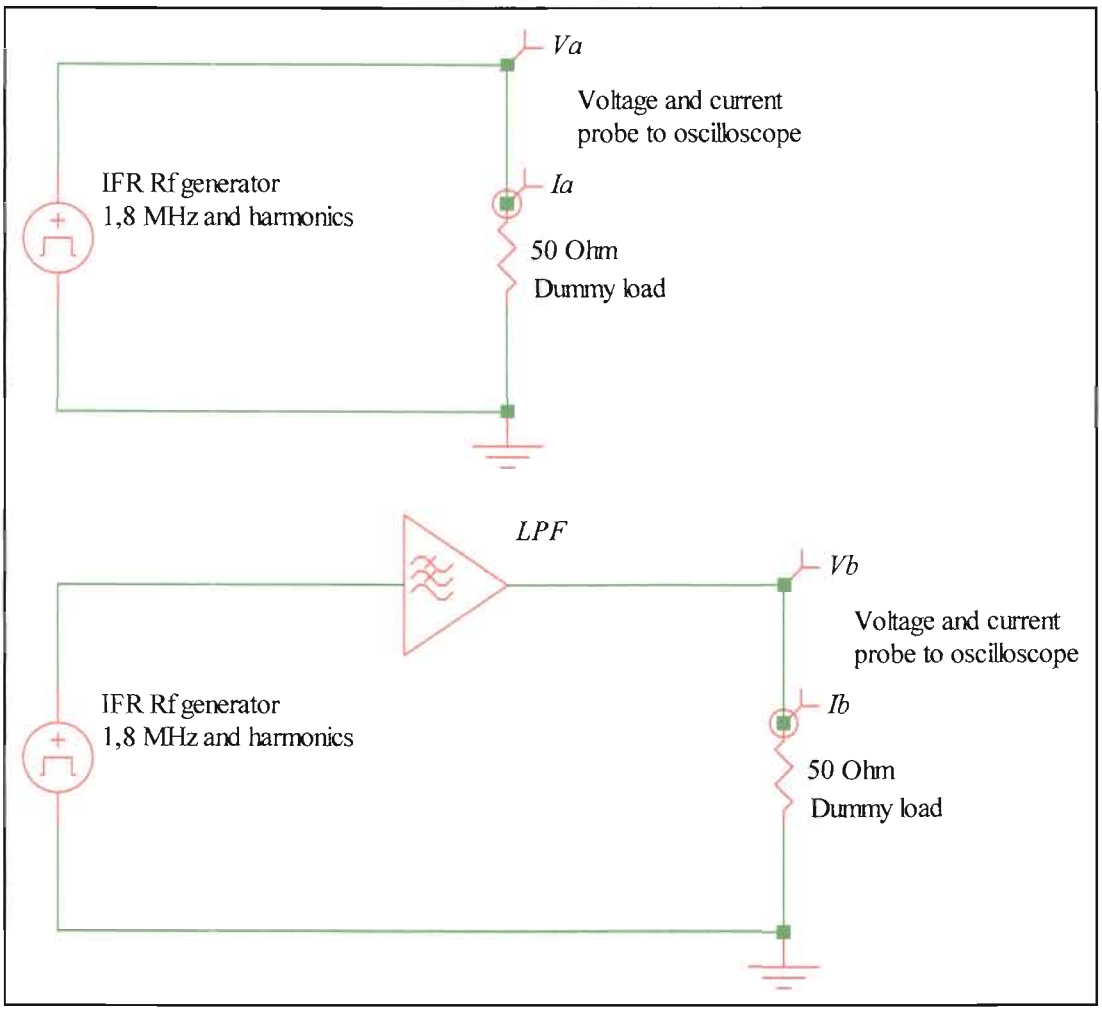

Figure 62 Harmonic analysis test setup

Table 27 Measured values form the harmonic analysis test setup depicted in Figure 62

Frequency under test	Power measurement a	Power measurement b	Filter attenuation
1,8 MHz	5,5 mW	4,2 mW	1,1 dB
3,6 MHz	6,0 mW	30 nW	53,0 dB
5,4 Mhz	6,1 mW	50 nW	50,8 dB
7,2 MHz	6,1 mW	75 nW	49,1 dB
9 MHz	5,4 mW	388 nW	41,4 dB

Table 28 shows the values from Table 16 after rearrangement into the format of Table 27.

Table 28 Reformatted values from Table 16

Frequency under test	Power measurement without LPF	Power measurement with LPF	Attenuation
1,8 MHz	33,7 dBm	34,4 dBm	-0,7 dB
3,6 MHz	23,9 dBm	-24,8 dBm	48,7 dB
5,4 MHz	14,5 dBm	-31,1 dBm	45,6 dB

This shows that the measured results are better than the simulated values. The filter shows an attenuation of 53 dB at the 3,6 Mhz harmonic frequency. This will be sufficient to reach the 60dB prescription, since the second harmonic of the rf output power from the Class E modulated amplifier will be less than the fundamental frequency's power.

4.6 Modulation distortion and AM envelope

Modulation distortion were tested by using the IFR communications service monitor. The modulated 1,8 MHz signal was demodulated to obtain the original modulation frequency on which the distortion is measured. Table 29 gives various readings on different percentage modulation. The tests were carried out using a 1 kHz modulation tone.

From the results given in Table 29 it is seen that, on all modulation percentages, the demodulated frequency deviates less than 1 Hz from the inserted modulation tone. The maximum distortion of 3,6 percent at 80 percent modulation is a rather desirable result.

Table 29 Distortion measurements

Modulation	Demodulated frequency	Distortion	Output power
20 %	1,000 kHz	1,7 %	1,73 W
40 %	1,000 kHz	2,2 %	1,92 W
60 %	1,000 kHz	3,0 %	2,32 W
80 %	1,000 kHz	3,6 %	2,72 W
100 %	1,000 kHz	3,3 %	3,22 W

On the 100 percent modulation measurement (Table 29), the resultant AM envelope was measured on the oscilloscope and is shown in Figure 63. Ch1 represents the output voltage and Ch2 represents the output current. The actual measured output voltage is

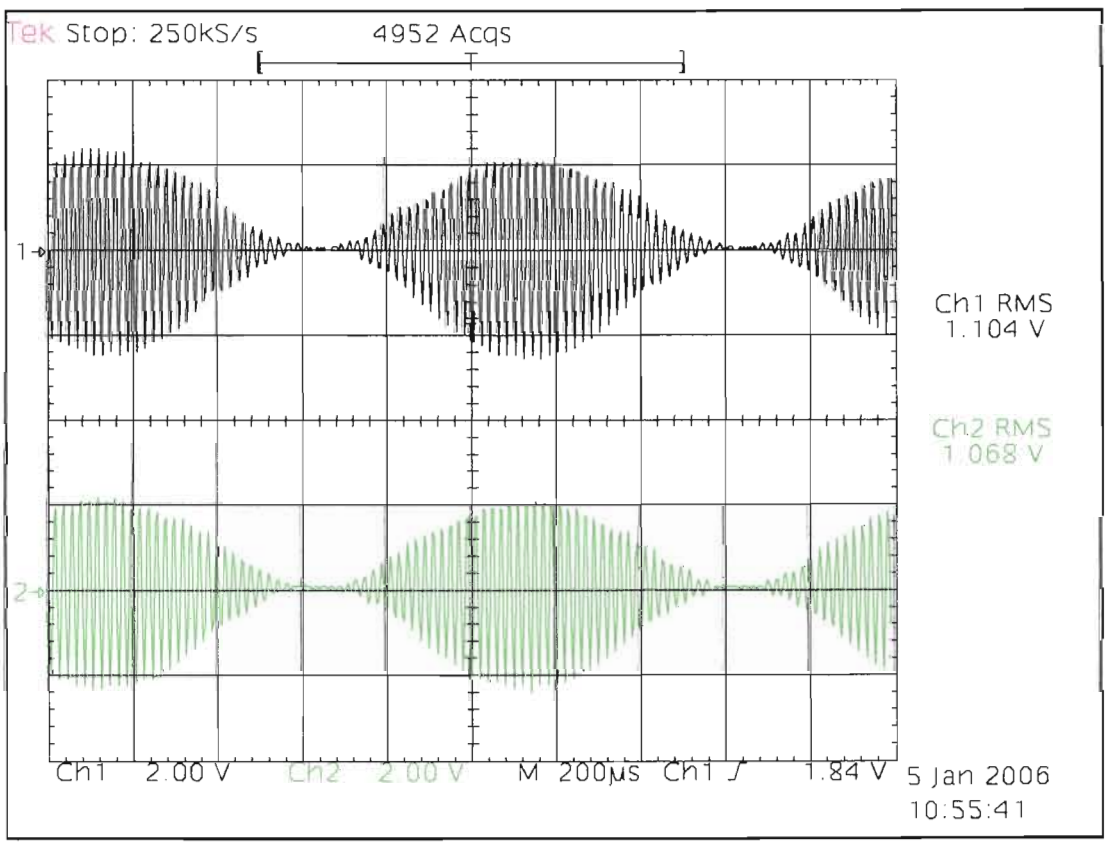

Figure 63 Measured AM envelope on 100 percent modulation

11,04 V and the measured output current is 213,6 mA. The results given in Figure 63 are similar to those depicted in Figure 59, but the measued results shown in Figure 59 were achieved with a 3 kHz modulation tone.

4.7 Summary

Both the calculations and simulations, which were done in previous chapters, were tested in this chapter. The results obtained compare satisfactorily to the calculations and simulations.

Chapter five will give a comprehensive review and conclusion on the high efficiency AM modulated Class E amplifier.

Chapter 5 Conclusions and recommendations

To have an overall overview on the research done, some conclusions concerning the research project will be made as well as recommendations for future research.

5.1 Conclusions

Preliminary to the explanation on the working of Class E amplifiers, it was important to see where Class E amplifiers fit into the general bigger picture. Therefore, a thorough study was made of the different types of amplifiers, which can be divided into non-high and high efficiency amplifiers. The Class E amplifier, which is a high efficiency amplifier, was the amplifier of choice because of certain unique characteristics that it has. The Class E amplifier's operation was discussed in depth, which included a complete discussion of the principle and supporting formulae.

Part of the successful implementation of Class E operation is the switching transistor and the driving thereof. The Mosfet was the obvious choice for the switch, but the carrier generator, or Mosfet driver, was a challenge. The first attempt was the micropower phase-locked loop IC, HCF4046BE, which could not drive the Mosfet. Following attempts included the CD40106BC which is a Hex Schmitt Trigger IC, the CD40106BC with a transistor buffer output and seven dedicated Mosfet driver ICs. The TC4421 IC was the chosen driver IC. To solve the overheating problem associated with the use of the TC4421, a different Mosfet, 540N, with a lower gate input capacitance was chosen and an eight volt regulator was included, to supply the TC4421 and the HCF4046 which generate the carrier frequency.

The Class E amplifier was designed according to the principle and supporting formulae. Together with the amplifier, a harmonic filter was designed. At first an ordinary all-pole network filter, which includes Butterworth and Chebyshev filters, was designed. This

was not effective enough at the first harmonic of 3,6 MHz. The Elliptic-function filter proved to be the answer to the problem, although it is a bit more complex. With this filter, very sharp roll-off characteristics were obtained. Because quite a few inductors were handmade, an equation was derived which gives the length of the coil in terms of the thickness of the wire.

The modulation process in Class E was easy in principle, but difficult to implement in an effective manner. The *RFC* in the form of a transformer was ideal to use for a dual purpose which simultaneously gave the constant current to the Class E configuration and inserted the modulation. A problem arose with the need for a higher value inductor of 18 mH for audio purposes, whereas only 44 uH was needed for the Class E. The higher inductance supported the successful transfer of the audio properties and prevented rf feedback into the audio source. However, it unfortunately also added a higher value DC resistance in series with the load which affected the output power. The Class E *RFC* and audio properties of the transformer were a tradeoff. A lot of effort was made to find a transformer which supported the audio transfer without influencing the output power above an acceptable level.

Tests were done on the Class E characteristics, output and input parameters, the efficiency, harmonic filter and the modulation distortion. All of these results compared quite satisfactory with the simulations done. The overall efficiency was lower than the simulation due to realistic attenuation of the harmonic filter. The Class E had an efficiency on its own of 99,1 percent. Together with the 79,2 percent modulation efficiency and the 1,5 dB *LPF* attenuation, the resultant overall measured efficiency was 60,4 percent.

It was proved that Class E amplifiers can indeed be used in an AM modulated configuration. AM broadcasting or simple transmission is not effective. To combine it with Class E amplifiers makes it much more efficient.

Future work on the high efficiency AM modulated Class E amplifiers would be to implement a channel selection option on the transmitter. It can be transformed into a two-way radio if a pre amp is included for a microphone and a simple AM receiver is built into the unit.

5.2 Recommendations

It is strongly recommended that this work be researched with the aid of the new Silicon Carbide devices. This technology promises to have very useful properties.

A definite research problem on the high efficiency AM modulated Class E amplifier, is the modulation process. With a more effective modulation process the overall efficiency will be drastically improved. An active process instead of the passive transformer could be an option.

Research must be done on the use of the Class E amplifier in a frequency modulated (FM) setup, as it was necessary to damp the unwanted FM signal by filtering the DC supply, in this study.

Most of the Mosfet driver ICs are limited to about 3MHz. More research must be done in this field to have a simple cost-effective Mosfet driver at higher frequencies.

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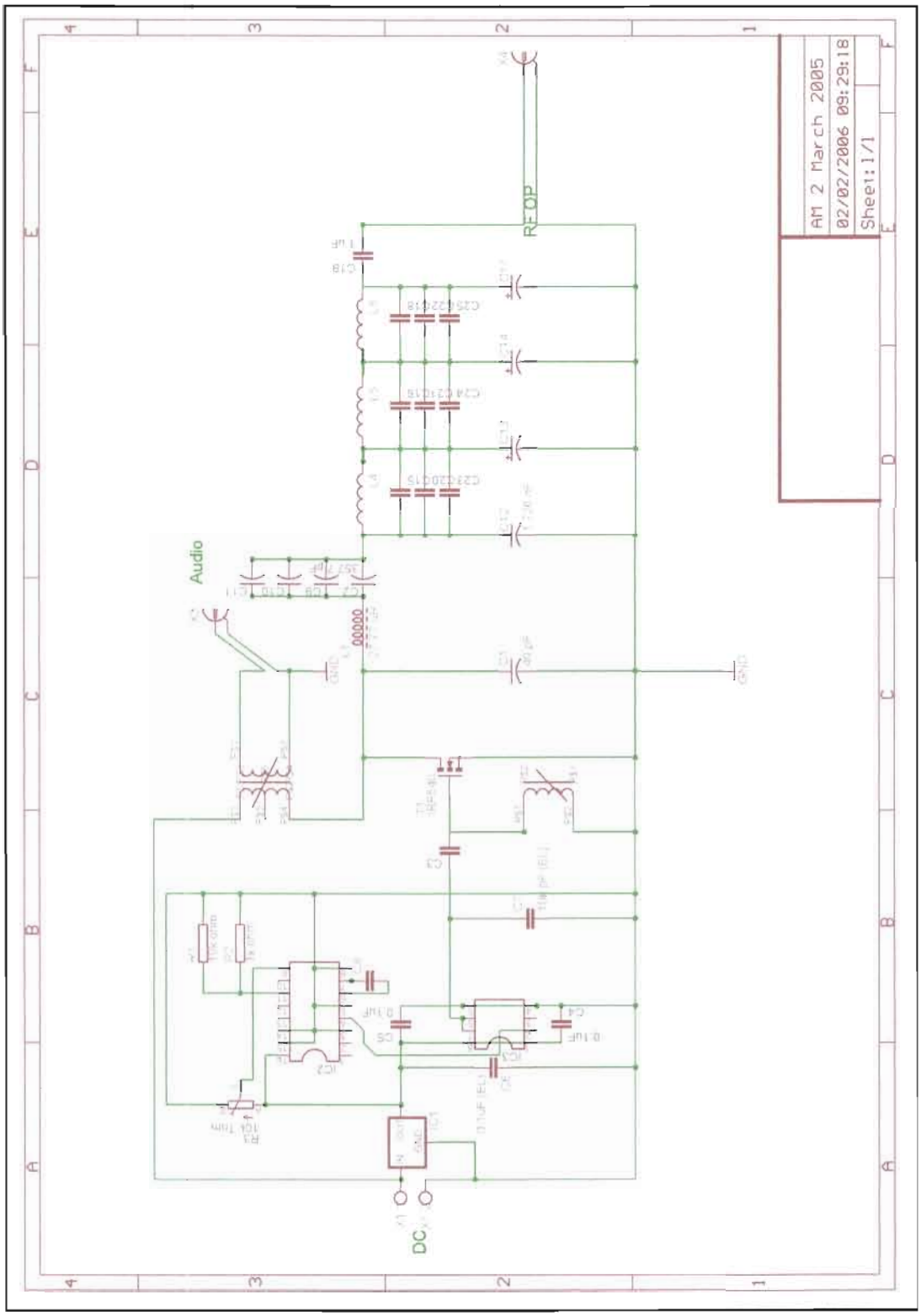


Figure 64 Schematic of PCB

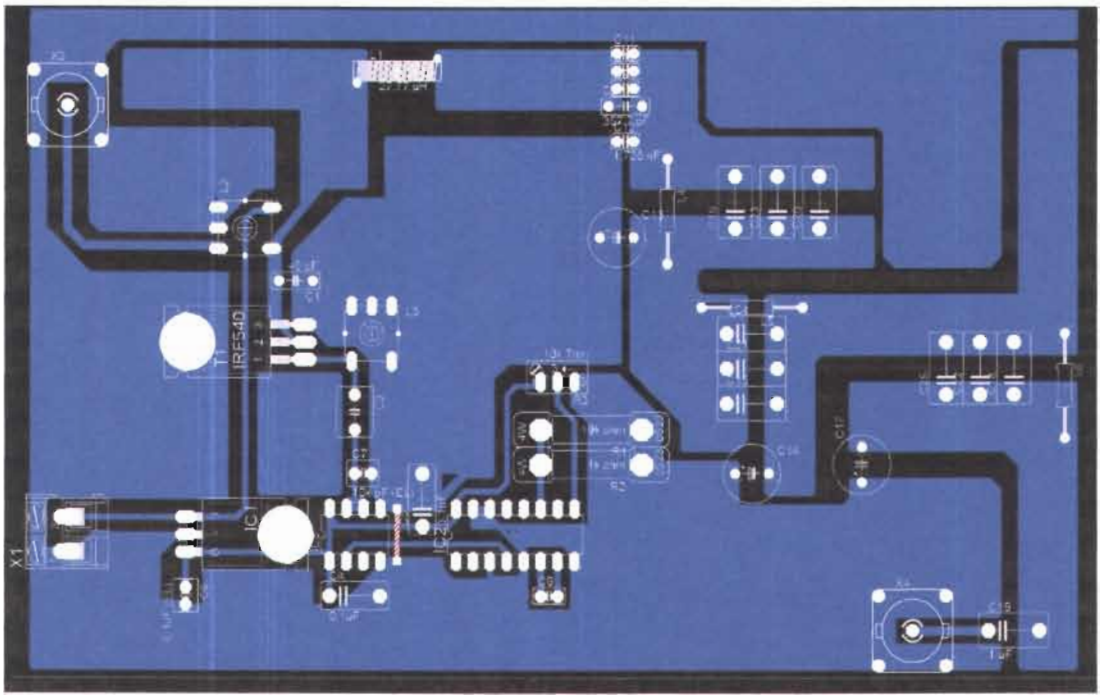


Figure 65 PCB layout

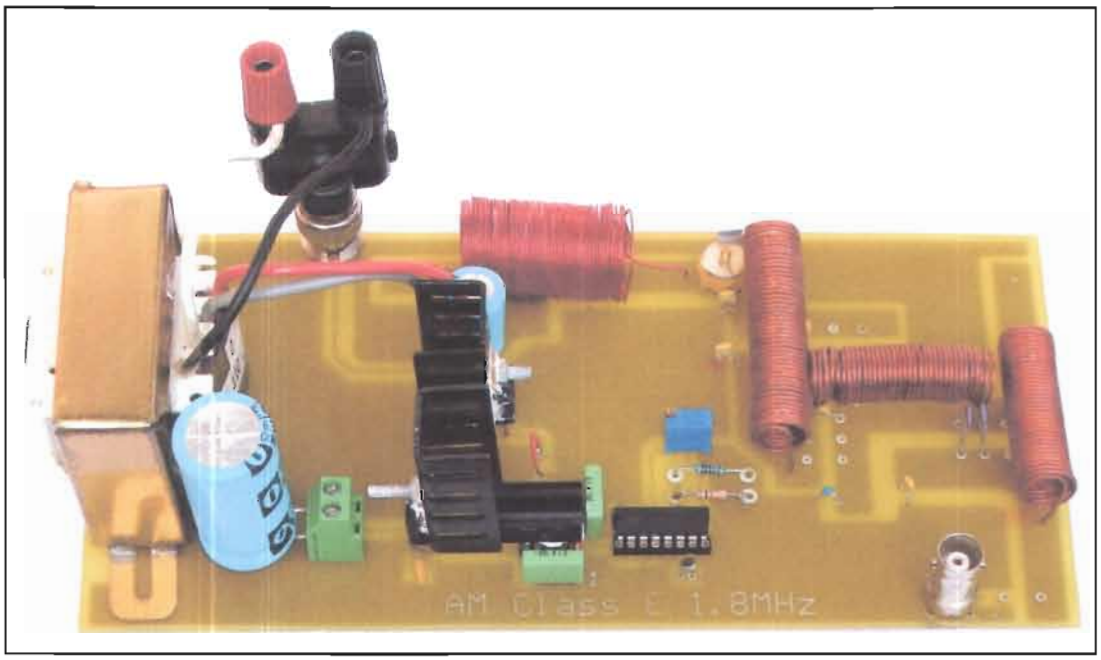
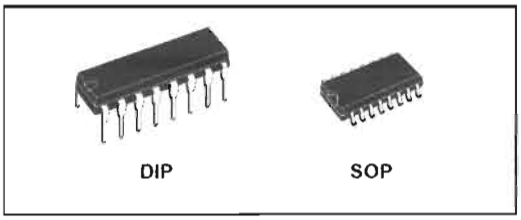


Figure 66 Photograph of the built PCB

HCF4046B

MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED UP TO 20V
- VERY LOW POWER CONSUMPTION : 70µW (TYP.) AT VCO f_o = 10kHz, V_{DD} = 5V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT V_{DD} = 10V
- LOW FREQUENCY DRIFT : 0.04%/°C (typ.) AT V_{DD} = 10V
- CHOICE OF TWO PHASE COMPARATORS : 1) EXCLUSIVE - OR NETWORK 2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY: <1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



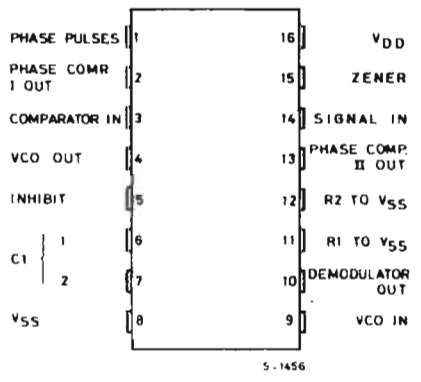
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4046BEY	
SOP	HCF4046BM1	HCF4046M013TR

DESCRIPTION

The HCF4046B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor Technology, available in 16-lead dual in-line plastic or ceramic package. The HCF4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

PIN CONNECTION



VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 KΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the HCF4024B, HCF4018B, HCF4020B, HCF4022B, HCF4029B and HBF4059A. One or more HCF4018B (Presettable Divide-by-N Counter) or HCF4029B (Presettable Up/Down Counter), or HBF4059A (Programmable Divide-by-"N" Counter), together with the HCF4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq$ 30% of (V_{DD}-V_{SS}), logic "1" $\geq$ 70% of (V_{DD}-V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (fo). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2 f_C). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2 f_L). The capture range is $\leq$ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig.1 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of fo is shown in fig.2. Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the

p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig.3 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

Figure 1 : Phase-Comparator I Characteristics at Low-Pass Filter Output.

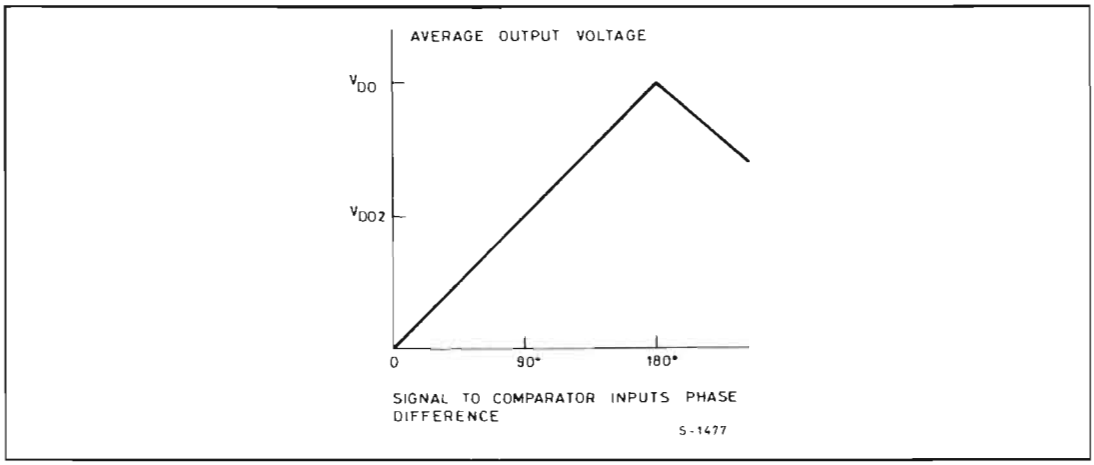


Figure 2 : Typical Waveforms for CMOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of f_o

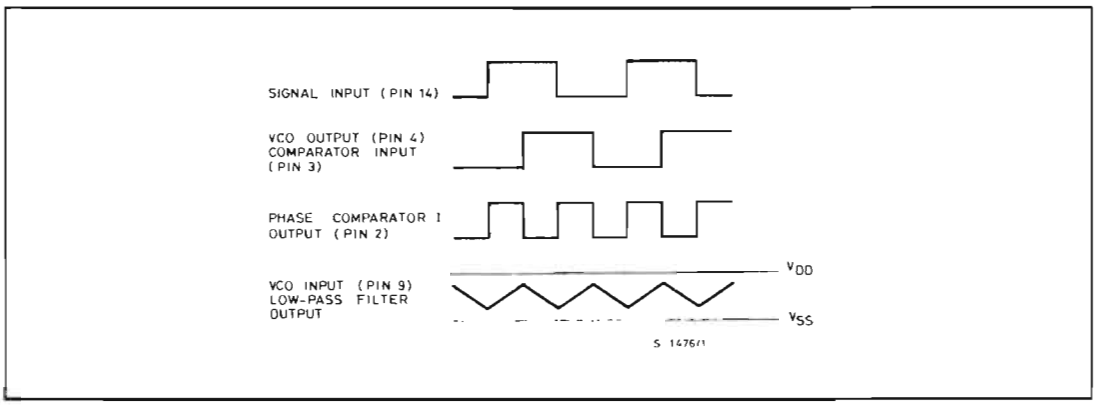
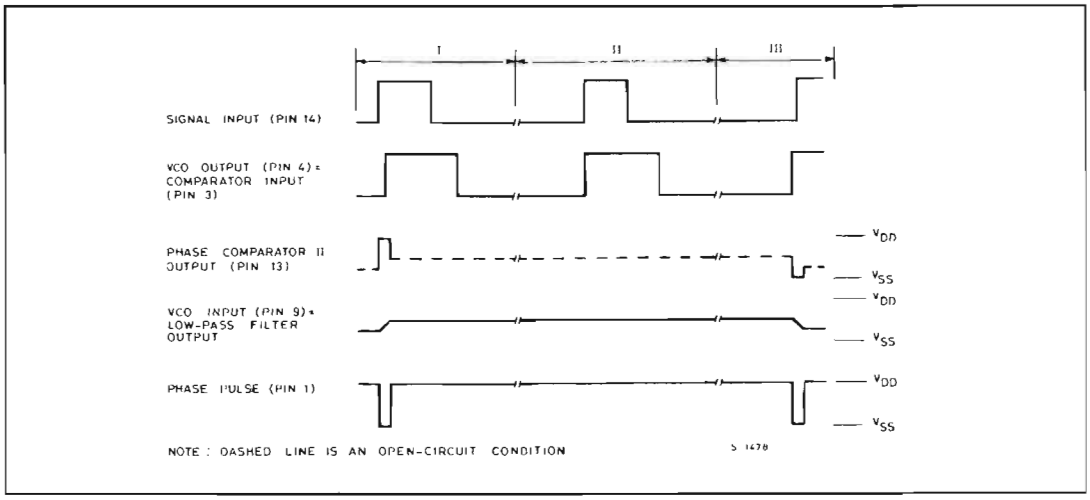
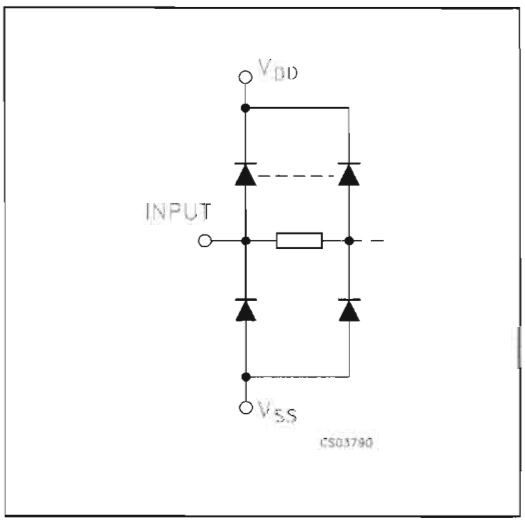


Figure 3 : Typical Waveforms for CMOS Phase-locked Loop Employing Phase Comparator II In Locked Condition



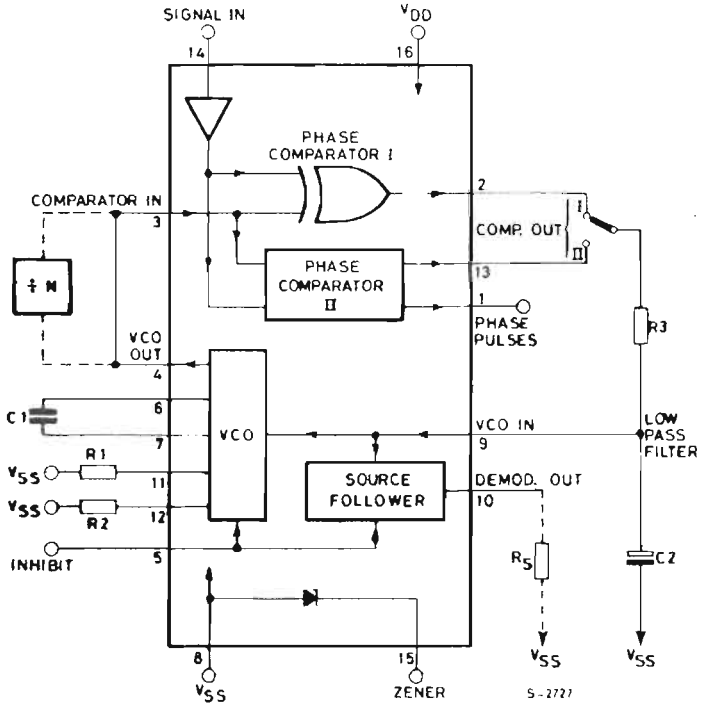
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	PHASE PULSES	Phase Comparator Pulse Output
2	PHASE COMP I OUT	Phase Comparator 1 Output
3	COMPARATOR IN	Comparator Input
4	VCO OUT	VCO Output
5	INHIBIT	Inhibit Input
6, 7	C1	Capacitors
9	VCO IN	VCO Input
10	DEMODULATOR OUT	Demodulator Output
11	R_1 TO V_{SS}	Resistor R1 Connection
12	R_2 TO V_{SS}	Resistor R2Connection
13	PHASE COMP II OUT	Phase Comparator 2 Output
14	SIGNAL IN	Signal Input
15	ZENER	Diode Zener
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
VCO SECTION													
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
PHASE COMPARATOR SECTION													
I_{DD}	Total Device Current Pin 14= Open Pin 5= V_{DD}	0/5			5		0.05	0.1		0.1		0.1	mA
		0/10			10		0.25	0.5		0.5		0.5	
		0/15			15		0.75	1.5		1.5		1.5	
		0/20			20		2	4		4		4	
	Total Device Current Pin 14= V_{SS} or V_{DD} Pin 5= V_{DD}	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000			
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
I_{OUT}	High Impedance Leakage Current	0/18	Any Input		18		$\pm 10^{-4}$	±0.4		±12		±12	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

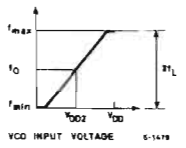
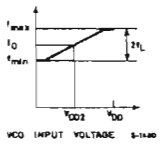
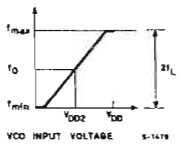
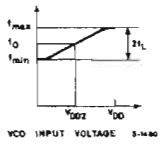
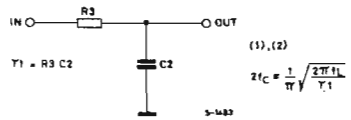
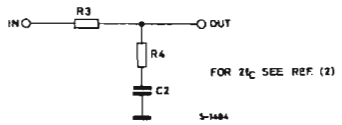
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Condition			Value (*)			Unit
		V_{DD} (V)			Min.	Typ.	Max.	
VCO SECTION								
P_D	Operating Power Dissipation	5	f_O = 10KHz	R1 = 10MΩ		70	140	µW
		10	R2 = ∞	$V_{COIN} = V_{DD}/2$		800	1600	
		15				3000	6000	
f_{MAX}	Maximum frequency	5	R_1 = 10KΩ	C1 = 50pF	0.3	0.6		ns
		10	R2 = ∞	$V_{COIN} = V_{DD}$	0.6	1.2		
		15			0.8	1.6		
		5	R_1 = 5KΩ	C1 = 50pF	0.5	0.8		ns
		10	R2 = ∞	$V_{COIN} = V_{DD}$	1	1.4		
		15			1.4	2.4		
	Center Frequency (f_O) and frequency Range f_{max} - f_{min}	Programable with external components R_1, R_2, and C_1 See Design Information						
	Linearity	5	V_{COIN} =2.5V$^{\pm 0.3}$	R_1 = 10KΩ		1.7		%
		10	V_{COIN} =5V$^{\pm 1}$	R_1 = 100KΩ		0.5		
		10	V_{COIN} =5V$^{\pm 2.5}$	R_1 = 400KΩ		4		
		15	V_{COIN} =7.5V$^{\pm 1.5}$	R_1 = 100KΩ		0.5		
		15	V_{COIN} =7.5V$^{\pm 5}$	R_1 = 1MΩ		7		
	Temperature Frequency Stability (no frequency offset) f_{min} = 0	5				±0.12		%/°C
		10				±0.04		
		15				±0.015		
	Temperature Frequency Stability (frequency offset) f_{min} = 0	5				±0.09		
		10				±0.07		
		15				±0.03		
VCO	Output Duty Cycle	5, 10, 15				50		%
t_{TLH} t_{THL}	VCO Output Transition Time	5				100	200	ns
		10				50	100	
		15				40	80	
	Source Follower Output (Demodulated Output): Offset Voltage V_{COIN}-V_{DEM}	5, 10, 15	R_S > 10KΩ			1.8	2.5	V
	Source Follower Output (Demodulated Output): Linearity	5	R_S = 100KΩ	V_{COIN} =2.5V$^{\pm 0.3}$		0.3		%
		10	R_S = 300KΩ	V_{COIN} =5V$^{\pm 2.5}$		0.7		
		15	R_S = 500KΩ	V_{COIN} =7.5V$^{\pm 5}$		0.9		
V_Z	Zener Diode Voltage		I_Z = 50 µA		4.45	5.5	7.5	V
R_Z	Zener Dynamic Resistance		I_Z = 1 mA			40		Ω

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
PHASE COMPARATOR SECTION							
R14	Pin 14 (signal in) Input Resistance	5		1	2		MΩ
		10		0.2	0.4		
		15		0.1	0.2		
	AC Coupled Signal Input Sensivity (*) (peak to peak)	5	f_{IN} = 100KHz sine wave		180	360	mV
		10			330	660	
		15			900	1800	
t_{PLH}	Propagation Delay Time High to Low Level Pins 14 to 1	5			225	450	ns
		10			100	200	
		15			65	130	
t_{PLH}	Propagation Delay Time Low to High Level	5			350	700	ns
		10			150	300	
		15			100	200	
t_{PHZ}	Disable Time High Level to High Impedance Pins 14 to 13	5			225	450	ns
		10			100	200	
		15			65	130	
t_{PLZ}	Disable Time Low Level to High Impedance	5			285	570	ns
		10			130	260	
		15			95	190	
t_r t_f	Input Rise or Fall Time Comparator Pin 3	5				50	µs
		10				1	
		15				0.3	
	Signal Pin 14	5				500	µs
		10				20	
		15				2.5	
t_{TLH} t_{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

(*) For sine Wave the frequency must be greater than 10KHz for Phase Comparator II

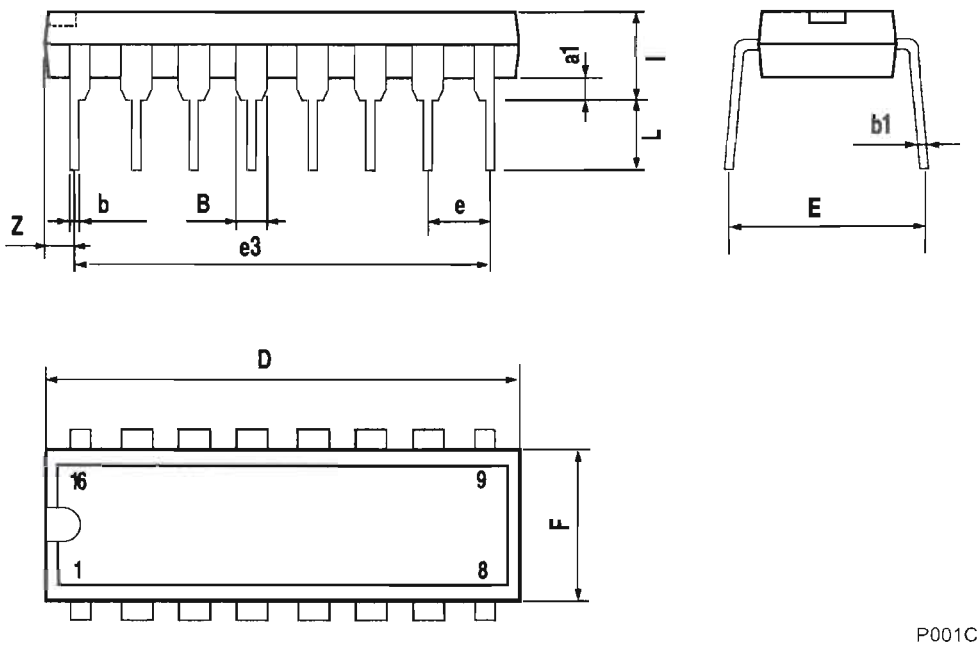
DESIGN INFORMATION This information is a guide for approximating the value of external components in a Phase-Locked-Loop system. The selected external components must be within the following ranges: $5K\Omega \leq R_1, R_2, R_S \leq 1M\Omega$ $C_1 \geq 100pF$ at $V_{DD} \geq 5V$ $C_1 \geq 50pF$ at $V_{DD} \geq 10V$

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL System will Adjust to Centre Frequency f_o		VCO in PLL System will Adjust to Lowest Operating Frequency f_o	
Frequency Lock Range, $2f_L$	$2f_L$ = Full VCO Frequency Range $2fL = f_{max} - f_{min}$			
Frequency Lock Range, $2f_C$			$f_C = f_L$	
Loop filter Component Section				
Phase Angle Between SIgnal and Comparator	90° at Centre frequency (f_O), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Nose Rejection	High		Low	

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ May 1965

Plastic DIP-16 (0.25) MECHANICAL DATA

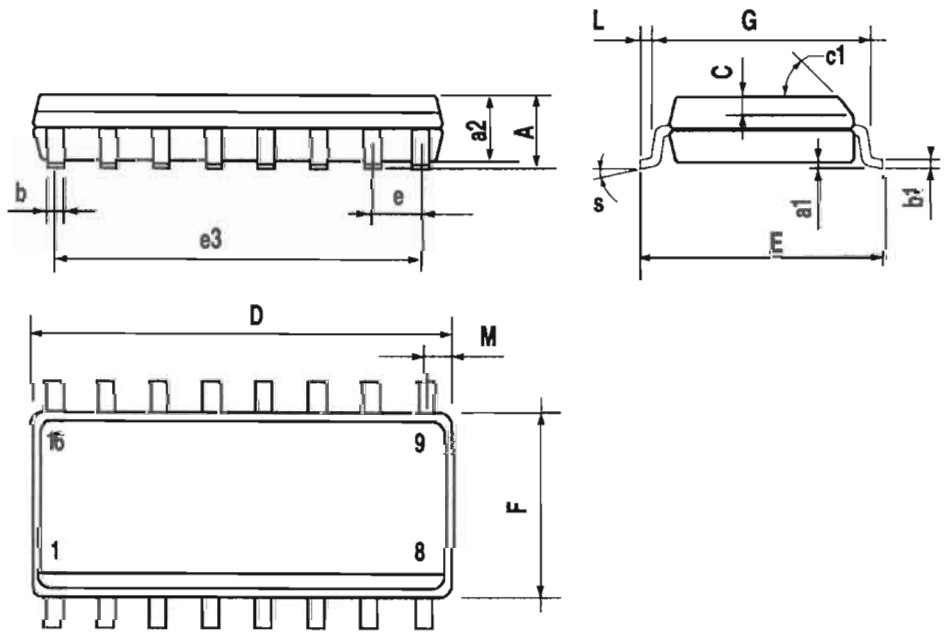
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TelCom Semiconductor, Inc.

TC4421
TC4422

9A HIGH-SPEED MOSFET DRIVERS

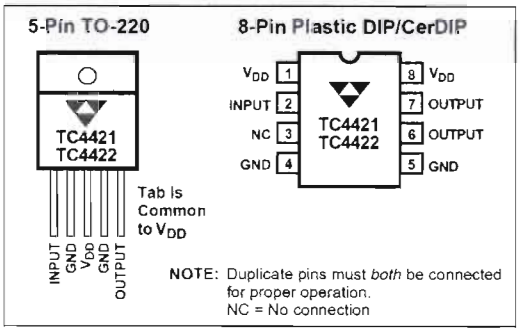
FEATURES

- Tough CMOS™ Construction
- High Peak Output Current 9A
- High Continuous Output Current ..... 2A Max
- Fast Rise and Fall Times:
  - — 30 nsec with 4,700 pF Load
  - — 180 nsec with 47,000 pF Load
- Short Internal Delays ..... 30nsec Typ
- Low Output Impedance ..... 1.4W Typ

APPLICATIONS

- Line Drivers for Extra-Heavily-Loaded Lines
- Pulse Generators
- Driving the Largest MOSFETs and IGBTs
- Local Power ON/OFF Switch
- Motor and Solenoid Driver

PIN CONFIGURATIONS



NOTE: Duplicate pins must *both* be connected for proper operation.
NC = No connection

GENERAL DESCRIPTION

The TC4421/4422 are high current buffer/drivers capable of driving large MOSFETs and IGBTs.

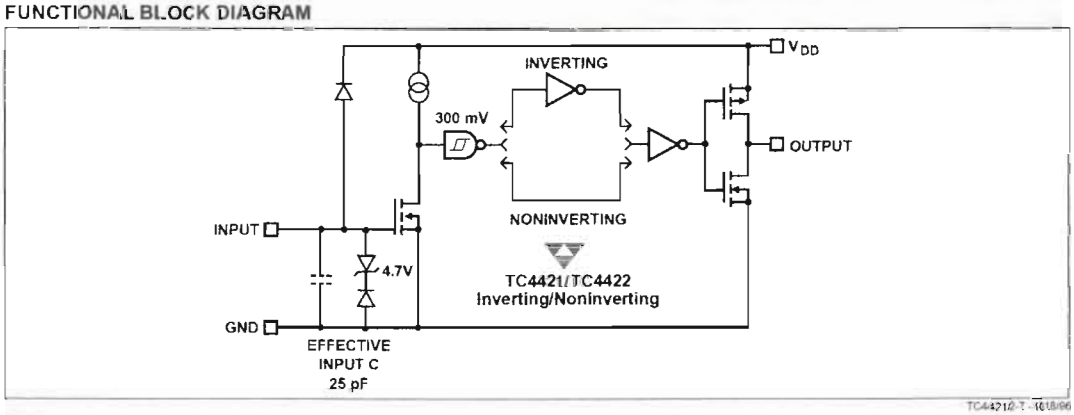
They are essentially immune to any form of upset except direct overvoltage or over-dissipation — they cannot be latched under any conditions within their power and voltage ratings; they are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals; they can accept, without either damage or logic upset, more than 1A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

The TC4421/4422 inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4421CAT	5-Pin TO-220	0°C to +70°C
TC4421CPA	8-Pin PDIP	0°C to +70°C
TC4421EPA	8-Pin PDIP	– 40°C to +85°C
TC4421MJA	8-Pin CerDIP	– 55°C to+125°C
TC4422CAT	5-Pin TO-220	0°C to +70°C
TC4422CPA	8-Pin PDIP	0°C to +70°C
TC4422EPA	8-Pin PDIP	– 40°C to +85°C
TC4422MJA	8-Pin CerDIP	– 55°C to+125°C

FUNCTIONAL BLOCK DIAGRAM



TC4421
TC4422

ABSOLUTE MAXIMUM RATINGS*

Power Dissipation, $T_A \leq 70°C$
- PDIP 730W
- CerDIP 800mW
- 5-Pin TO-220 ..... 1.6W

Power Dissipation, $T_A \leq 70°C$
- 5-Pin TO-220 (With Heat Sink) 1.60W

Derating Factors (To Ambient)
- PDIP ..... 8mW/°C
- CerDIP ..... 6.4mW/°C
- 5-Pin TO-220 ..... 12mW/°C

Thermal Impedance (To Case)
- 5-Pin TO-220 $R_{\theta J-C}$ ..... 10°C/W

Storage Temperature ..... – 65°C to +150°C

Operating Temperature (Chip) ..... 150°C

Operating Temperature (Ambient)
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Lead Temperature (10 sec) ..... 300°C

Supply Voltage 20V

Input Voltage ..... (V_{DD} + 0.3V) to (GND - 5V)

Input Current ($V_{IN} > V_{DD}$) ..... 50 mA

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = 25°C with 4.5V ≤ V_{DD} ≤ 18V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	1.4	—	Ω
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	0.9	1.7	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	9	—	A
I_{DC}	Continuous Output Current	10V ≤ V_{DD} ≤ 18V, T_C = 25° (TC4421/22 CAT only)	2			A
I_{REV}	Latch-Up Protection	Duty Cycle ≤ 2% Withstand Reverse Current	>1500 t ≤ 300 µsec	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	75	nsec
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	75	nsec
t_{D1}	Delay Time	Figure 1	—	30	60	nsec
t_{D2}	Delay Time	Figure 1	—	33	60	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.2	1.5	mA
		V_{IN} = 0V	—	55	150	µA
V_{DD}	Operating Input Voltage		4.5	—	18	V
Input						
V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA

9A HIGH-SPEED MOSFET DRIVERS

ELECTRICAL CHARACTERISTICS (cont.):

Measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	2.4	3.6	W
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	1.8	2.7	W
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	120	nsec
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	120	nsec
t_{D1}	Delay Time	Figure 1	—	50	80	nsec
t_{D2}	Delay Time	Figure 1	—	65	80	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.45	3	mA
		V_{IN} = 0V	—	0.06	0.2	
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

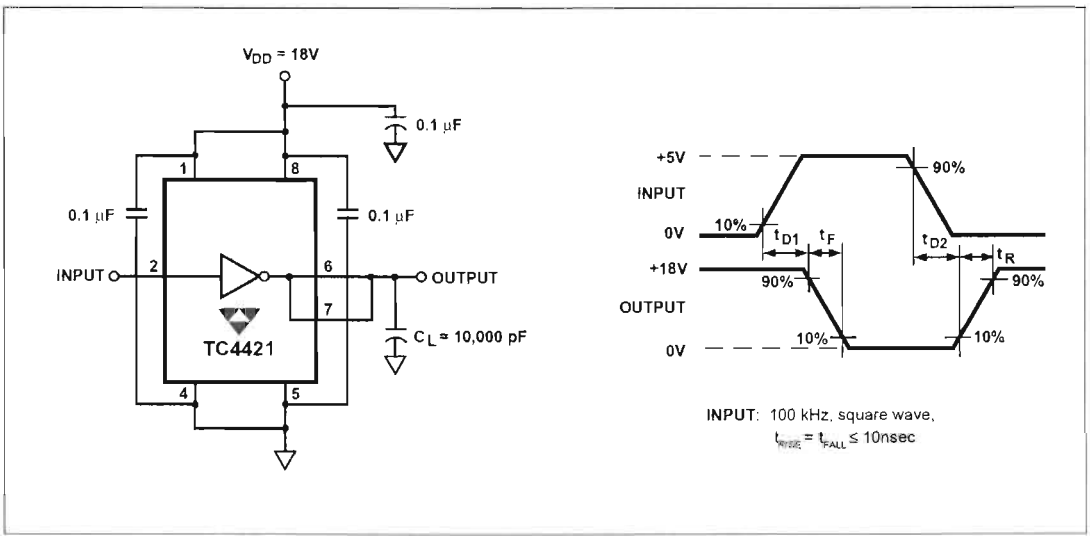
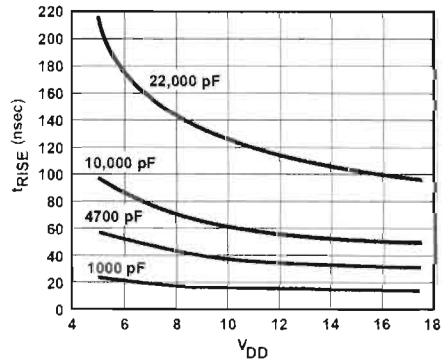


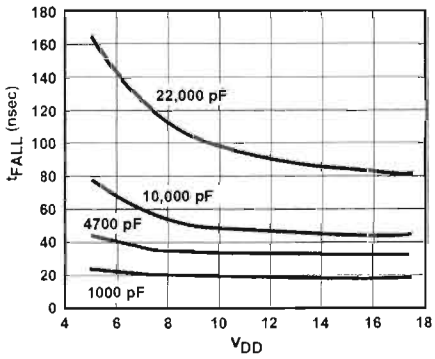
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS

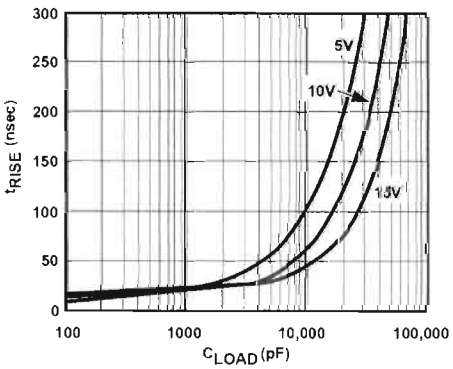
Rise Time vs. Supply Voltage



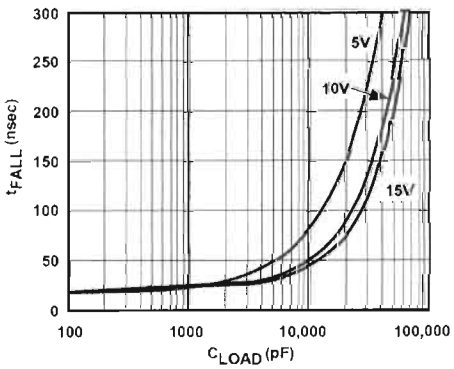
Fall Time vs. Supply Voltage



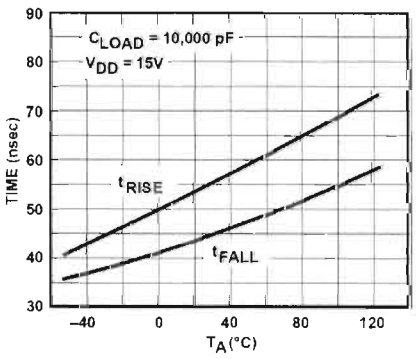
Rise TIme vs. Capacitive Load



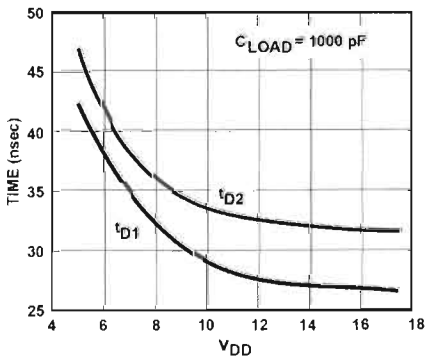
Fall TIme vs. Capacitive Load



Rise and Fall Times vs. Temperature

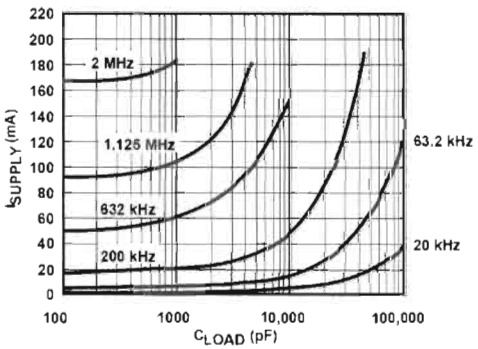


Propagation Delay vs. Supply Voltage

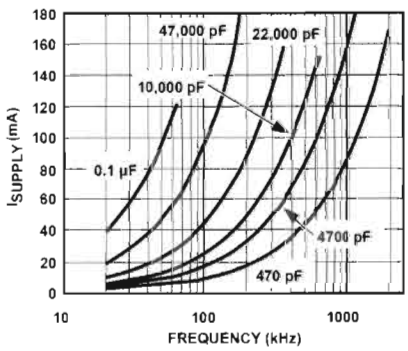


TYPICAL CHARACTERISTICS (Cont.)

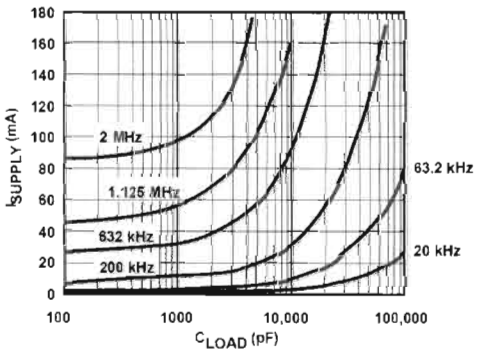
Supply Current vs. Capacitive Load
(V_{DD} = 18V)



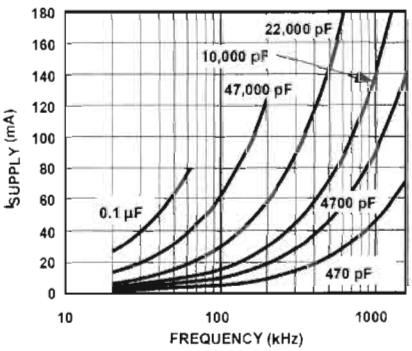
Supply Current vs. Frequency
(V_{DD} = 18V)



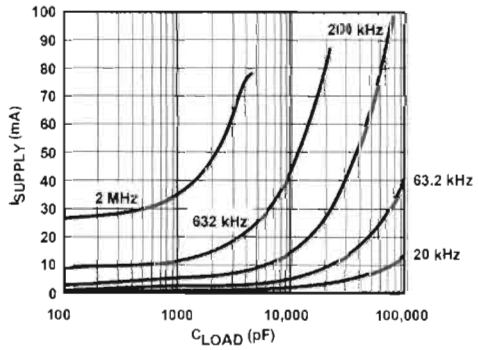
Supply Current vs. Capacitive Load,
(V_{DD} = 12)



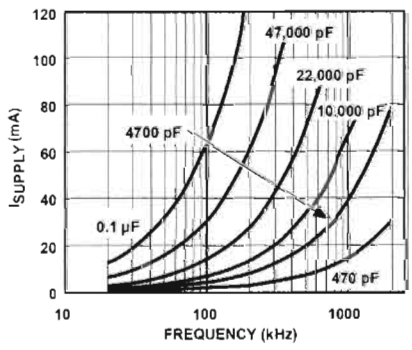
Supply Current vs. Frequency
(V_{DD} = 12)



Supply Current vs. Capacitive Load
(V_{DD} = 6V)

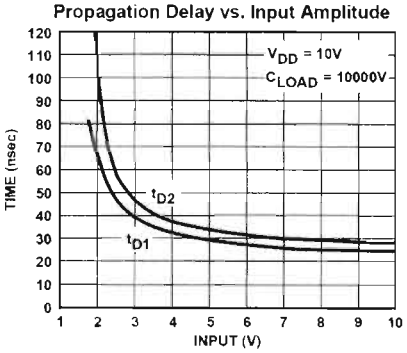


Supply Current vs. Frequency
(V_{DD} = 6V)

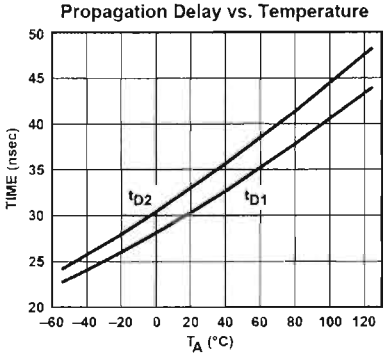


TYPICAL CHARACTERISTICS (Cont.)

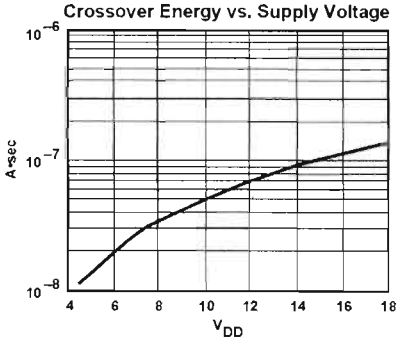
Propagation Delay vs. Input Amplitude



Propagation Delay vs. Temperature

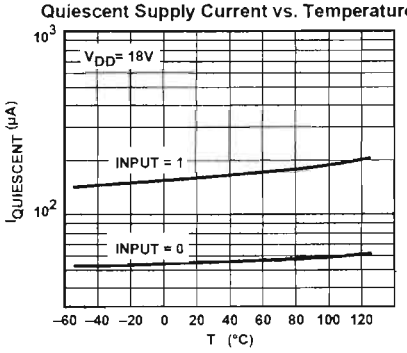


Crossover Energy vs. Supply Voltage



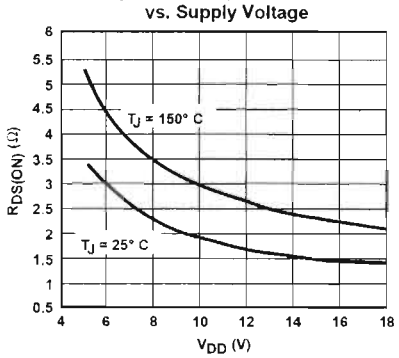
NOTE: The values on this graph represent the loss seen by the driver during a complete cycle. For the loss in a single transition, divide the stated value by 2.

Quiescent Supply Current vs. Temperature

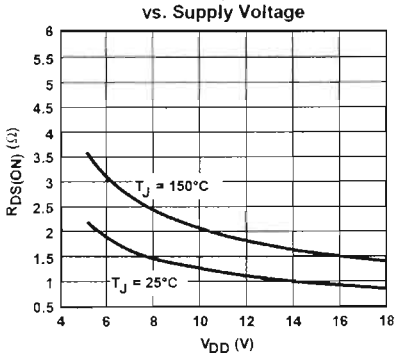


J

High-State Output Resistance vs. Supply Voltage



Low-State Output Resistance vs. Supply Voltage



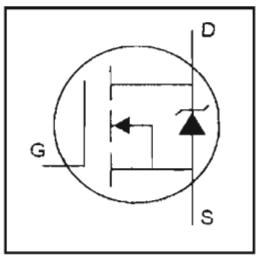
International
IOR Rectifier

PD - 91341B

IRF540N

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 44mΩ

I_D = 33A

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	33	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	23	
I_{DM}	Pulsed Drain Current ①	110	
P_D @T_C = 25°C	Power Dissipation	130	W
	Linear Derating Factor	0.87	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	16	A
E_{AR}	Repetitive Avalanche Energy①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	7.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.15	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

IRF540N

International
IOR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	44	mΩ	V_{GS} = 10V, I_D = 16A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	21	—	—	S	V_{DS} = 50V, I_D = 16A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	71	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	—	—	14		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	21		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 50V
t_r	Rise Time	—	35	—		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		R_G = 5.1Ω
t_f	Fall Time	—	35	—		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1960	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	250	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	40	—		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	700⑤	185⑥	mJ	I_{AS} = 16A, L = 1.5mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	115	170	ns	T_J = 25°C, I_F = 16A
Q_{rr}	Reverse Recovery Charge	—	505	760	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L =1.5mH R_G = 25Ω, I_{AS} = 16A. (See Figure 12)

③ I_{SD} ≤ 16A, di/dt ≤ 340A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

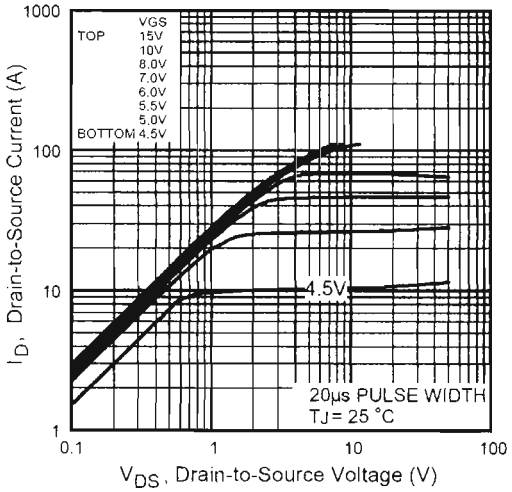


Fig 1. Typical Output Characteristics

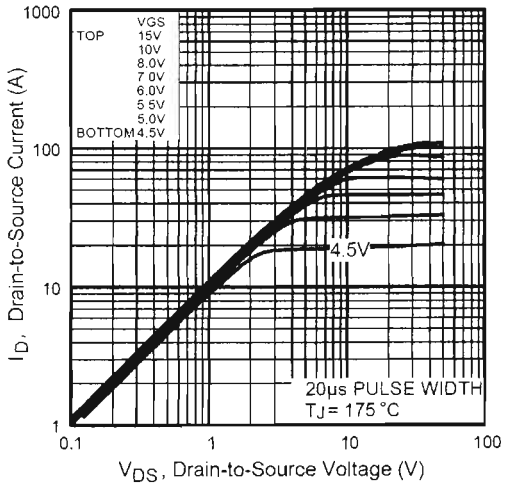


Fig 2. Typical Output Characteristics

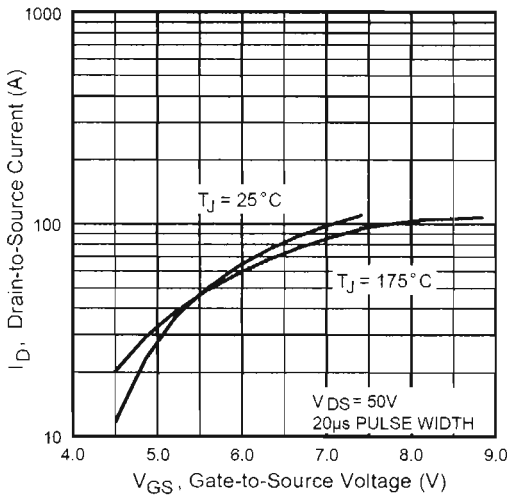


Fig 3. Typical Transfer Characteristics

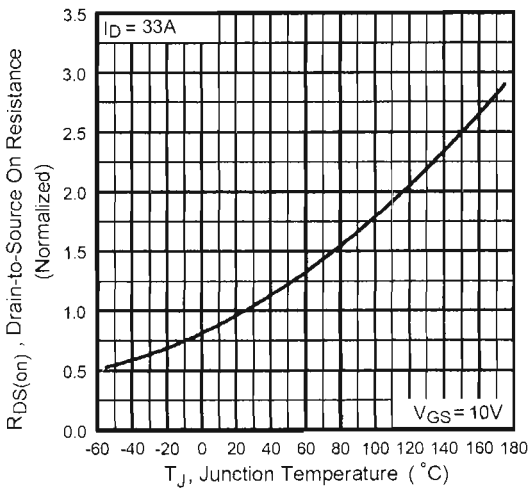


Fig 4. Normalized On-Resistance Vs. Temperature

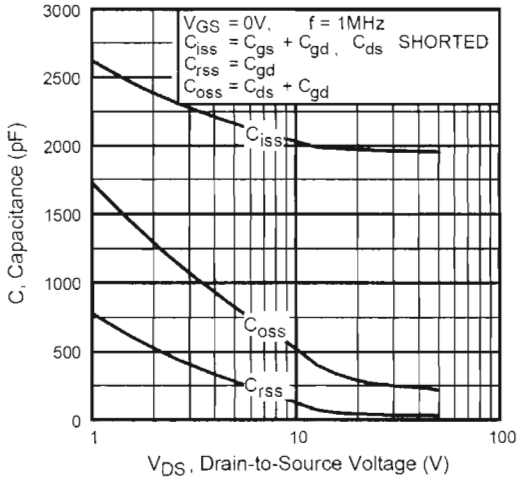


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

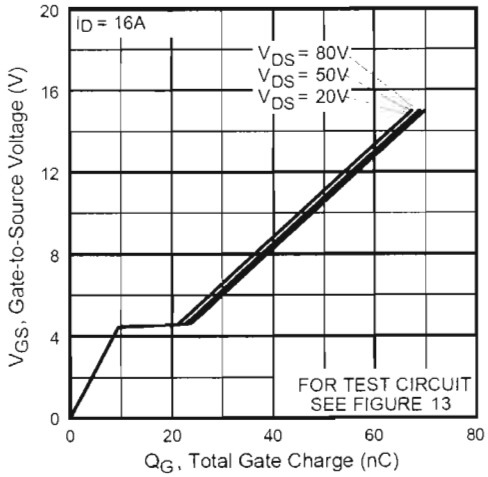


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

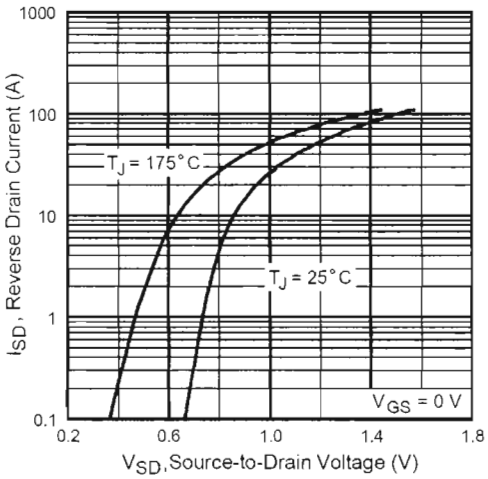


Fig 7. Typical Source-Drain Diode Forward Voltage

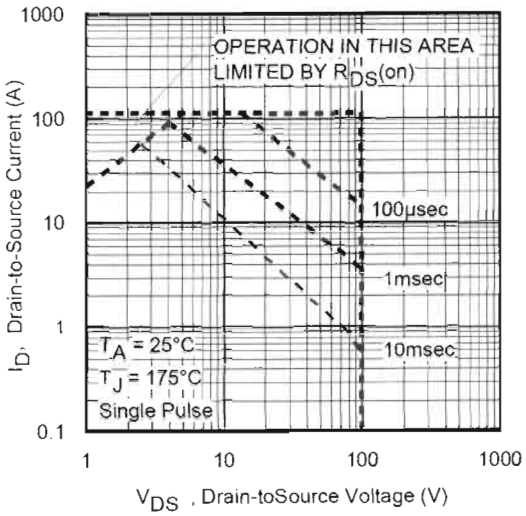


Fig 8. Maximum Safe Operating Area

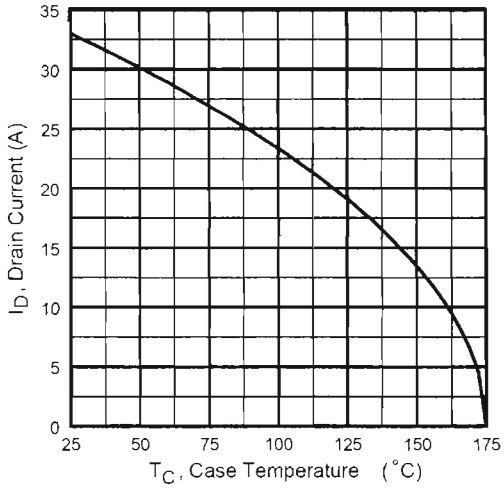


Fig 9. Maximum Drain Current Vs. Case Temperature

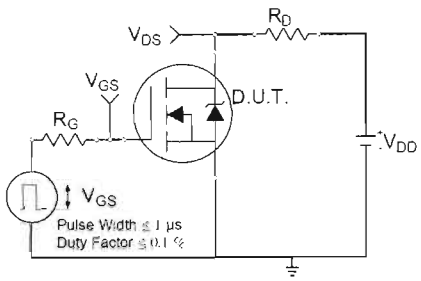


Fig 10a. Switching Time Test Circuit

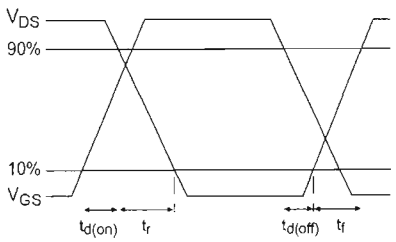


Fig 10b. Switching Time Waveforms

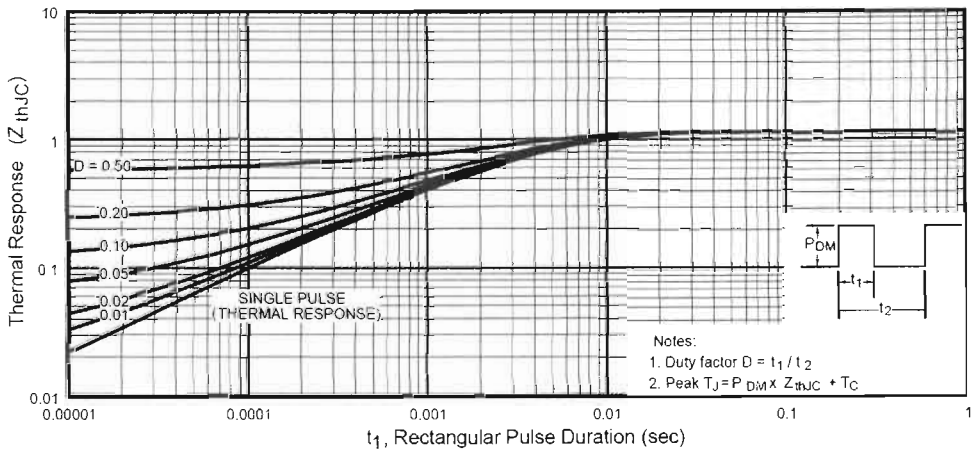


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

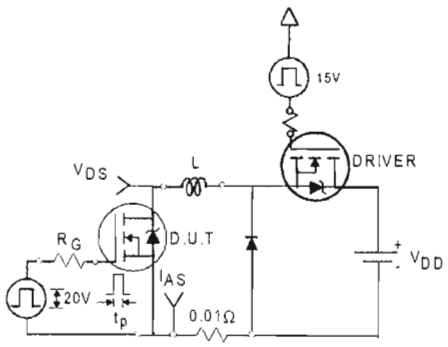


Fig 12a. Unclamped Inductive Test Circuit

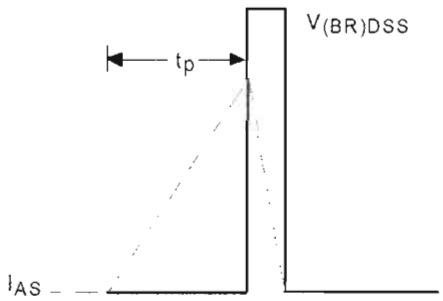


Fig 12b. Unclamped Inductive Waveforms

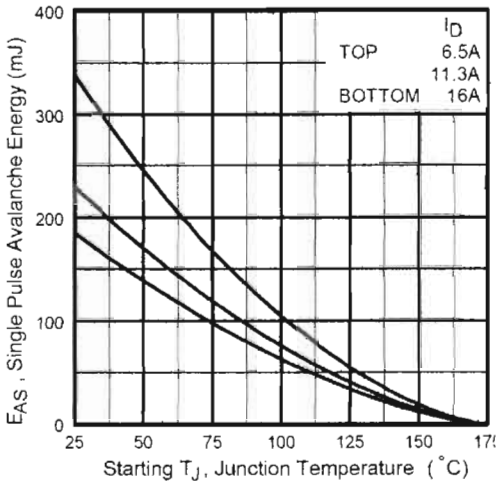


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

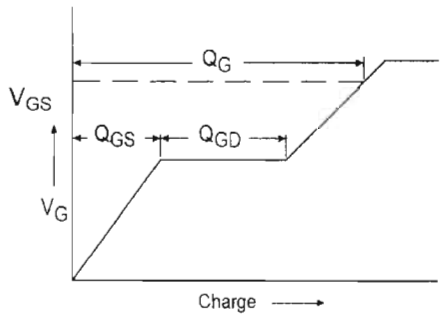


Fig 13a. Basic Gate Charge Waveform

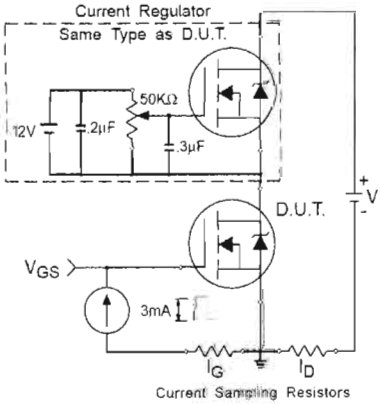
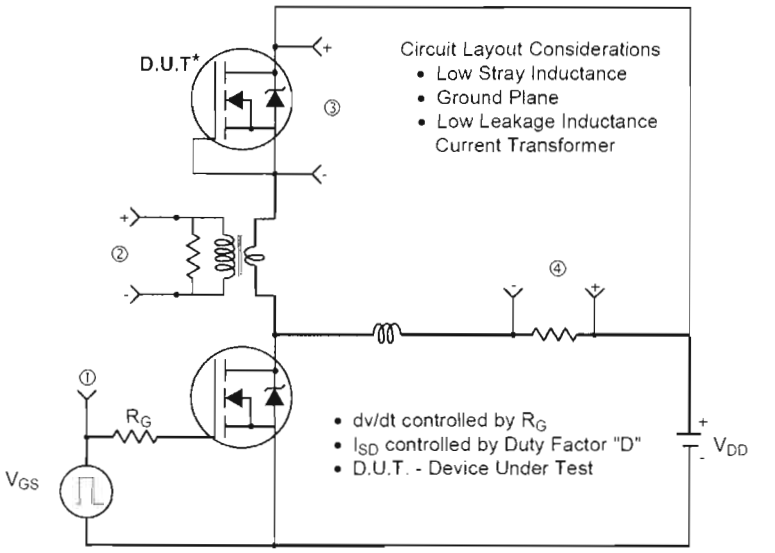
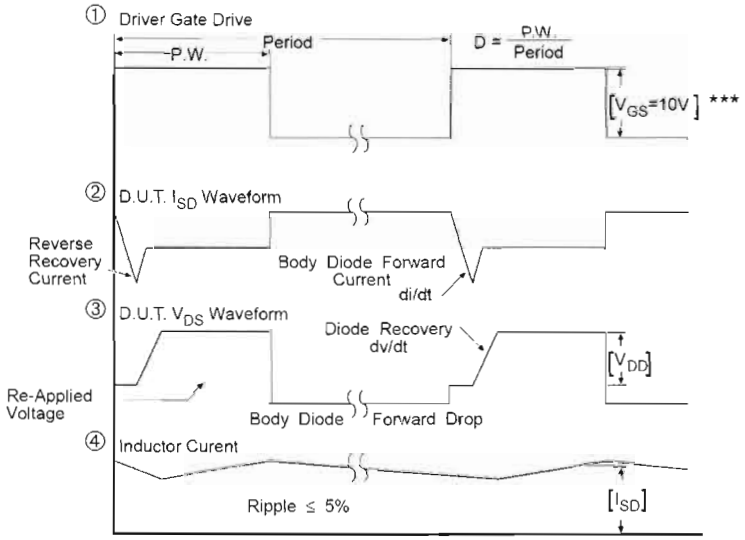


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

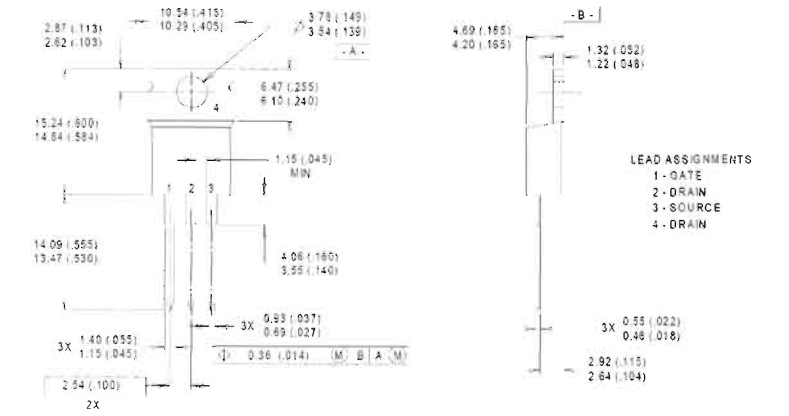
IRF540N

International
IOR Rectifier

Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)

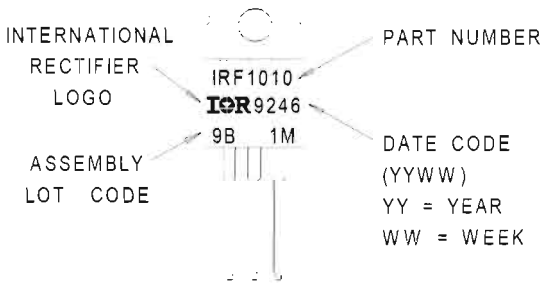


NOTES
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.03/01

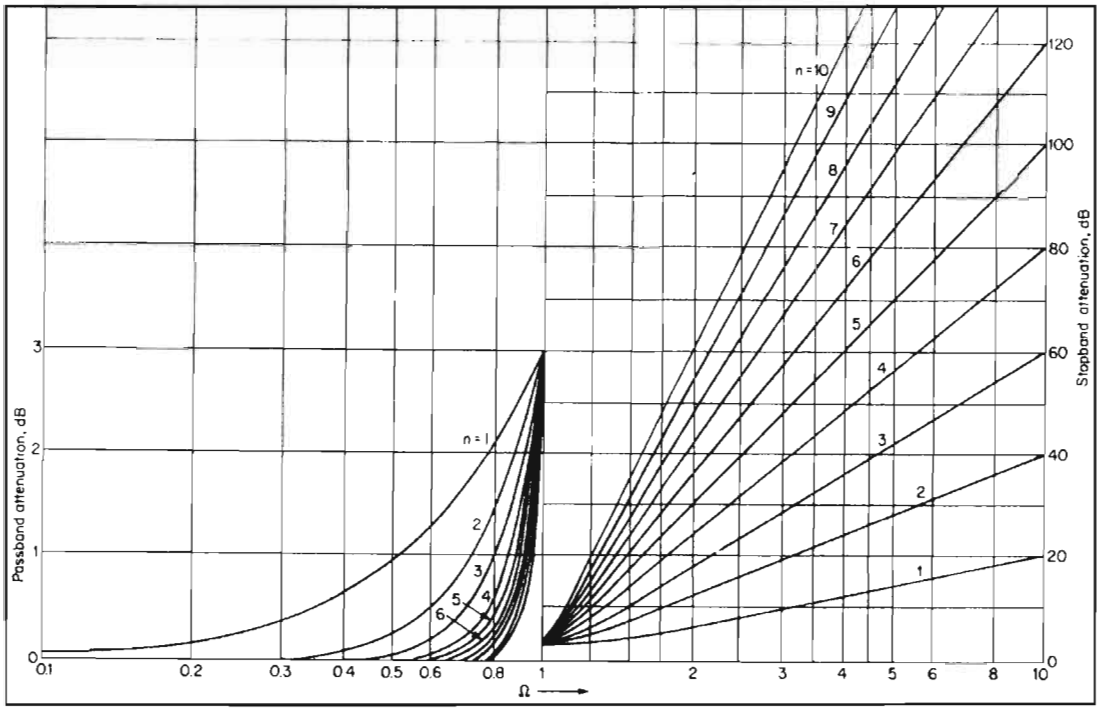


Figure 67 Attenuation characteristics for Butterworth filters (Williams and Taylor, 1995:2.37)

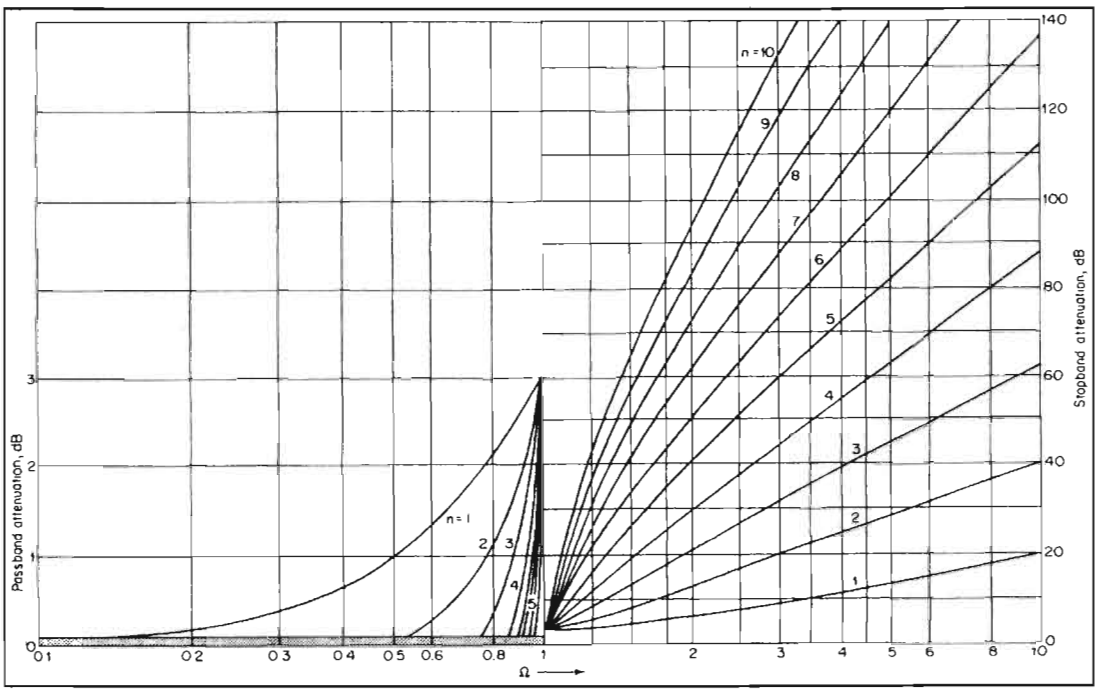
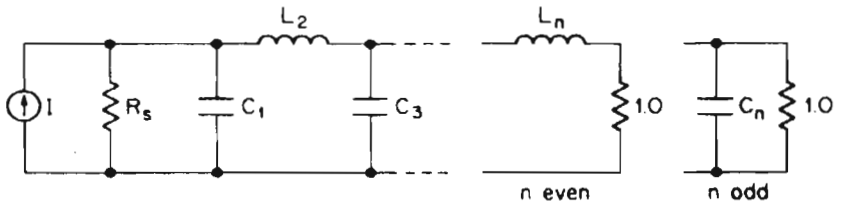


Figure 68 Attenuation characteristics for Chebyshev filters with 0,1dB ripple (Williams and Taylor, 1995:2.46)

Table 30 0,1 dB Chebyshev *LC* element values
(Williams and Taylor, 1995:11.27)



n	R_s	C_1	L_2	C_3	L_4
2	1.3554	1.2087	1.6382		
	1.4286	0.9771	1.9824		
	1.6667	0.7326	2.4885		
	2.0000	0.5597	3.0538		
	2.5000	0.4169	3.8265		
	3.3333	0.2933	5.0502		
	5.0000	0.1841	7.4257		
	10.0000	0.0868	14.4332		
	Inf.	1.3911	0.8191		
3	1.0000	1.4328	1.5937	1.4328	
	0.9000	1.4258	1.4935	1.6219	
	0.8000	1.4511	1.3557	1.8711	
	0.7000	1.5210	1.1927	2.1901	
	0.6000	1.6475	1.0174	2.6026	
	0.5000	1.8530	0.8383	3.1594	
	0.4000	2.1857	0.6603	3.9675	
	0.3000	2.7630	0.4860	5.2788	
	0.2000	3.9418	0.3172	7.8503	
	0.1000	7.5121	0.1549	15.4656	
	Inf.	1.5133	1.5090	0.7164	
4	1.3554	0.9924	2.1476	1.5845	1.3451
	1.4286	0.7789	2.3480	1.4292	1.7001
	1.6667	0.5764	2.7304	1.1851	2.2425
	2.0000	0.4398	3.2269	0.9672	2.8563
	2.5000	0.3288	3.9605	0.7599	3.6976
	3.3333	0.2329	5.1777	0.5602	5.0301
	5.0000	0.1475	7.6072	0.3670	7.6143
	10.0000	0.0704	14.8873	0.1802	15.2297
	Inf.	1.5107	1.7682	1.4550	0.6725

n	$1/R_s$	L_1	C_2	L_3	C_4

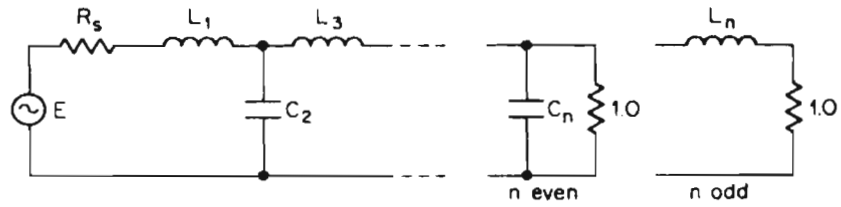
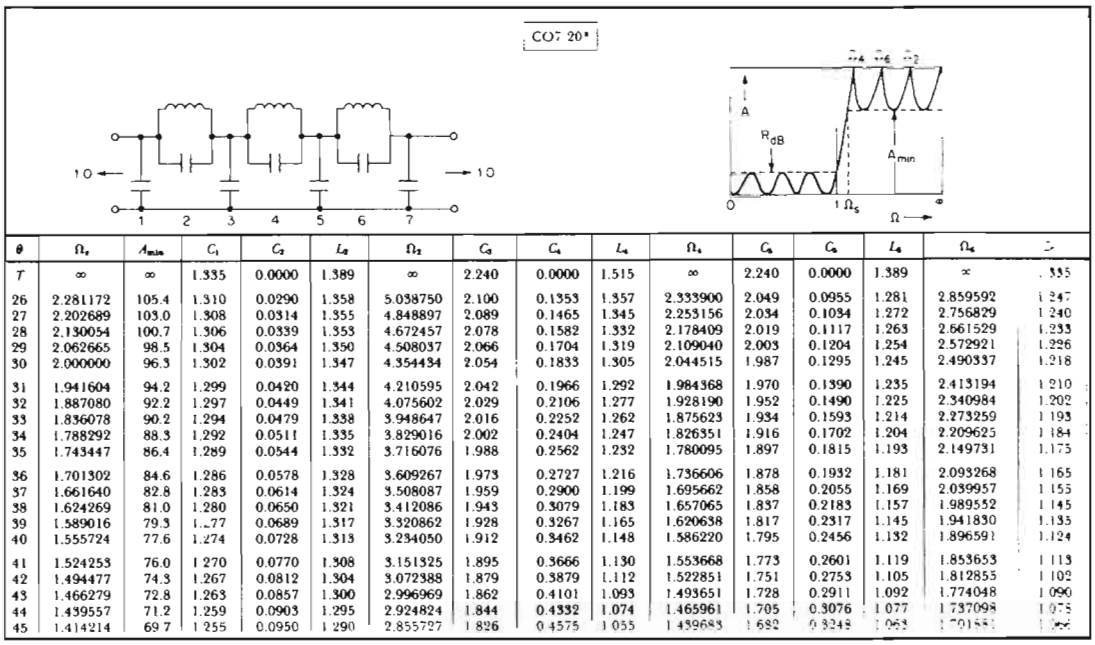


Table 31 Elliptic-function *LC* element values

(Williams and Taylor, 1995:11.90)



θ	Ω_s	A_{min}	C_1	C_2	L_2	Ω_2	C_3	C_4	L_4	Ω_4	C_5	C_6	L_6	Ω_6	∴
T	∞	∞	1.335	0.0000	1.389	∞	2.240	0.0000	1.515	∞	2.240	0.0000	1.389	∞	. 335
26	2.281172	105.4	1.310	0.0290	1.358	5.038750	2.100	0.1353	1.357	2.333900	2.049	0.0955	1.281	2.859592	1 247
27	2.202689	103.0	1.308	0.0314	1.355	4.848897	2.089	0.1465	1.345	2.253156	2.034	0.1034	1.272	2.756829	1 240
28	2.130054	100.7	1.306	0.0339	1.353	4.672457	2.078	0.1582	1.332	2.178409	2.019	0.1117	1.263	2.661529	1.233
29	2.062665	98.5	1.304	0.0364	1.350	4.508037	2.066	0.1704	1.319	2.109040	2.003	0.1204	1.254	2.572921	1.226
30	2.000000	96.3	1.302	0.0391	1.347	4.354434	2.054	0.1833	1.305	2.044515	1.987	0.1295	1.245	2.490337	1.218
31	1.941604	94.2	1.299	0.0420	1.344	4.210595	2.042	0.1966	1.292	1.984368	1.970	0.1390	1.235	2.413194	1 210
32	1.887080	92.2	1.297	0.0449	1.341	4.075602	2.029	0.2106	1.277	1.928190	1.952	0.1490	1.225	2.340984	1.202
33	1.836078	90.2	1.294	0.0479	1.338	3.948647	2.016	0.2252	1.262	1.875623	1.934	0.1593	1.214	2.273259	1 193
34	1.788292	88.3	1.292	0.0511	1.335	3.829016	2.002	0.2404	1.247	1.826351	1.916	0.1702	1.204	2.209625	1 184
35	1.743447	86.4	1.289	0.0544	1.332	3.716076	1.988	0.2562	1.232	1.780095	1.897	0.1815	1.193	2.149731	1.175
36	1.701302	84.6	1.286	0.0578	1.328	3.609267	1.973	0.2727	1.216	1.736606	1.878	0.1932	1.181	2.093268	1 165
37	1.661640	82.8	1.283	0.0614	1.324	3.508087	1.959	0.2900	1.199	1.695662	1.858	0.2055	1.169	2.039957	1 155
38	1.624269	81.0	1.280	0.0650	1.321	3.412086	1.943	0.3079	1.183	1.657065	1.837	0.2183	1.157	1.989552	1 145
39	1.589016	79.3	1.277	0.0689	1.317	3.320862	1.928	0.3267	1.165	1.620638	1.817	0.2317	1.145	1.941830	1.135
40	1.555724	77.6	1.274	0.0728	1.313	3.234050	1.912	0.3462	1.148	1.586220	1.795	0.2456	1.132	1.896591	1.124
41	1.524253	76.0	1.270	0.0770	1.308	3.151325	1.895	0.3666	1.130	1.553668	1.773	0.2601	1.119	1.853653	1 113
42	1.494477	74.3	1.267	0.0812	1.304	3.072388	1.879	0.3879	1.112	1.522851	1.751	0.2753	1.105	1.812855	1 102
43	1.466279	72.8	1.263	0.0857	1.300	2.996969	1.862	0.4101	1.093	1.493651	1.728	0.2911	1.092	1.774048	1 090
44	1.439557	71.2	1.259	0.0903	1.295	2.924824	1.844	0.4332	1.074	1.465961	1.705	0.3076	1.077	1.737098	1.078
45	1.414214	69.7	1.255	0.0950	1.290	2.855727	1.826	0.4575	1.055	1.439683	1.682	0.3248	1.063	1.701881	1.066

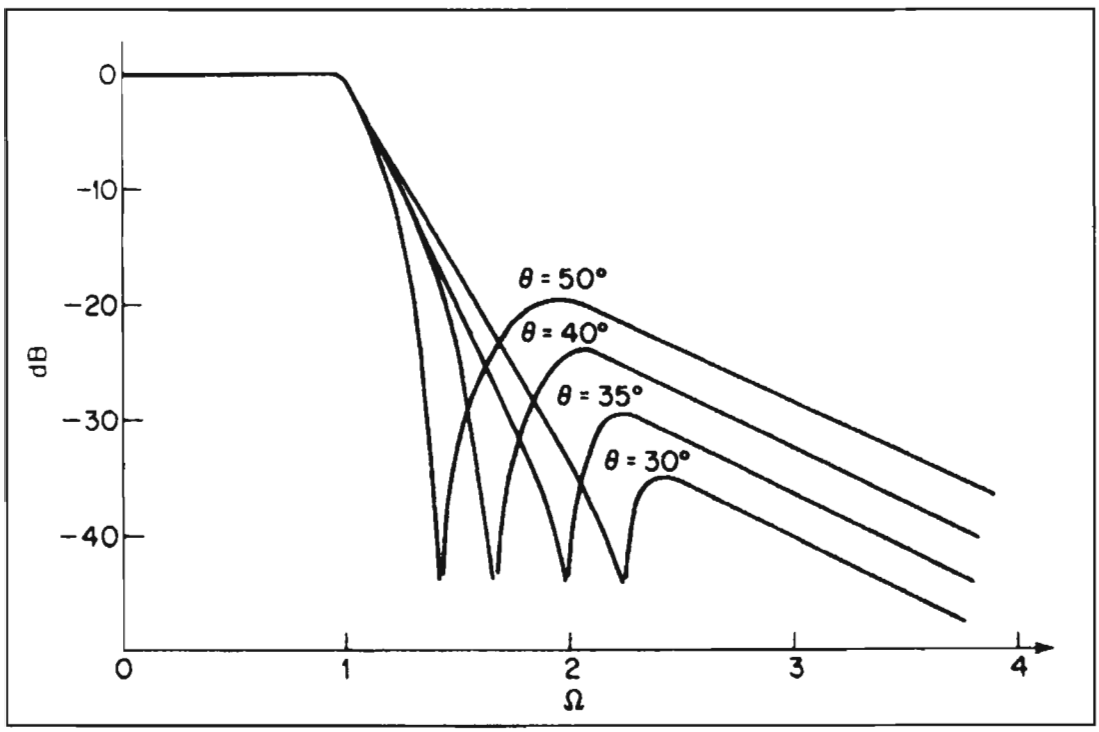


Figure 69 Elliptic-function low pass response, illustrating θ
(Williams and Taylor, 1995:2.77)

Simple rf current probe

A design of a simple rf current probe is given by Ordy (2002:1). [Online]. Available at: <http://www.seed-solutions.com/gregordy/Amateur%20Radio/Experimentation/RFProbe.htm:>

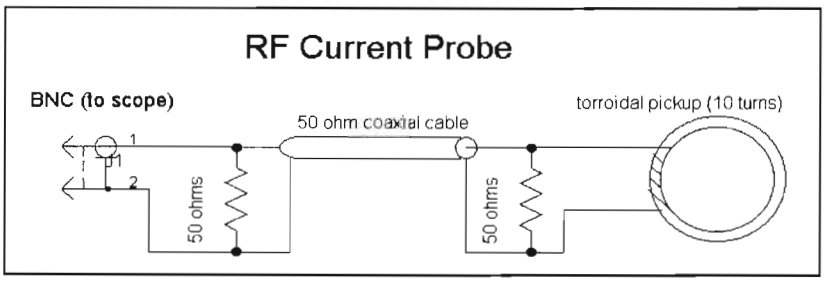


Figure 70 Schematic of simple rf current probe (Ordy, 2002:1)

The schematic is given in Figure 70 by Ordy (2001:1) The built rf current probe which was used for the measurements done in Chapter 4 is shown in Figure 71. This probe was calibrated at the Randse Afrikaanse Universiteit to a commercial Tektronix current probe.

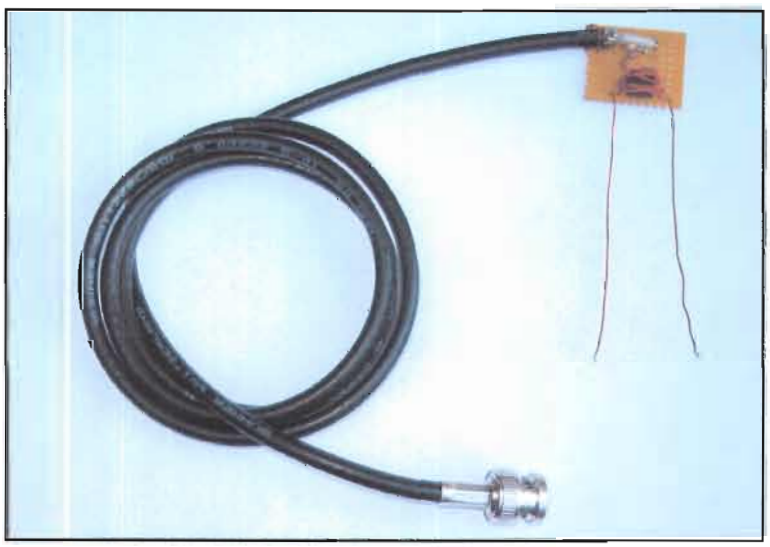


Figure 71 Simple rf current probe

Amplitude modulation background

In this annexure the background theory on AM is considered. This include the AM principles, modulation factor and the power in AM waves. Recalling from chapter one, only Amplitude Modulation with double side band and full carrier wave is considered, also known as double side band full carrier (DSBFC).

The following will be covered:

- Principles of AM
- Modulation factor
- Power in AM waves

1 Principles of AM

Amplitude modulation is accomplished when a signal amplitude is modulating the amplitude of a radio carrier wave at an appropriate frequency.

The general expression for a sinusoidal carrier wave is given by Green (1985:2):

$$v = V_{cr} \sin(\omega_c t + \theta) \text{ V} \quad \textbf{(33)}$$

The variables in equation (33) represent the following:

- v - instantaneous carrier voltage
- V_{cr} - peak value of v or amplitude of the carrier voltage
- θ - phase of the carrier voltage at time $t = 0$. Here, θ will be taken as zero
- ω_{cr} - 2π times the carrier frequency

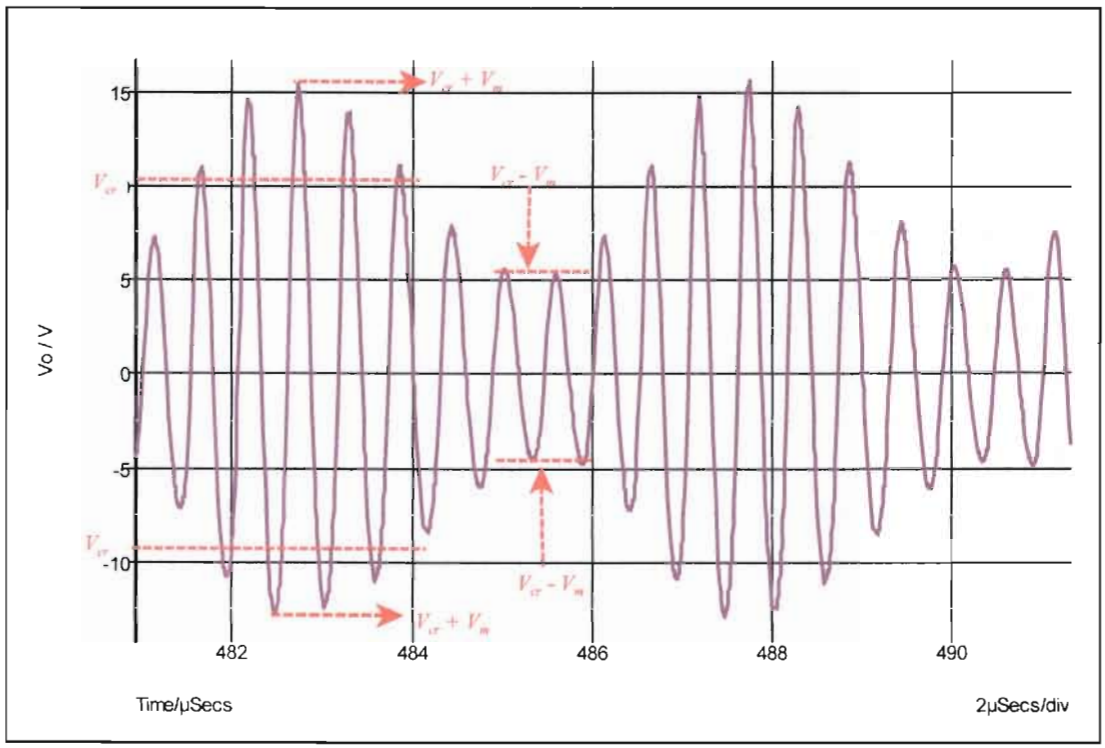


Figure 72 An amplitude modulated wave

For modulation the carrier voltage must be varied in accordance with the characteristics of the modulating signal. Suppose the modulating signal is sinusoidal and is given by (Green, 1985:2):

$$v = V_m \sin \omega_m t \ \text{V} \qquad \textbf{(34)}$$

where V_m is the peak modulating value and ω_m is 2π times the modulating frequency. Green (1985:2) further states that the amplitude of the carrier must then vary sinusoidally about a mean value of V_{cr} volts (Figure 72). The peak value of this variation should be V_m volts, and the frequency of the variation should be $\omega_m/2\pi$ hertz. The amplitude A of the modulated carrier wave is therefore:

$$A = V_c + V_m \sin \omega_m t \qquad \textbf{(35)}$$

and the expression of the instantaneous voltage of an amplitude modulated wave is:

$$v = (V_{cr} + V_m \sin \omega_m t) \sin \omega_{cr} t \ \text{V} \qquad \textbf{(36)}$$

multiplying out results in:

$$v = V_{cr} \sin \omega_{cr} t + V_m \sin \omega_m t \sin \omega_{cr} t \ \text{V} \qquad \textbf{(37)}$$

Recalling trigonometric identity:

$$2 \sin A \sin B = \cos(A - B) - \cos(A + B)$$

equation (37) can be rewritten as:

$$v = \left[V_{cr} \sin \omega_{cr} t + \frac{V_m}{2} \cos(\omega_{cr} - \omega_m)t - \frac{V_m}{2} \cos(\omega_{cr} + \omega_m)t \right] \text{V} \qquad \textbf{(38)}$$

Equation (38) shows that a sinusoidally modulated carrier wave contains components at three different frequencies (Green, 1985:2) Note that the modulating frequency, f_m, is not present. The three frequencies are:

- original carrier frequency, $f_{cr} = \omega_{cr} / 2\pi$
- lower side frequency, $f_{cr} - f_m = (\omega_{cr} - \omega_m) / 2\pi$
- upper side frequency, $f_{cr} + f_m = (\omega_{cr} + \omega_m) / 2\pi$

The maximum amplitude of the modulated wave occurs when sin ω_mt = 1, which is $V_{cr} + V_m$. The minimum amplitude occurs when sin ω_mt = -1, which is $V_{cr} - V_m$.

Figure 72 shows the waveform of a sinusoidally modulated wave, the outline of the wave is known as the modulation envelope. The modulating envelope has the same waveform as the original modulating signal.

When the wave is displayed on amplitude versus frequency then the band of the side frequencies below the carrier frequency is known as the lower side band, while the band above the carrier forms the upper side band.

2 Modulation factor

The modulated wave in Figure 72 shows the modulation as V_m. As V_{cr} - V_m approaches zero the higher the modulation. The amount of modulation can be given as the modulation factor, m, with A as the amplitude and can be expressed as:

$$m = \frac{\max A - \min A}{\max A + \min A} \qquad \textbf{(39)}$$

When equation (39) is expressed as a percentage, m is known as the percentage modulation, or the depth of modulation.

The maximum amplitude in equation (39) is $V_{cr} + V_m$ and the minimum amplitude is V_{cr} - V_m. Equation (39) can be restated as:

$$\begin{aligned} m &= \frac{(V_{cr} + V_m) - (V_{cr} - V_m)}{(V_{cr} + V_m) + (V_{cr} - V_m)} \\ &= \frac{V_m}{V_{cr}} \end{aligned} \qquad \textbf{(40)}$$

If m is one, or 100 percent modulation occurs then $V_{cr} = V_m$.

3 Power in AM waves

Green (1985:8) states that if the RMS voltage of an amplitude modulated wave is V, then the total power, P_t, dissipated by that wave in a resistance R is given by:

$$\begin{aligned} P_t &= \frac{V^2}{R} \\ &= P_{cr}(1+\frac{1}{2}m^2) \text{ W} \end{aligned} \tag{41}$$

The power dissipated by the carrier component alone is:

$$P_{cr} = \frac{{V_{cr}}^2}{2R} \text{ W}$$

Therefore:

$$\begin{aligned} \frac{P_t}{P_{cr}} &= \frac{2V^2}{{V_{cr}}^2} = \frac{P_{cr}(1+\frac{1}{2}m^2)}{P_{cr}} \\ 2V^2 &= {V_{cr}}^2(1+\frac{1}{2}m^2) \\ V &= \frac{V_{cr}}{\sqrt{2}}\sqrt{1+\frac{1}{2}m^2} \text{ V} \end{aligned} \tag{42}$$

Equation (41) can be rewritten when 100 percent modulation is used. Thus, m will be equal to one:

$$\begin{aligned} P_t &= P_{cr}(1+\frac{1}{2}m^2) \\ &= P_{cr}(1+\frac{1}{2}1^2) \\ &= \frac{3}{2}P_{cr} \text{ W} \end{aligned}$$

but:

$$\begin{aligned} P_t &= P_{cr} + P_m \\ P_m &= P_t - P_{cr} \\ &= \frac{3}{2}P_{cr} - P_{cr} \\ &= \frac{1}{2}P_{cr} \text{ W} \end{aligned} \tag{43}$$

This shows that for 100 percent modulation, the modulation power will be half of the carrier power or a third of the total power.

4 Summary

This annexure gave the AM theory which was used in chapter three.

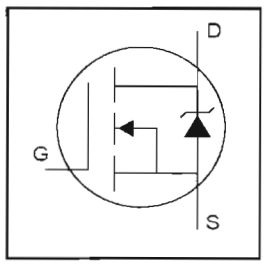
International
IOR Rectifier

PD - 94008

IRFP250N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 200V

$R_{DS(on)}$ = 0.075Ω

I_D = 30A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_{DM}	Pulsed Drain Current ①	120	
P_D @T_C = 25°C	Power Dissipation	214	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	315	mJ
I_{AR}	Avalanche Current①	30	A
E_{AR}	Repetitive Avalanche Energy①	21	mJ
dv/dt	Peak Diode Recovery dv/dt ③	8.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.075	Ω	V_{GS} = 10V, I_D = 18A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	17	—	—	S	V_{DS} = 50V, I_D = 18A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	123	nC	I_D = 18A
Q_{gs}	Gate-to-Source Charge	—	—	21		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	57		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 100V
t_r	Rise Time	—	43	—		I_D = 18A
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		R_G = 3.9Ω
t_f	Fall Time	—	33	—		R_D = 5.5Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2159	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	315	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	83	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	120		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 18A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	186	279	ns	T_J = 25°C, I_F = 18A
Q_{rr}	Reverse Recovery Charge	—	1.3	2.0	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 1.9mH R_G = 25Ω, I_{AS} = 18A. (See Figure 12)

③ I_{SD} ≤ 18A, di/dt ≤ 374A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

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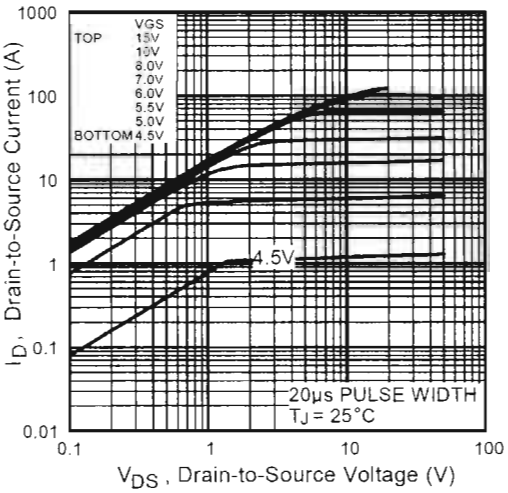

Fig 1. Typical Output Characteristics

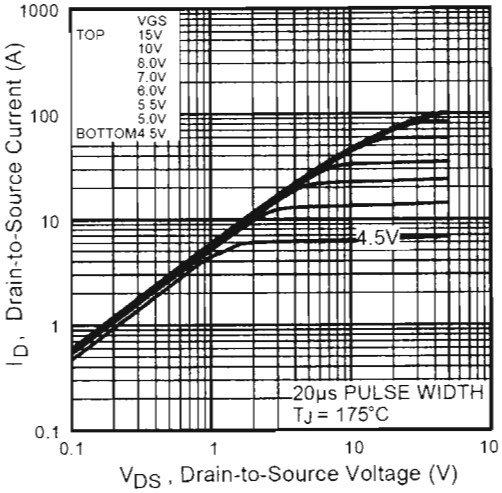

Fig 2. Typical Output Characteristics

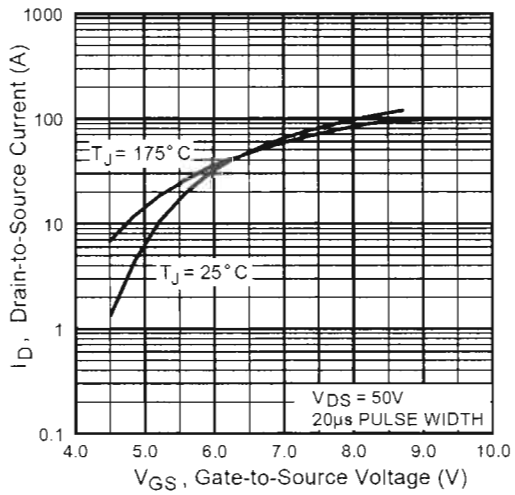

Fig 3. Typical Transfer Characteristics

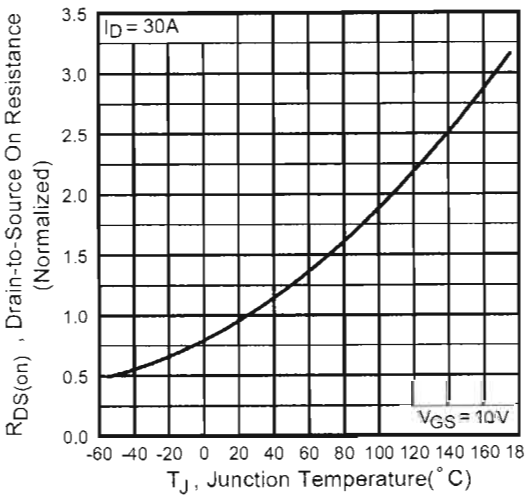

Fig 4. Normalized On-Resistance Vs. Temperature

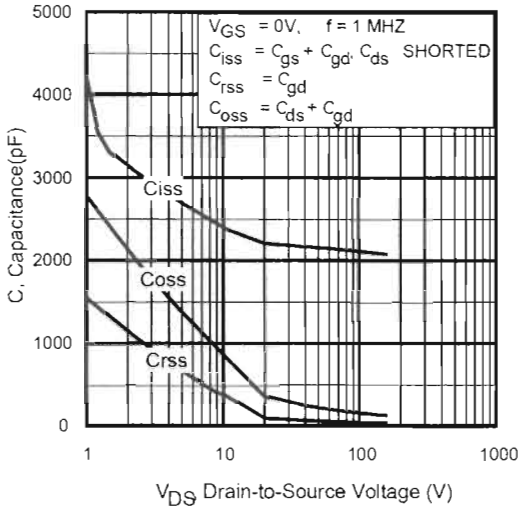

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

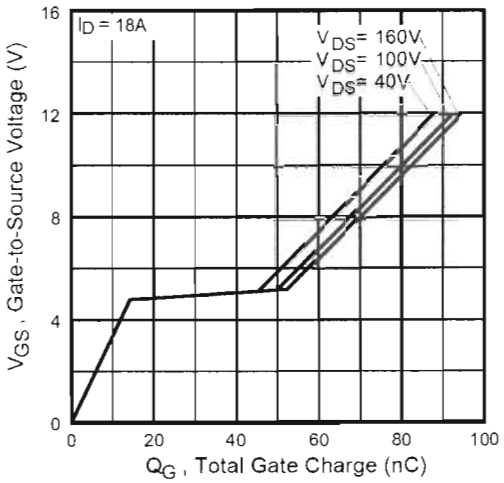

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

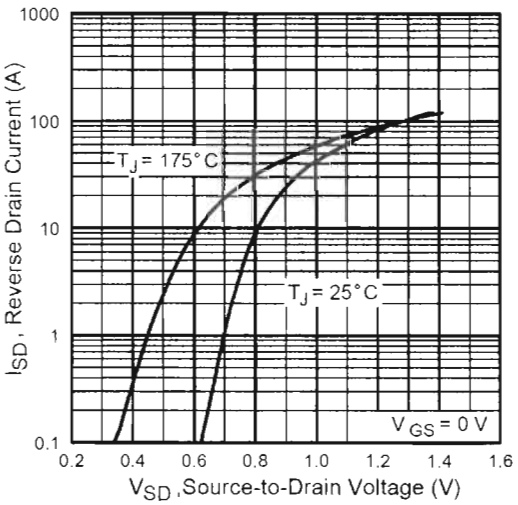

Fig 7. Typical Source-Drain Diode Forward Voltage

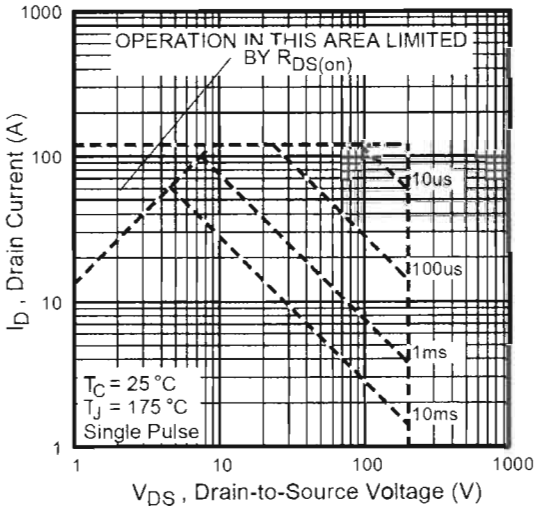

Fig 8. Maximum Safe Operating Area

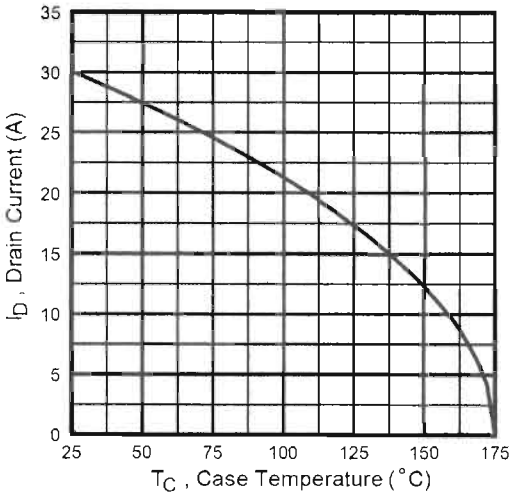

Fig 9. Maximum Drain Current Vs. Case Temperature

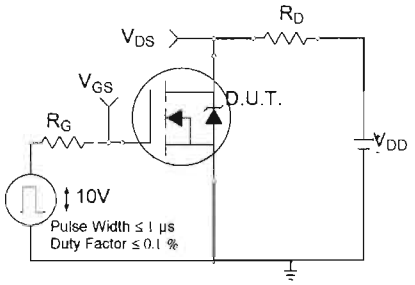

Fig 10a. Switching Time Test Circuit

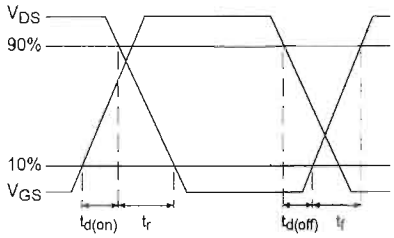

Fig 10b. Switching Time Waveforms

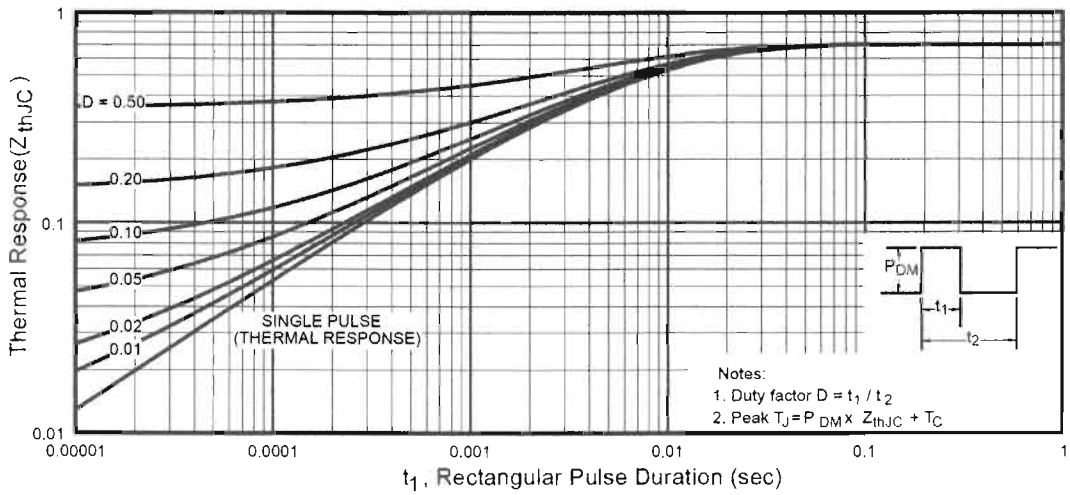

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

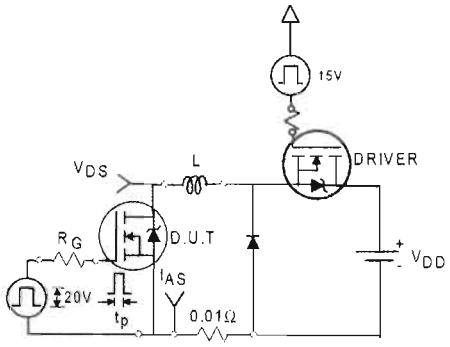

Fig 12a. Unclamped Inductive Test Circuit

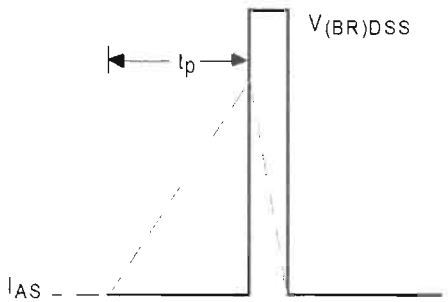

Fig 12b. Unclamped Inductive Waveforms

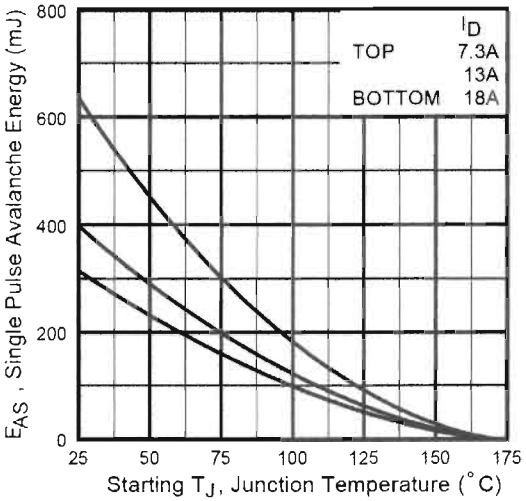

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

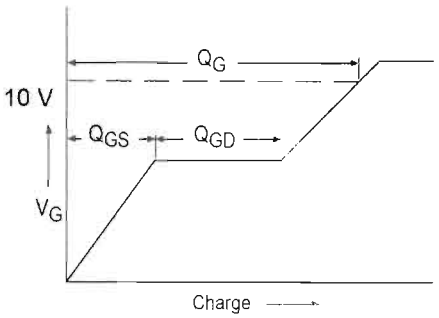

Fig 13a. Basic Gate Charge Waveform

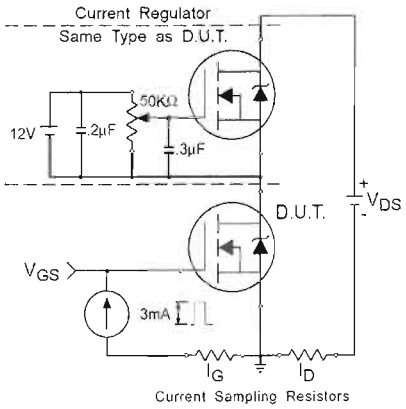

Fig 13b. Gate Charge Test Circuit

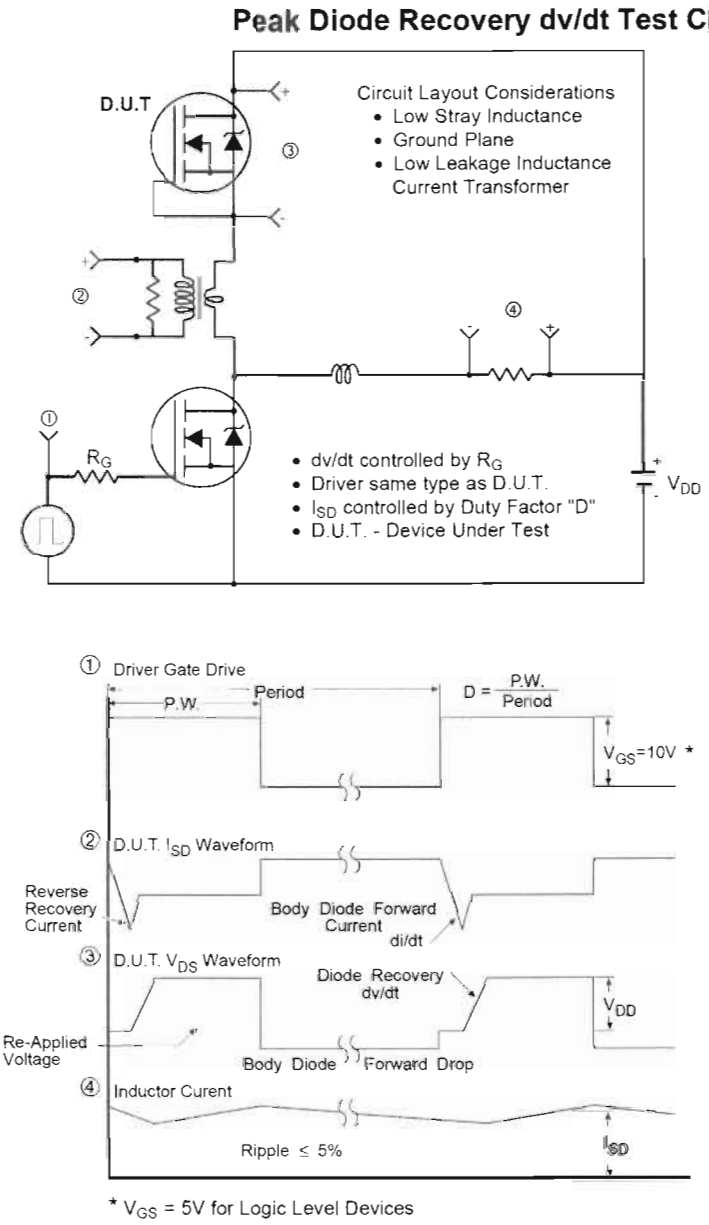

Fig 14. For N-Channel HEXFETS

IRFP250N

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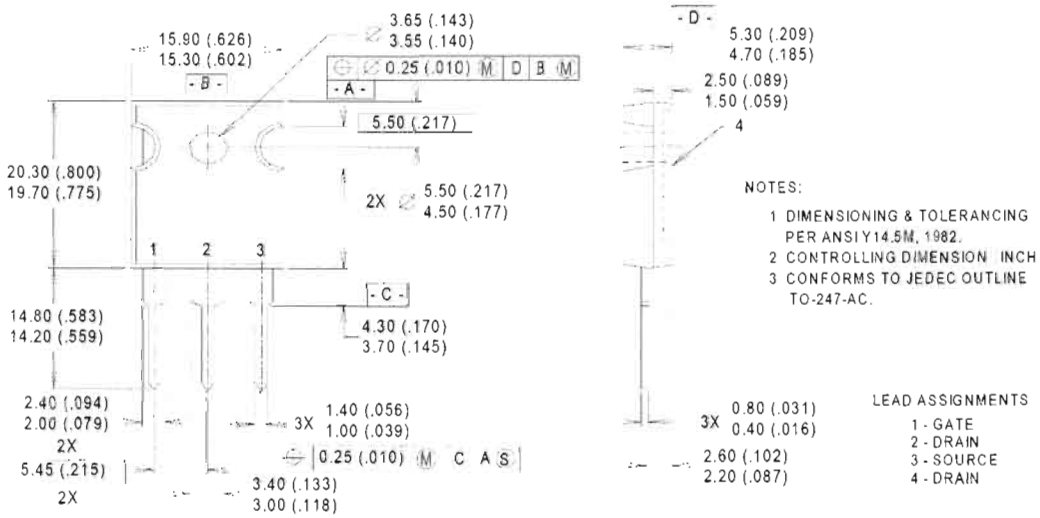
Package Outline

TO-247AC Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: INCH
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

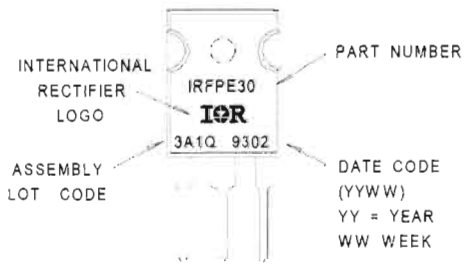
LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

Part Marking Information

TO-247AC

EXAMPLE : THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 3A1Q



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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 10/00

FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised September 2003

CD40106BC
Hex Schmitt Trigger

General Description

The CD40106BC Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{DD} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2$ V_{DD} is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

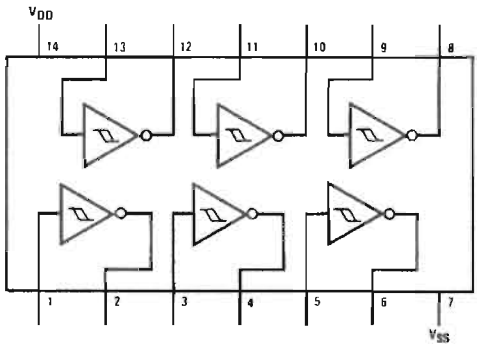
- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.7 V_{DD} (typ.)
- Low power TTL compatibility:
  Fan out of 2 driving 74L or 1 driving 74LS
- Hysteresis: 0.4 V_{DD} (typ.),
  0.2 V_{DD} guaranteed
- Equivalent to MM74C14

Ordering Code:

Order Number	Package Number	Package Description
CD40106BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD40106BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

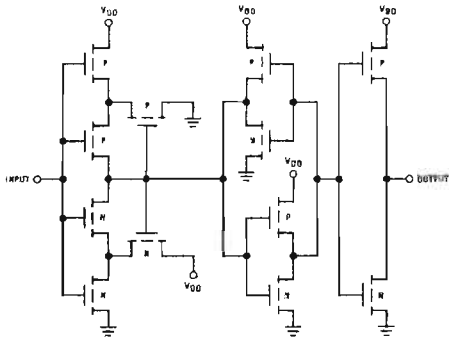
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

Schematic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	
		V_{DD} = 10V		2.0			2.0		60	µA
		V_{DD} = 15V		4.0			4.0		120	
V_{OL}	LOW Level Output	$\|I_O\|$ < 1 µA								
	Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	
		V_{DD} = 15V		0.05			0.05		0.05	
V_{OH}	HIGH Level Output	$\|I_O\|$ < 1 µA								
	Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		0.95		
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_T	Negative-Going Threshold	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	
	Voltage	V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	
V_{T+}	Positive-Going Threshold	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	
	Voltage	V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	
	Voltage	V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	
I_{OL}	LOW Level Output	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		
	Current (Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		
	Current (Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

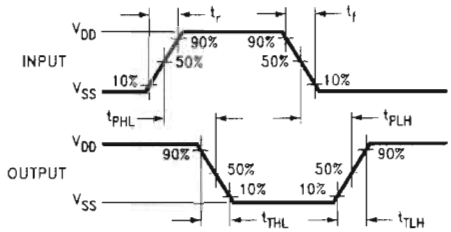
T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	
		V_{DD} = 15V		70	160	
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	
		V_{DD} = 15V		40	80	
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate (Note 5)		14		pF

Note 4: AC Parameters are guaranteed by DC correlated testing

Note 5: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 74C Family Characteristics Application Note, AN-90.

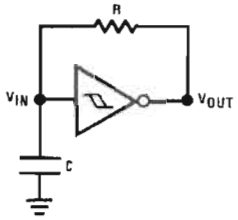
Switching Time Waveforms



$t_r = t_f = 20$ ns

Typical Applications

Low Power Oscillator



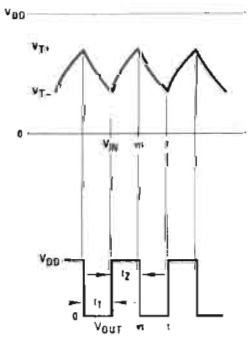
$$t_1 \approx RC\ ln\frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC\ ln\frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

$$f \approx \frac{1}{RC\ ln\frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

Note: The equations assume

$t_1 + t_2 >> t_{PHL} + t_{PLH}$



FEATURES

- High current (max. 1.5 A)
- Low voltage (max. 80 V).

APPLICATIONS

- Driver stages in hi-fi amplifiers and television circuits.

DESCRIPTION

NPN power transistor in a TO-126; SOT32 plastic package. PNP complements: BD136, BD138 and BD140.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector, connected to metal part of mounting surface
3	base

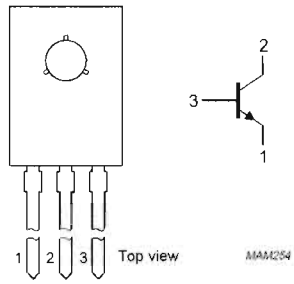


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BD135		–	45	V
	BD137		–	60	V
	BD139		–	100	V
V_{CEO}	collector-emitter voltage	open base			
	BD135		–	45	V
	BD137		–	60	V
	BD139		–	80	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	1.5	A
I_{CM}	peak collector current		–	2	A
I_{BM}	peak base current		–	1	A
P_{tot}	total power dissipation	$T_{mb} \leq 70$ °C	–	8	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base		10	K/W

Note

1. Refer to TO-126; SOT32 standard mounting conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	–	100	nA
		I_E = 0; V_{CB} = 30 V; T_j = 125 °C	–	–	10	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 5 V	–	–	100	nA
h_{FE}	DC current gain	V_{CE} = 2 V; (see Fig.2)				
		I_C = 5 mA	40	–	–	
		I_C = 150 mA	63	–	250	
		I_C = 500 mA	25	–	–	
	DC current gain	I_C = 150 mA; V_{CE} = 2 V;				
	BD135-10; BD137-10; BD139-10	(see Fig.2)	63	–	160	
	BD135-16; BD137-16; BD139-16		100	–	250	
V_{CEsat}	collector-emitter saturation voltage	I_C = 500 mA; I_B = 50 mA	–	–	0.5	V
V_{BE}	base-emitter voltage	I_C = 500 mA; V_{CE} = 2 V	–	–	1	V
f_T	transition frequency	I_C = 50 mA; V_{CE} = 5 V; f = 100 MHz	–	190	–	MHz
$\frac{h_{FE1}}{h_{FE2}}$	DC current gain ratio of the complementary pairs	$\lvert I_C \rvert$ = 150 mA; $\lvert V_{CE} \rvert$ = 2 V	–	1.3	1.6	

PNP power transistors BD136; BD138; BD140

FEATURES

- High current (max. 1.5 A)
- Low voltage (max. 80 V).

APPLICATIONS

- General purpose power applications, e.g. driver stages in hi-fi amplifiers and television circuits.

DESCRIPTION

PNP power transistor in a TO-126; SOT32 plastic package. NPN complements: BD135, BD137 and BD139.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector, connected to metal part of mounting surface
3	base

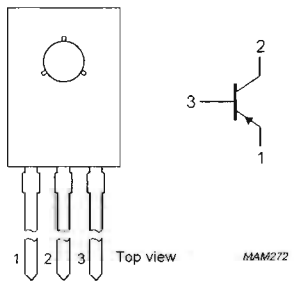


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BD136		–	−45	V
	BD138		–	−60	V
	BD140		–	−100	V
V_{CEO}	collector-emitter voltage	open base			
	BD136		–	−45	V
	BD138		–	−60	V
	BD140		–	−80	V
V_{EBO}	emitter-base voltage	open collector	–	−5	V
I_C	collector current (DC)		–	−1.5	A
I_{CM}	peak collector current		–	−2	A
I_{BM}	peak base current		–	−1	A
P_{tot}	total power dissipation	$T_{mb} \leq 70$ °C	–	8	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base		10	K/W

Note

1. Refer to TO-126 (SOT32) standard mounting conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = –30 V	–	–	–100	nA
		I_E = 0; V_{CB} = –30 V; T_j = 125 °C	–	–	–10	μA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = –5 V	–	–	–100	nA
h_{FE}	DC current gain	V_{CE} = –2 V; (see Fig.2)				
		I_C = –5 mA	40	–	–	
		I_C = –150 mA	63	–	250	
		I_C = –500 mA	25	–	–	
	DC current gain	I_C = –150 mA; V_{CE} = –2 V;				
	BD136-10; BD138-10; BD140-10	(see Fig.2)	63	–	160	
	BD136-16; BD138-16; BD140-16		100	–	250	
V_{CEsat}	collector-emitter saturation voltage	I_C = –500 mA; I_B = –50 mA	–	–	–0.5	V
V_{BE}	base-emitter voltage	I_C = –500 mA; V_{CE} = –2 V	–	–	–1	V
f_T	transition frequency	I_C = –50 mA; V_{CE} = –5 V; f = 100 MHz	–	160	–	MHz
$\frac{h_{FE1}}{h_{FE2}}$	DC current gain ratio of the complementary pairs	$\lvert I_C \rvert$ = 150 mA; $\lvert V_{CE} \rvert$ = 2 V	–	1.3	1.6	

International
IOR Rectifier

Data Sheet No. PD60017 Rev.Q

IR2125(S) & (PbF)

CURRENT LIMITING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input
- 2.5V, 5V and 15V input logic compatible
- Also available LEAD-Free

Product Summary

V_{OFFSET}	500V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSth}	230 mV
$t_{on/off}$ (typ.)	150 & 150 ns

Packages

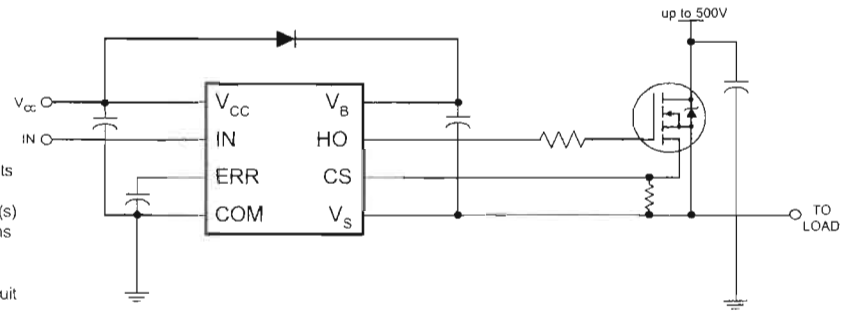
8-Lead PDIP

16-Lead SOIC
(Wide Body)

Description

The IR2125(S) is a high voltage, high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 2.5V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle by cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting conditions and latched shutdown. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 500 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	525	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{ERR}	Error Signal Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 lead PDIP)	—	1.0	W
	(16 lead SOIC)	—	1.25	
Rth_{JA}	Thermal Resistance, Junction to Ambient (8 lead PDIP)	—	125	°C/W
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	V_S + 12	V_S + 18	V
V_S	High Side Floating Offset Voltage	Note 1	500	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	0	18	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{ERR}	Error Signal Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_B	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +500V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 3300 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figures 3 through 6.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	170	240	ns	V_{IN} = 0 & 5V V_S = 0 to 600V
t_{off}	Turn-Off Propagation Delay	8	—	200	270		
t_{sd}	ERR Shutdown Propagation Delay	9	—	1.7	2.2	µs	
t_r	Turn-On Rise Time	10	—	43	60	ns	
t_f	Turn-Off Fall Time	11	—	26	35		
t_{cs}	CS Shutdown Propagation Delay	12	—	0.7	1.2	µs	
t_{err}	CS to ERR Pull-Up Propagation Delay	13	—	9.0	12		C_{ERR} = 270 pF

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	14	2.2	—	—	V	
V_{IL}	Logic "0" Input Voltage	15	—	—	0.8		
V_{CSTH+}	CS Input Positive Going Threshold	16	150	230	320	mV	
V_{CSTH-}	CS Input Negative Going Threshold	17	130	210	300		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	18	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	19	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	20	—	—	50	µA	V_B = V_S = 500V
I_{QBS}	Quiescent V_{BS} Supply Current	21	—	400	1000		V_{IN} = V_{CS} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	22	—	700	1200		V_{IN} = V_{CS} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current	23	—	4.5	10		V_{IN} = 5V
I_{IN-}	Logic "0" Input Bias Current	24	—	—	1.0		V_{IN} = 0V
I_{CS+}	"High" CS Bias Current	25	—	4.5	10		V_{CS} = 3V
I_{CS-}	"Low" CS Bias Current	26	—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	27	8.5	9.2	10.0	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	28	7.7	8.3	9.0		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	29	8.3	8.9	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	30	7.3	8.0	8.7		
I_{ERR}	ERR Timing Charge Current	31	65	100	130	µA	V_{IN} = 5V, V_{CS} = 3V ERR < V_{ERR+}
I_{ERR+}	ERR Pull-Up Current	32	8.0	15	—	mA	V_{IN} = 5V, V_{CS} = 3V ERR > V_{ERR+}
I_{ERR-}	ERR Pull-Down Current	33	16	30	—		V_{IN} = 0V
I_{O+}	Output High Short Circuit Pulsed Current	34	1.0	1.6	—	A	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	35	2.0	3.3	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

IR2125(S) & (PbF)

International
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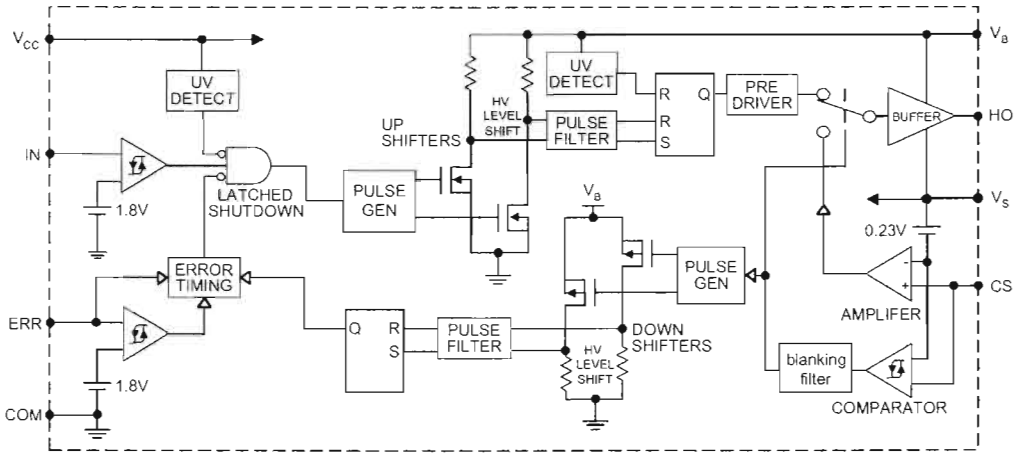
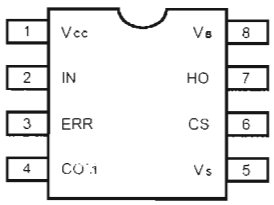
Functional Block Diagram



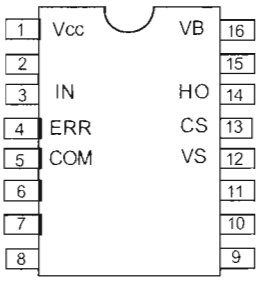
Lead Definitions

Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO
ERR	Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead PDIP



16 Lead SOIC (Wide Body)

IR2125	Part Number	IR2125S

MC34151, MC33151

High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual−in−line and surface mount packages.

Features

- Pb−Free Packages are Available
- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

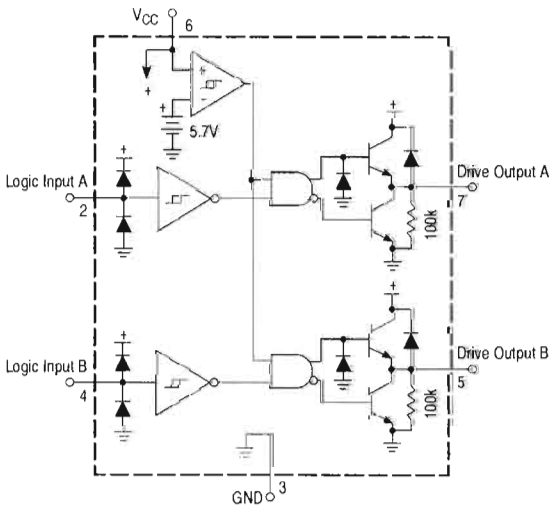


Figure 1. Representative Block Diagram

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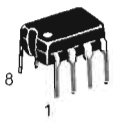
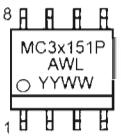
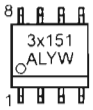
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

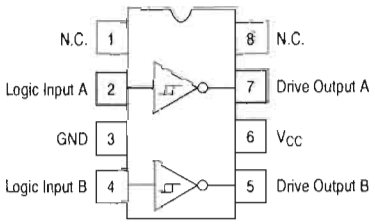


SOIC−8
D SUFFIX
CASE 751



x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

July, 2004 − Rev. 4

Publication Order Number:
MC34151/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	−0.3 to V_{CC}	V
Drive Outputs (Note 2)			A
Totem Pole Sink or Source Current	I_O	1.5	
Diode Clamp Current (Drive Output to V_{CC})	$I_{O(clamp)}$	1.0	
Power Dissipation and Thermal Characteristics			
D Suffix SOIC−8 Package Case 751			
Maximum Power Dissipation @ T_A = 50°C	P_D	0.56	W
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	180	°C/W
P Suffix 8−Pin Package Case 626			
Maximum Power Dissipation @ T_A = 50°C	P_D	1.0	W
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34151		0 to +70	
MC33151		−40 to +85	
MC33151V		−40 to +125	
Storage Temperature Range	T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage − Output Transition High to Low State	V_{IH}	−	1.75	2.6	V
Output Transition Low to High State	V_{IL}	0.8	1.58	−	
Input Current − High State (V_{IH} = 2.6 V)	I_{IH}	−	200	500	μA
− Low State (V_{IL} = 0.8 V)	I_{IL}	−	20	100	
DRIVE OUTPUT					
Output Voltage − Low State (I_{Sink} = 10 mA)	V_{OL}	−	0.8	1.2	V
(I_{Sink} = 50 mA)		−	1.1	1.5	
(I_{Sink} = 400 mA)		−	1.7	2.5	
− High State (I_{Source} = 10 mA)	V_{OH}	10.5	11.2	−	
(I_{Source} = 50 mA)		10.4	11.1	−	
(I_{Source} = 400 mA)		9.5	10.9	−	
Output Pulldown Resistor	R_{PD}	−	100	−	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	−	35	100	
Logic Input to Drive Output Fall	$t_{PHL(in/out)}$	−	36	100	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	−	14	30	ns
C_L = 2.5 nF		−	31	−	
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	−	16	30	ns
C_L = 2.5 nF		−	32	−	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		−	6.0	10	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)		−	10.5	15	
Operating Voltage	V_{CC}	6.5	−	18	V

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151 T_{high} = +70°C for MC34151
   −40°C for MC33151 +85°C for MC33151