# TECHNOLOGY DEVELOPMENT OF A MAXIMUM POWER POINT TRACKER FOR REGENERATIVE FUEL CELLS

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# **Declaration**

I, Neil Jansen van Rensburg, hereby declare that the following research information is solely my own work. This is submitted in fulfilment of the requirements for the Magister Technologiae: Engineering: Electrical to the Department of Electronic Engineering at the Vaal University of Technology, Vanderbijlpark. It has not been submitted previously for any assessment to any educational institution.

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#### **Dedication**

This dissertation is dedicated to my parents, Ronnie and Thea, my sisters, Elaine and Nicolene, as well as their spouses, my friends, and lastly, the love of my life, Tanya Nortje, for all their support and continuing encouragement throughout the study of this project.

Success is the ability to go from failure to failure without losing your enthusiasm.

- Sir Winston Churchill

#### **Abstract**

Global warming is of increasing concern due to several greenhouse gases. The combustion of fossil fuels is the major contributor to the greenhouse effect. To minimalise this effect, alternative energy sources have to be considered. Alternative energy sources should not only be environmentally friendly, but also renewable and/or sustainable. Two such alternative energy sources are hydrogen and solar energy.

The regenerative fuel cell, commonly known as a hydrogen generator, is used to produce hydrogen. The current solar/hydrogen system at the Vaal University of Technology's Telkom Centre of Excellence makes use of PV array to supply power to an inverter and the inverter is connected to the hydrogen generator. The inverter provides the hydrogen generator with 220VAC. The hydrogen generator has its own power supply unit to convert the AC power back to DC power. This reduces the efficiency of the system because there will be power loss when converting DC power to AC power and back to DC power. The hydrogen generator, however, could be powered directly from a PV array. However, the hydrogen generator needs specific input parameters in order to operate. Three different input voltages with their own current rating are required by the hydrogen generator to operate properly. Thus, a DC-DC power supply unit needs to be designed to be able to output these parameters to the hydrogen generator. It is also important to note that current PV panel efficiency is very low; therefore, the DC-DC power supply unit also needs to extract the maximum available power from the PV array. In order for the DC-DC power supply unit to be able to extract this maximum power, a maximum power point tracking algorithm needs to be implemented into the design. The DC-DC power supply is designed as a switch mode power supply unit. The reason for this is that the efficiency of a switch mode power supply is higher than that of a linear power supply.

To reach the objective the following methodology was followed. The first part of the research provided an introduction to PV energy, charge controllers and hydrogen generators. The problem statement is included as well as the purpose of this research

and how this research was to be carried out. The second part is the literature review. This includes the background study of algorithms implemented in MPPT's; it also explains in detail how to design the MPPT DC-DC SMPS. The third part was divided into two sections. The first section is the design, programming and manufacturing of the MPPT DC-DC SMPS. The second section is the simulation of the system as a whole which is the simulation of the PV array connected to the MPPT DC-DC SMPS and the hydrogen generator. The fourth part in the research compared the results obtained in the simulation and practical setup. The last part of the research provided a conclusion along with recommendation made for further research.

The simulation results showed that the system works with an efficiency of 40,84%. This is lower than expected but the design can be optimised to increase efficiency. The practical results showed the efficiency to be 38%. The reason for the lower efficiency is the simulation used ideal components and parameters, whereas the practical design has power losses due to the components not being ideal.

The design of the DC-DC switch mode power supply, however, indicated that the hydrogen generator could be powered from a PV array without using an inverter, with great success.

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# Glossary of abbreviations

A.	IC – Integrated circuit
<u>A</u>	-
A - Amp	Irr - Irradiance
AC – Alternating current	<u>K</u>
ADC – Analog to digital converter	kW – Kilowatt
<u>C</u>	<u>L</u>
CIGS – Copper indium gallium selenide	LED – Light emitting diode
CMC – Current-mode control	<u>M</u>
CNC - Computer numerical control	MCU – Microcontroller unit
CCM - Continuous conduction mode	Mosfet – Metal-oxide semiconductor
<u>D</u>	field-effect transistor
DC – Direct current	MPLab – Microchip PICmicro Laboratory
DC-DC - Direct current to direct current	MPP – Maximum power point
DCM – Discontinuous conduction mode	MPPT – Maximum power point tracker
D – Duty cycle	<u>N</u>
<u>E</u>	N/A – Not available
ESC – Extremum seeking control	<u>o</u>
EHP – electron-hole pair	$O_2$ – Oxygen
eV – electron Volt	<u>P</u>
eff - Efficiency	P – Power
<u>F</u>	$P_{\rm PV}$ – Power of photovoltaic panel
$f_{\rm SW}$ – Switching frequency	PCB – Printed circuit board
FC – Fuel cell	PEM – Proton Exchange Membrane
<u>H</u>	PIC – Peripheral interface controller
H <sub>2</sub> – Hydrogen gas molecule	PID – Proportional-Integral-Derivative
$H_2O$ – Water	P&O – Perturb and Observe
HG – Hydrogen generator	PV – photovoltaic
Hz – Hertz	P-N – p-type and n-type
Ī	P-V – Power versus voltage
$I_{\mathrm{MPP}}$ – Current at maximum power	PWM – Pulse-width modulation
$I_{\rm SC}$ – Short circuit current	<u>R</u>
$I_{PV}$ – Current of photovoltaic panel	RFC – Regenerative fuel cell
I-V – Current versus voltage	<u>s</u>
ICD – In-circuit debugger	SinESC – Sinusoidal ESC

SMESC – Sliding mode ESC

SMPS – Switch-mode power supply

STC – Standard test conditions

# <u>T</u>

TCD – Thermal conductivity detector

## $\underline{\mathbf{U}}$

URFC – Unitized regenerative fuel cell

μH – micro-Henry

μF – micro-Farad

# $\underline{\mathbf{V}}$

V-Voltage

VAC – Volts alternating current

VCM – Voltage-mode control

VUT – Vaal University of Technology

 $V_{\rm OC}$  – Open circuit voltage

 $V_{\mathrm{MPP}}$  – Voltage at maximum power

 $V_{PV}$  – Voltage of photovoltaic panel

# $\mathbf{W}$

W-Watt

#### CHAPTER 1 INTRODUCTION AND OVERVIEW

# 1.1 Global warming and solar energy

Global warming (greenhouse effect) is becoming an ever-increasing concern for humanity. According to \$en (2008), there are several greenhouse gases that contribute to the global warming effects in the atmosphere and they are almost entirely due to human activities. Fossil fuel combustion is one of the contributing factors to the greenhouse effect, along with acid rain, air pollution, climate changes and oil spills (\$en, 2008). Thus, it is logical that research in alternative energy sources, which are not only environmentally friendly, but also renewable and/or sustainable, are of primary concern. Farret and Simões (2006) state that there are several renewable energy sources that have been used for thousands of years, one of which is solar energy.

The radiation from the sun, that is capable of producing heat, causing chemical reactions or generating electrical energy, is called solar energy (Ashok, 2012). According to \$\\$en (2008), solar radiation is the world's most abundant and permanent energy source. Lynn (2010) states that the sun provides, in about an hour, the present energy requirements of earth's entire population for a whole year. It can be seen clearly that solar energy is an important renewable and sustainable alternative energy source. But, how will all that energy be harnessed? There are two ways to produce electricity from solar energy: solar thermal and photovoltaic (PV) systems. The method that is of an increasing interest in electrical power applications, according to Kwon *et al.* (2006), is PV energy. The reason for this increase in interest is that it is clean, free, abundant, pollution-free and inexhaustible. The rapid growth in solar cells and power electronics technology also contributes to an increase in PV energy (Kwon *et al.*, 2006).

#### 1.2 Photovoltaic energy

The European Commission (2009) defines PV as the field of technology and research related to devices, which convert sunlight (solar radiation) directly into electrical energy. PV cells, which are made of semiconductor materials, such as silicon, are the basic building blocks of PV technology (European Commission, 2009). The PV cell,

which is a semiconductor P-N junction device, converts sunlight into electrical energy due to the PV effect shown in Figure 1. The PV effect was discovered in 1839 by Edmund Becquerel, a French scientist (Solanki, 2009). Sunlight contains photons, and these photons contain various amounts of energies depending on different light situations. Photons can either be reflected, absorbed or they can pass through when they strike the PV cell. For the PV effect to take place, there are three basic requirements, namely (1) absorption of photons through the creation of electron-hole pairs (EHPs); (2) separation of the these EHPs from each other across the P-N junction, resulting in the generation of a potential difference in the PV cell; (3) transfer of these separated electrons and holes through electrical terminals to an external circuit in the form of electrical current, and thus, power can be extracted from the PV cell (Mitchell and Tatro, 2008; Solanki, 2009; de Neufville, 2012).

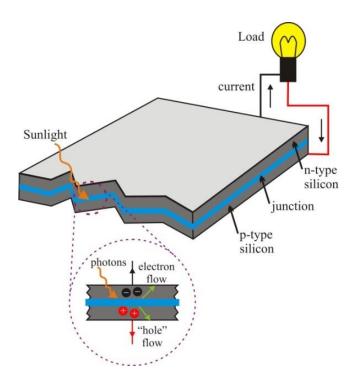


Figure 1 PV effect

Fraas and Partain (2010) state that the main characteristic of a PV cell is the conversion efficiency of solar energy into electrical energy. Unfortunately, several causes place limitations on the PV cell efficiency. One of the limitations is based on the properties of the silicon semiconductors used in PV cells. Photons, having energy less than 1.12 eV, do not get absorbed in the material due to the band gap of the cell,

and photons with energies more than 1.12 eV lose their energy in the form of heat dissipation. Other losses include: optical losses, recombination losses and resistive losses (Fraas and Partain, 2010). It can be observed that due to all these losses the efficiency is greatly reduced. For example, according to Fraas and Partain (2010) the theoretical efficiency of a crystalline silicon PV cell is about 29%, the world record is 24.3% but average efficiencies for typical industrial PV cells are only in the range of 16% to 17%.

Solanki (2009) explains that solar PV modules/panels are numerous individual PV cells collectively connected to each other in a series and/or parallel grid. Lynn (2010) then describes a PV array as a group of interconnected modules working together in a PV installation. PV systems can either be grid-tied or stand-alone, according to Lynn (2010). When PV systems are used for stand-alone applications, a battery (or any DC storage component) is normally connected to the system as a back-up source to supply the load during the night or overcast days when the PV array is not operational (Solanki, 2009). Solanki (2009) explains that where batteries are used, it is important to prevent over-charging or deep discharging to prolong battery life. This is achieved by using charge controllers.

#### 1.3 Charge controllers and maximum power point trackers

IEEE-SA (2003) defines a charge controller as an electrical control device that regulates battery charging by voltage control and/or other means. It may also incorporate one or more of the following functions: discharge termination, regulation voltage temperature compensation, load control and status indication. According to Solanki (2009) there are three types of charge controllers: series controllers, shunt controllers and maximum power point trackers (MPPTs).

The first two charge controllers mentioned deliver all the power from the PV array into the battery, with low efficiency. It can be concluded that because of the low efficiency of PV cells every bit of output power is important. Solanki (2009) explains that for the charging to be more efficient, the PV array has to be operated at a point where the PV array output power is maximum, in other words at the maximum power point (MPP). Figure 2 shows a typical PV array characteristic curve.

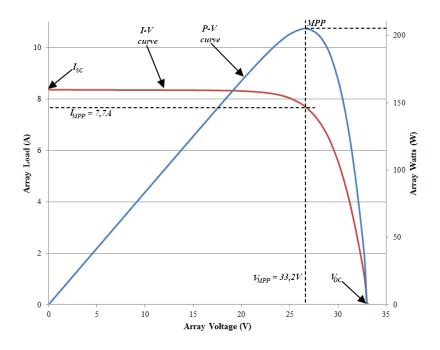


Figure 2 PV array characteristic curve

This is where the MPPT fits in. E-Power (2008) explains that MPP tracking is a technique used in charge controllers to extract the maximum available power (the point on a PV module's I-V curve, where the product of the voltage and the current is a maximum) from the panels, as the maximum power changes according to variations in ambient temperature, solar cell temperature and solar radiation. The MPPT measures the output of the PV panels, comparing it to a battery's voltage and then setting the highest power that the PV panels can deliver to charge the battery. It then converts the power to the optimum voltage to transfer maximum current into the battery.

Currently, there are different kinds of MPP tracking algorithms used in PV systems. Esram and Chapman (2007) explain that all the methods vary in their complexity, sensors required, convergence speed, cost, effectiveness, implementation hardware, popularity and in other aspects. They also range from simplistic to complex; from ineffective to effective but simplicity does not necessarily mean ineffective. Xiao *et al.* (2011) mention a comparison study that was presented by Jain and Agarwal (2007) and Esram and Chapman (2007), which illustrated MPP tracking methods developed before 2006. Some of these techniques are heuristic search (hill climbing, perturb and observe); extreme value searching (incremental conductance); linear

approximation methods (fractional  $V_{\rm OC}$  or fractional  $I_{\rm SC}$ ); intelligent control (fuzzy logic, neural network); linear control techniques (dV/dV or dP/dI feedback control) and a few other methods. All these methods have their own advantages, disadvantages, effectiveness and reliability.

Xiao *et al.* (2011) classifies the latest MPP tracking algorithm developments since 2006 in the following categories: (1) Real-time identification method, (2) Extremum seeking control, (3) Particle swarm optimisation, (4) DIRECT (DIviding RECTangles) search algorithm, and (5) Adaptive step-size method. The importance of MPPT originates from the fact that it adjusts the power interfaces to achieve the greatest possible power from a PV array during moment to moment variations of light level, shading, temperature and PV module characteristics (Xiao *et al.*, 2011). Xiao *et al.* (2011) states, "MPPT has become an essential component to evaluate the design performance of PV power systems".

Instead of storing the solar energy in batteries, the energy could be converted to hydrogen. The stored hydrogen could be manufactured with a regenerative fuel cell.

#### 1.4 Regenerative fuel cells

A regenerative fuel cell (RFC) is a device that produces hydrogen (H<sub>2</sub>). The RFC, which can also be referred to as a hydrogen generator (HG), is a fuel cell (FC) operating in the reverse mode. A FC, which operates in the forward mode, uses hydrogen (H<sub>2</sub>) and oxygen (O<sub>2</sub>) to produce electrical energy and water (H<sub>2</sub>O) (Li *et al.*, 2010). In contrast, a RFC uses electrical energy and water to produce H<sub>2</sub> and O<sub>2</sub>. A dedicated RFC should not be confused with a unitised RFC (URFC). The RFC works only in the reverse mode (electrolyser), whereas the URFC operates in both reverse and forward modes (Grigoriev *et al.*, 2011; Van Tonder, 2011).

The HG that is focused on in this research is the HOGEN® GC 300, which utilises a four cell proton exchange membrane (PEM) RFC stack to produce H<sub>2</sub>, see Figure 3. The reason for the choice of this specific HG is that it is currently in use at the Vaal University of Technology (VUT), Electronics Department, for their research in a solar-hydrogen fuel cell plant.



Figure 3 HOGEN® GC 300

The HOGEN® GC 300 incorporates a power supply of 110-220 VAC, single phase and a frequency of 50 or 60 Hz to operate (see Annexure B). The HOGEN® GC 300 uses a switch-mode power supply (SMPS) to supply DC voltage to the electronic components on the printed circuit board (PCB). Figure 4 shows the power supply section of the HOGEN® GC 300.

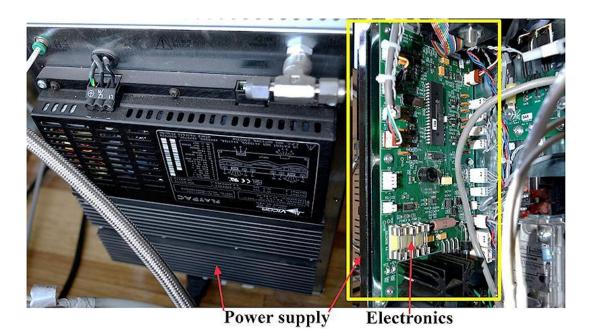


Figure 4 HOGEN® GC 300 power supply and electronics

The output voltages of the power supply are indicated in Table 1.

Table 1 HOGEN® GC 300 power supply output voltages

Output	Voltage (V)	Power (P)		
Output 1	7,5	20	150	
Output 2	12	4,2	50	
Output 3	5	10	50	

The output voltages of the PSU supply specific sections of the HOGEN® GC 300, they are as follows:

- Output 1: Fuel cell stack
- Output 2: Water circulatory pump
- Output 3: Microcontroller unit (MCU) and the rest of the electronic components and circuitry.

Figure 5 shows the block diagram of the unmodified HOGEN® GC 300.

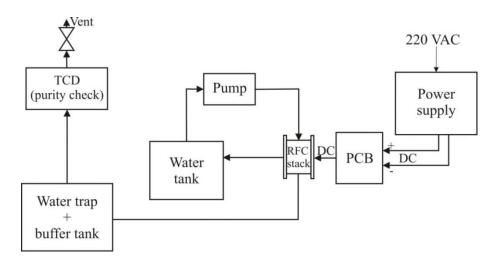


Figure 5 HOGEN® GC 300 block diagram

The work done in this project will bypass the need for a 220 VAC power supply by directly powering the PCB in the HG, with DC voltage from a PV panel, through the MPPT.

Commercially available HGs, as in the case with the HOGEN® GC 300, are dependent on an input voltage of 220 VAC, although in essence it only requires DC voltage to operate. The reason for this is that 220 VAC is fed to the power supply,

which converts the AC to a number of DC output voltages as indicated in Table 1, which are 7.5 V, 12 V and 5 V.

#### 1.5 Problem statement

To power a regenerative hydrogen generator from a PV array is a problem because the available HGs make use of 220 VAC. To address the problem of sustainable and alternative energy, there is a need to develop technology to power HGs directly from PV panels, via a MPPT. Commercially available MPPTs are not designed for a wide range of electrical loads and are particularly not designed for HGs. Such MPPTs for HGs do not exist, yet it is a crucial link in the sustainable alternative energy chain.

# 1.6 Focus and purpose

The focus and purpose of the research will be on the design and development of a MPPT, as indicated in Figure 6. As can be seen, the research forms part of a sustainable alternative solar energy system. The research will significantly improve the sustainability and efficiency of the integrated alternative energy system at VUT and will largely contribute towards the commercialisation of the system.

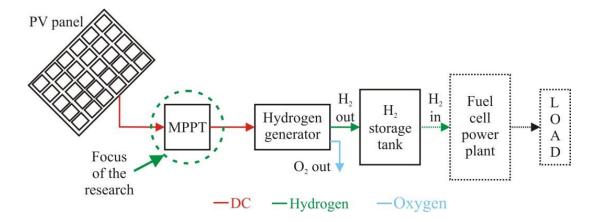


Figure 6 VUT Sustainable/Alternative Energy System

In the proposed system for this research the MPPT will replace the HG power supply (see Figure 7), thus making the HG independent from grid power as illustrated in Figure 6. The hybrid system will consist of a PV array, MPPT, HG and a hydrogen storage tank and the FC power plant. The MPPT will deliver optimum power to the HG to increase its efficiency.

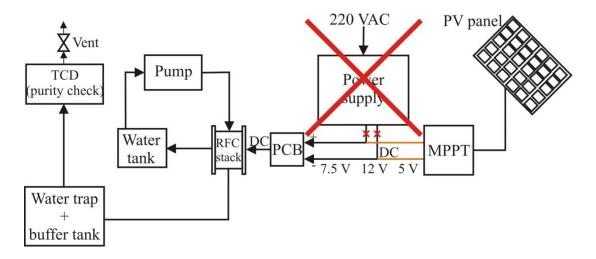


Figure 7 HOGEN GC 300 block diagram with new power supply

# 1.7 Objective

To design and develop dedicated MPPT technology, in order to connect PV panels directly to the HG.

#### 1.7.1 Specific objectives

- 1.7.1.1 Gathering of electrical data and information plus analysis of the data
  - Gathering electrical data on RFCs
  - Evaluating data obtained on RFCs
  - Choosing the most suitable MPPT algorithm for this application.
- 1.7.1.2 Development of the MPPT
  - Mathematical modelling of the chosen MPPT
  - Designing of the MPPT and programming of the algorithm
  - Running design simulations
  - Evaluating simulation results.
- 1.7.1.3 Fabrication and testing of the MPPT
  - Fabricating the MPPT
  - Testing the MPPT in the laboratory and in real time
  - Evaluating the results and comparing results with the simulated results.
- 1.7.1.4 Implementation in the VUT hybrid system and testing the system over a period of time
- 1.7.1.5 Documentation and thesis writing.

#### 1.8 Research methodology

The strategy that was followed in the research study:

- 1.8.1 Gathering of electrical data and information plus analysis of the data
  - Taking electrical measurements to determine the electrical requirements of a HG
  - These data are an important design parameter of the MPPT.
  - A MPPT algorithm was chosen according to data obtained on the RFC as well as on other criteria.

#### 1.8.2 Development of the MPPT

- Simulations on the design was done using Mathworks Matlab (Mathematical software) and Mathworks Simulink (Simuliink is a logic circuit simulation software)
- Altium Designer (schematic and PCB design software) was used to design the circuit.
- Programming the algorithm on a PIC microcontroller was done using Microchip MPlabX (microcontroller programming software).
- Efficiency was evaluated and adjustments to the circuit design were done.

# 1.8.3 Fabrication and testing of the MPPT

- A CNC machine (Computer Numerical Control) was used to fabricate the PCB (printed circuit board)
- The algorithm was loaded onto the microcontroller using the Microchip ICD3 (In-circuit debugger and programmer)
- Outdoor testing was done using a PV panel to test the MPPT under real world conditions.
- Efficiency was evaluated and adjustments to the circuit design will be done.
- 1.8.4 Implementation in the VUT hybrid system and testing of the system over a period of time in order to evaluate overall system efficiency and performance

# 1.8.5 Documentation and thesis writing.

# 1.9 Summary

This chapter explained the impact of global warming and the need for alternative energy sources. An overview of PV energy was also given and how to extract maximum power from PV panels to deliver optimum power to the HG. The purpose of the study along with the problem statement was given. Lastly, an overview was given to indicate the outline of the research.

Chapter 2 describes theoretical background study on the MPPT algorithms and DC-DC SMPS.

#### CHAPTER 2 MAXIMUM POWER POINT TRACKERS

#### Introduction

In order to power a HG from a PV array a summary of PV panel characteristics are given. PV panel manufacturers make use of different technologies and materials to produce PV panels, which gives each panel a unique characteristic (El Chaar *et al.*, 2011). Two of the more popular technologies are crystalline and thin-film. Some of the materials used for the crystalline technology are mono-crystalline and polycrystalline and for thin-film technology, the materials are amorphous silicon and cadmium telluride. Table 2 shows the technologies, materials and characteristics from different manufacturers for their PV panels. See Annexure A for the PV panel datasheets. As seen from Table 2 each PV panel has different characteristics that have to be taken into account when designing an efficient MPPT.

Table 2 PV panel characteristics

	Cell	type	Characteristics					
Manufacturer	Crystalline	Thin-film	Power	Effeciency	$V_{ m MPP}$	$I_{\mathrm{MPP}}$	$V_{ m oc}$	$I_{ m SC}$
			<b>(P)</b>	(%)	<b>(V)</b>	(A)	(V)	(A)
Solyndra		CIGS	150	N/A	65,70	2,28	91,40	2,72
CanadianSolar	Poly		235	14,61	29,80	7,90	36,90	8,46
Sharp	Poly		235	14,40	29,20	8,05	37,40	8,59
Sungen		Amorphous	95	N/A	70,00	1,35	90,00	1,67
Sungen			195	15,30	38,60	5,05	46,10	5,56

- $V_{\text{MPP}} \equiv \text{Voltage at maximum power point}$
- $I_{\text{MPP}} \equiv \text{Current at maximum power point}$
- $V_{\rm OC}$  = Open-circuit voltage
- $I_{SC} \equiv Short-circuit current$

#### 2.1 MPPT classification

Salas *et al.* (2006) explains that MPPT algorithms can be classified as either direct (not PV panel characteristic dependent) or indirect (PV panel characteristic dependent) methods. Indirect methods take measurements such as short-circuit current, open-circuit voltage and irradiance, which are indirect occurrences from the operating voltage and current, to approximate the optimum voltage from an exact

model of the PV panel used, and according to Hohm and Ropp (2003) they are also called model-based MPPT algorithms.

On the other hand, direct methods do not require an exact model of a PV panel to operate effectively. Direct methods search for the optimum point from the operating voltage and current measurements and their time-derivatives (Leyva *et al.*, 2011).

Table 3 is adapted from various studies of MPPTs done by Esram and Chapman (2007), Hohm and Ropp (2003), Onat (2010c) and Leyva *et al.* (2011).

Table 3 Direct and indirect MPPT algorithms

МРРТ	Direct/ Indirect	True MPPT	Analog/ Digital	Periodic tuning	Track speed	Sensed parameter	Efficiency (%)
Perturb & observe	Direct	Yes	Both	No	Varies	Voltage, Current	81,5 - 85
Constant voltage/current	Indirect	No	Analog	Yes	Medium	Voltage/ Current	73 - 85
Hill climbing	Direct	Yes	Both	No	Varies	Voltage, Current	81,5 - 85
Fractional V <sub>OC</sub>	Indirect	No	Both	Yes	Medium	Voltage	N/A
Artificial intelligence	Indirect	Yes	Both	No	Fast	Varies	>95
Incremental conductance	Direct	Yes	Digital	No	Varies	Voltage, Current	73 - 85

# Category descriptions:

- **MPPT:** Type of MPPT algorithm.
- **Direct:** Not PV panel characteristic dependent and **Indirect:** PV panel characteristic dependent.
- **True MPPT:** Tracks the MPP accurately or uses approximations.
- Analog/Digital: Uses only analog/digital components or both in the circuit.
- **Periodic tuning:** The circuit parameters need to be calibrated often in order to track the MPP.
- **Track speed:** Tracking speed of the MPP.
- **Sensed parameters:** What type of sensor the algorithm needs in order to track the MPP.
- **Efficiency:** Algorithm efficiency for tracking the MPP.

Before a MPPT algorithm is selected there are a few criteria that need to be considered beforehand in order to make the correct choice of algorithm for a specific application. Summarised below is the main criteria when considering a MPPT algorithm (Onat, 2010a):

- Ease of implementation. Methods can be either analog, digital or both. Digital MPPT algorithms may require software and programming of a MCU.
- Required number of sensors. Sensors are either current, voltage or both.
   Voltage sensing is easier and more reliable than current sensors. Current can be cumbersome and rather expensive.
- Partial shading can affect the normal operation of the MPPT. Power loss may
  occur during partial and thus the algorithm must take this into account if
  possible.
- Cost of the MPPT must be taken into consideration. System features will
  determine most of the cost, such as digital or analog, programming and
  software requirements and number of sensors. Analog algorithms are
  normally cheaper.
- Different MPPT techniques are more suitable for different applications.
   Depending on the application, the algorithm must match the requirements of that application. Different algorithms may have different results depending on the application.

#### 2.2 Direct MPPT algorithms

Since exact knowledge of a PV panel is needed for the indirect methods to work, the research will focus on the direct methods. The methods are perturb and observe, hill climbing and incremental conductance. A brief explanation of each is discussed below:

#### Perturb and observe

According to Hohm and Ropp (2003) the most commonly used algorithm in commercial MPPTs is the perturb and observe (P&O) method. The structure of the P&O algorithm is that of simple regulation with a few parameters of measurement. It involves perturbation in the operating voltage of a PV panel.

This means it senses the voltage of the PV panel via a voltage sensor and periodically increments or decrements the operating voltage and then it compares the power obtained in the current cycle with that obtained in the previous cycle (de Brito *et al.*, 2011).

#### • Hill climbing

Hill climbing also involves perturbation but it differs from P&O in the sense that has perturbation in the duty cycle of the power converter. The duty cycle is perturbed, which in turn perturbs the PV panel operating current and consequently perturbs the PV panel operating voltage (Esram and Chapman, 2007).

## • Incremental conductance (IncCond)

The IncCond method is the same as the P&O method in the sense that it monitors both the voltage and current of the PV but there is no need to calculate the PV power. The basic principle of IncCond is the fact that the power slope of the PV is zero at the MPP (dP/dV = 0), thus the MPP can be tracked in terms of the increment in the array conductance (Zegaoui *et al.*, 2011).

Comparing the algorithms according to the main criteria described previously along with numerous other aspects taken into account, the following should be included with the chosen algorithm.

- It has to be a direct method, meaning it is not model-based and, therefore, does not depend of the PV panel characteristics.
- The algorithm should be easy to implement into a microcontroller.
- The sensor can be either analog or digital depending on the design.
- Partial shading problem should be partially eliminated by modifying the algorithm.
- Fast tracking should be achieved with high efficiency by modifying the algorithm according.

The next section will describe the P&O algorithm, as it is the chosen method to be implemented into the system.

#### 2.3 P&O algorithm

As described previously the P&O algorithm senses the voltage of the PV panel via a voltage sensor and periodically increases/decreases the operating voltage. It then compares the power obtained in the current cycle with that obtained in the previous cycle. Petreuş *et al.* (2011) indicate that to adjust the panel voltage, a DC-DC SMPS needs to be placed between the PV panel and the load, which is normally a battery bank. In this case, the load will not be a battery but the hydrogen generator and storage tanks. The algorithm will continuously change the duty cycle to the DC-DC SMPS, thus extracting the maximum power available from the PV panel. As Figure 8 indicates, the DC-DC SMPS input signals are the PV panel voltage  $V_{PV}$  and the PV panel current  $I_{PV}$ , thus the PV panel power is  $P_{PV} = I_{PV} \cdot V_{PV}$ .

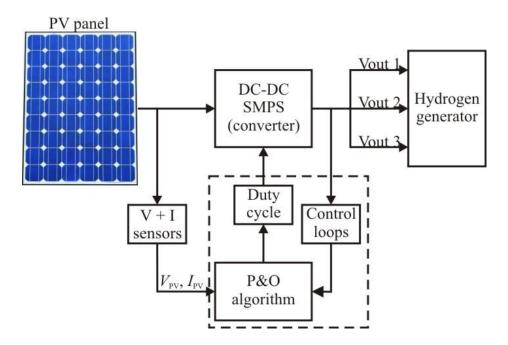


Figure 8 MPPT scheme of PV system

Figure 9 is adapted from studies done by Zegaoui *et al.* (2011) and Onat (2010b), which shows a family of P-V characteristic curves, at different irradiance (Irr) levels, for uniform irradiance and temperature. Assume the PV array is operating at point A in Figure 9. First, the input voltage of the PV array  $V_{PV}$  is measured by the voltage sensor.  $V_{PV}$  is then perturbed by a small increment, and the resulting change in PV array power ( $\Delta P_{PV}$ ) is calculated. If  $\Delta P_{PV}$  is positive, meaning an increase in PV array power, then the increase in  $V_{PV}$  moved the operating point of the PV array

closer to that of the MPP at point B (Femia *et al.*, 2005). Thus, further perturbing the  $V_{PV}$  in the same direction (with the same algebraic sign) moves the operating point closer and closer to the MPP until it reaches the MPP. If the  $\Delta P_{PV}$  is negative and operating at point C, meaning a decrease in PV array power, the operating point moved away from the MPP. When this happens the perturbation of  $V_{PV}$  is reversed (the algebraic sign is reversed) to move back in the direction of the MPP toward point D. This process is continuously repeated until the MPP is reached, thus the algorithm has a small oscillation about the MPP point resulting in a small percentage power loss (Esram and Chapman, 2007).

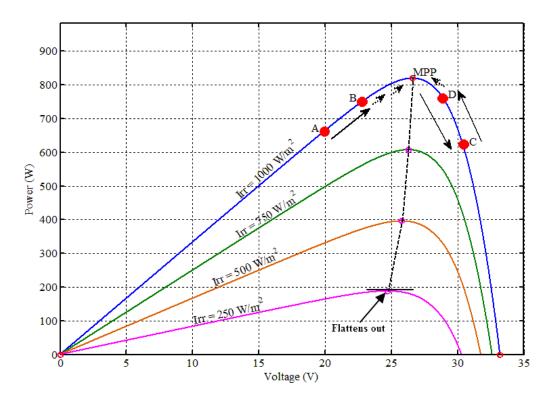


Figure 9 P-V Characteristic family curve

The P&O algorithm can be summarised as indicated in Table 4.

Table 4 Summary of P&O algorithm

Perturbation   Change in Power		Next Perturbation
Positive	Positive	Positive
Positive Negative		Negative
Negative Positive		Negative
Negative	Negative	Positive

The P&O algorithm can also be expressed in the form of a flowchart. By using a flowchart, the algorithm can easily be programmed onto a MCU. Figure 10 represents the basic operation principle (Atallah *et al.*, 2014).

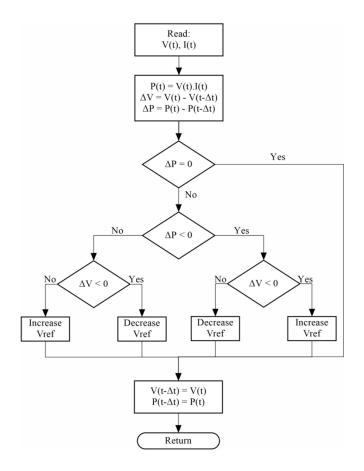


Figure 10 Flowchart of the P&O algorithm

Due to the ease of simplicity and implementation, there are a few drawbacks regarding P&O. One of these limitations is that when the irradiance decreases the P-V curve flattens out, as seen in Figure 9. This occurrence makes it difficult for the algorithm to discern the location of the MPP, due to the small change in power regarding the perturbation of the voltage. Another small drawback, as mentioned earlier, is that the algorithm oscillates around the MPP causing small power losses. One last drawback occurs at rapidly changing atmospheric conditions such as the irradiance. As seen in Figure 11, when the irradiance increases the power curve is shifted from P1 to P2 within the same sampling period. The operating point moves from A to C, this shifting of the curve indicates an increase in power, thus the perturbation stays the same according to the principles of operation of the P&O

algorithm. The operation point will keep diverging from the MPP as the irradiance increases (Onat, 2010a; Esram and Chapman, 2007).

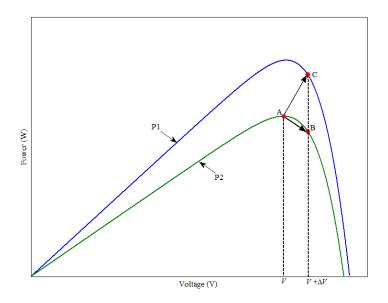


Figure 11 Divergence of P&O from MPP

Despite the abovementioned drawbacks, the P&O is still widely used. Much research has been done to improve the efficiency of the P&O algorithm by either completely or partially overcoming the drawbacks mentioned. By adding the optimisations that follow, the efficiency of the P&O algorithm can be increased to about 95-98%. The following are optimisations of the fundamental P&O algorithm to increase efficiency (Hohm and Ropp, 2003; Esram and Chapman, 2007):

- Variable-step perturbations. When the operating point is far from the MPP, large perturbation steps are used; as the operating point nears MPP, smaller steps are used. This increases the tracking of the MPP.
- Introduction of a 'waiting' function that causes a temporary termination of
  the perturbations if the algebraic sign changes several times in succession,
  indicating that the MPP has been reached. This function reduces the
  oscillation around the MPP in the steady state under constant irradiance
  conditions. This, however, slows the response time to changing atmospheric
  conditions.
- Optimising the sampling rate as well as introducing a high sampling speed.
   These two optimisation methods are used to overcome the slow response time

with the previously mentioned optimisations. However, it will also increase the response time according to rapid changing atmospheric conditions.

#### 2.4 DC-DC Switch Mode Power Supply (SMPS)

As indicated in Figure 8, a DC-DC SMPS is incorporated between the PV panel and the HG. As Kalogirou (2009) explains, the MPP, which is the optimum operating voltage, varies according to changes in temperature and irradiance. Thus, the DC output voltage from the PV panel is unregulated. DC-DC SMPS play the role of converting the unregulated voltage into a controlled and stable output voltage (Mohan *et al.*, 2003).

# 2.4.1 Types of DC-DC converter topologies

There are two basic converter topologies, namely step-down voltage (buck) and step-up (buck). Then, there are two variations of these two topologies, namely buck-boost and čuk converters. The advantage of these types of converters is that they do not require a transformer. These converter topologies are also non-isolated converters, which means the output and input has no dielectric isolation between them. Below are short explanations of these converters.

#### • Buck converter

Buck converters are current step-up and voltage step-down devices. The input voltage is higher than the output voltage and the input current is lower than the output current (Agrawal, 2001).

#### Boost converter

Boost converters are current step-down and voltage step-up devices. Where the input voltage is lower than the output voltage and the input current is higher than the output current (Agrawal, 2001).

#### • Buck-boost converter

This type of converter is a combination of a buck topology in cascade with a boost topology. Either a step-up or step-down function can be utilised at any time (Agrawal, 2001).

#### • Čuk converter

The čuk converter configuration is almost the same as the buck-boost converter and can deliver either the step-up or step-down voltages, but with inverted polarity (Agrawal, 2001).

#### 2.4.2 The buck converter

The chosen DC-DC converter topology is the buck converter because the voltage required by the power supply as indicated in Table 1 is less than that supplied by the PV panel.

In Figure 12 below, the basic buck converter topology is shown. The circuit consists of a DC input voltage (unregulated)  $V_{PV}$ , a mosfet switch Q, a diode D, an inductor L, filter capacitor C, and the HG as the load. Though for clarity the HG structure is not shown (Mack, 2005).

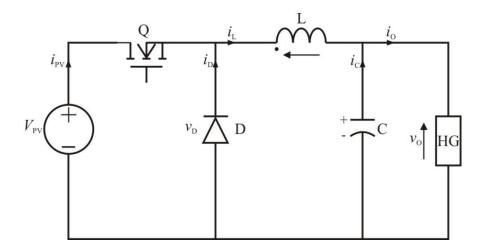


Figure 12 Buck converter topology

It is important to note that according to Janse van Rensburg (2012) the output voltage's magnitude is directly proportional to the duty cycle of the switch Q, which is operated at a high frequency.

For the operation of the buck converter, it is assumed that the circuit is running in the steady-state. The steady-state operation has two states, namely:

• Switch Q closed: If switch Q is closed/turned on, diode D does not conduct, because it is reversed biased. The inductor opposes a change in current, thus

if switch Q is closed the inductor stores energy in its magnetic field. The capacitor opposes a change in voltage, therefore, capacitor charges during this stage (Jacob, 2002).

• Switch Q open: If switch S is open/turned off, diode D is forward biased because the polarity of the inductor L is reversed. If switch Q is open, the inductor generates current. Also, during this stage the voltage starts to drop, therefore, the capacitor discharges, sending current to the HG to hold the voltage up (Jacob, 2002).

Janse van Rensburg (2012) also states that the net charge and discharge over one cycle is zero, thus the capacitor voltage stays constant.

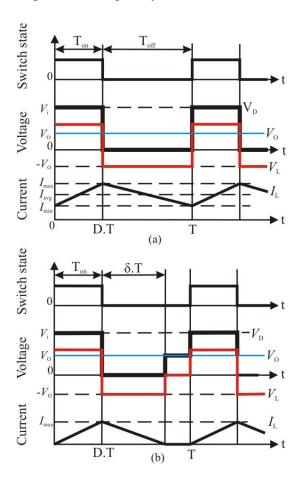


Figure 13 Buck converter steady-state operating modes: (a) CCM and (b) DCM

When running in steady-state, there are two definable operating modes with respect to the inductor current  $i_L$ . If the inductor current always stays positive and never falls to zero at any given time during the switching period, it is called the continuous

conduction mode (CCM). The other mode is the discontinuous conduction mode (DCM). That is where the inductor current goes to zero during each switching period (Siwakoti *et al.*, 2010). Figure 13 distinguishes between the two modes.

The input voltage is chopped into a rectangle by switching switch S on and off. The duty cycle of the switch is D, given by

$$D = \frac{t_{\text{on}}}{T_{\text{period}}} \tag{1}$$

Where:

 $D \equiv \text{Duty cycle}$ 

 $t_{\rm on} \equiv \text{Time on}$ 

 $T_{\rm period} \equiv \text{Total time on and off for Switch S}$ 

The output voltage across the load is a fraction of the input voltage, and this fraction is equal to the duty cycle, therefore, the duty cycle can also be expressed as:

$$D = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{2}$$

Where:

 $V_{\text{out}} \equiv \text{Voltage across the load (HOGEN®GC300)}$ 

 $V_{\rm in} \equiv \text{Input voltage (PV panel)}$ 

Thus, the voltage across the HG can be expressed as:

$$V_{\text{out}} = D \bullet V_{\text{in}} \tag{3}$$

It is important to note that the MPPT must continuously track the MPP with the highest possible efficiency. Therefore, the CCM is chosen as the operation mode for the buck converter because the inductor current is never zero and constant power will be delivered to the HG.

It must be included that it is possible to go from CCM to DCM. Siwakoti *et al.* (2010) indicates that this happens when the switching frequency is low and/or the input current is low. To prevent this situation from happening, the diode is replaced

by a second mosfet switch. This new arrangement according to Vazquez *et al.* (2010) is known as synchronous rectification and the second mosfet is called a synchronous rectifier. Figure 14 shows the synchronous buck converter configuration.

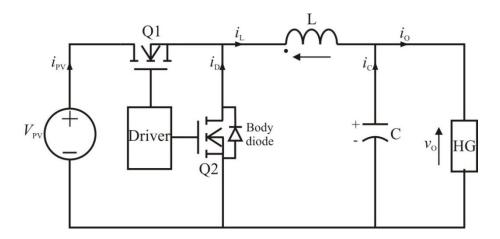


Figure 14 Synchronous buck converter

According to Vazquez *et al.* (2010), the advantage of the second mosfet (Q2) is that the voltage drop across the mosfet is much lower than that of the diode, even a Shottky diode, which has a voltage drop of 0.3 V to 0.4 V. The replacement of the diode will result in much higher circuit efficiency. It is also important that the two mosfets are not switched on at the same time in order to prevent a short circuit across the source (PV panel). Therefore, a 'dead time' is built into the switching control, meaning one mosfet is turned off before the other mosfet is turned on (Siwakoti *et al.*, 2010). For improved switching, a diode is placed in parallel with the second mosfet (Q2) to provide a conducting path for the inductor current for the small period when both mosfets are off (dead time). The diode can either be a Shottky diode or the mosfet body diode (Vazquez *et al.*, 2010). The mosfet body diode will be chosen is stead of the Shottky diode in order to maintain a high efficiency.

### 2.5 Control of the DC-DC SMPS

A DC-DC SMPS can be controlled either by hard-wired analog controllers or by software driven digital controllers. Software driven digital controllers are preferable due to less sensitivity to the aging of components and electrical noise and the adaptability to digital control methods such as the proportional-integral-derivative control (PID) of the power supply's response to the load and source variation,

interferences, and transients. There are three types of control modes that can be implemented, namely voltage-mode control (VMC), current-mode control (CMC) and proportional-integral-derivative (PID) control (Agrawal 2001:473-474).

## 2.5.1 Voltage-mode control

In the voltage-mode control, the output of the SMPS is divided using a voltage divider sub-circuit, which is then subtracted from a reference voltage and compensated using an error amplifier. Next, the error voltage at the output of the error amplifier is compared to a saw-tooth to generate the driving signal for the switching transistor. Thus, voltage-mode control is a **single loop** control technique (Agrawal 2001:473-474). Figure 15 illustrates the voltage-mode control applied in a circuit.

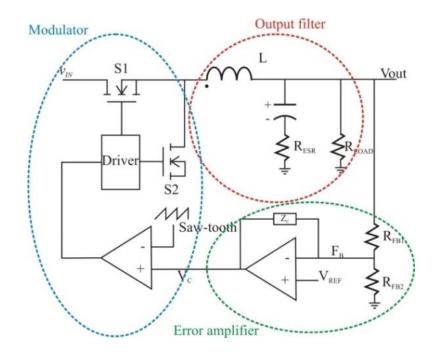


Figure 15 Voltage-mode control

Listed below are the advantages and disadvantages of the voltage-mode control:

## Advantages:

- Less sensitive to noise because of a large-amplitude ramp waveform, thus a
  more stable modulation.
- A single feedback loop makes it easier to design and analyse.

 Works over a wide range of duty cycles because it has better cross-regulation due to the low-impedance output power.

# Disadvantages:

- Compensation is complicated due to the fact that the loop gain is proportional to the input voltage.
- The differences between CCM and DCM create a compensation challenge.
- Slow response to input voltage changes due to the fact that the changes must first be sensed as an output change and then corrected by the feedback loop.
- Current limiting must be done separately.

### 2.5.2 Current-mode control

Current-mode control is **multi-loop** control. The outer loop is a voltage-loop, so the voltage still has to be sensed and subtracted from a reference voltage and compensated for, but now the error amplifier output provides a reference for the inner current loop. In the inner loop a current in the system is sensed (by using a current sense resistor or otherwise) and compared to the reference (from the voltage loop) and this is used to generate the switching signal for the transistor. Usually the inner current loop is faster than the outer voltage loop. Figure 16 illustrates the current-mode control applied in a circuit.

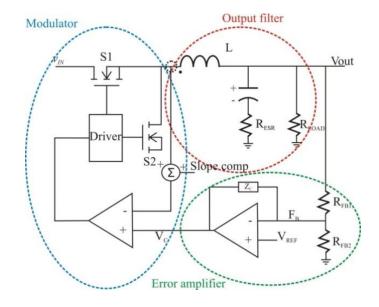


Figure 16 Current-mode control

There are also a number of current-mode control types: peak current-mode control, average current-mode control and hysteretic current mode control (Agrawal 2001:473-474). The most important aspect in the current-mode control design is to keep noise off the compensation ramp. Listed below are the advantages and disadvantages of the current-mode control.

# Advantages:

- Due to the fact that the error amplifier is now used to work with the output current rather than with the voltage, the output inductor effect is minimised and the filter offers only a single-pole to the feedback loop, resulting in simpler compensation and higher gain bandwidth.
- It responds immediately to line voltage changes because the inductor current rises with a slope determined by the difference between the input and output voltage, thus eliminating not only the delayed response but also the gain variation with changes in input voltage.
- Inherent cycle-by-cycle current limiting protection, by clamping the command from the error amplifier, making it immune to over-current damage from short-circuited outputs or overloads.
- Current sharing when multiple supply units are in parallel.

## Disadvantages:

- Circuit analysis is more difficult because of the two feedback loops.
- There is sub-harmonic oscillation instability when approaching a 50% duty cycle, unless compensation is added.
- Resonances in the power stage can insert noise into the control loop because the control modulation is based on a signal derived from the output current.
- Another noise source is the leading edge current spike normally caused by transformer winding capacitance and output rectifier recovery current.
- For multiple outputs, coupled inductors are required to get acceptable crossregulation because the control loop is forcing a current drive making the load regulation worse.

Table 5 gives a comprehensive comparison of the two different control modes (Maniktala, 2012).

Table 5 Comparison of the voltage and current-mode control techniques

	CMC	VMC
Rejection of line disturbances	Good (inherent)	Very good (with
(dynamic line response)		line feedforward)
Rejection of load disturbances	Good (constant	Good
(dynamic load response)	bandwidth)	
Constant frequency	Excellent	Excellent
Predictable EMI	Excellent	Excellent
Audible noise suppression	Excellent	Excellent
Extreme down conversion (buck)	Poor	Good
Insensitivity to PCB layout	Poor	Excellent
Excellent stability of loop	Excellent	Good
responses (tolerances and long-		
term drifts)		
Simplicity of compensation	Good	Poor
I <sub>Q</sub> (quiescent current)	Good	Poor
Loop stability with use of output	Excellent (with type	Very good
ceramic caps	3 compensation)	
Auto-tuning	Complex	Very complex

According to Mammano (1994) there are considerations to be made, which would point to a more optimum solution for a specific application. There will be trade-offs for either selection, but choosing the optimum solution will increase the efficiency of the DC-DC SMPS. Choosing a control mode is as follows:

Consider the use of the current-mode control if:

- The output is to be either a very high output voltage or current source
- The fastest possible response time is required for a given frequency
- When the input voltage variation is relatively constrained
- For applications where parallel load sharing is required

- Where transformer flux is important in push-pull circuits
- For low-cost applications with the absolute minimum number of components.

Consider the use of the voltage-mode control if:

- The possibility of wide input line and/or output load variations is possible
- With light load conditions, where the current ramp slope is too low for stable pulse-width modulation (PWM) operation
- Noisy and/or high power applications, where noise on the current waveform would be difficult to control
- Good cross-regulation with multiple output voltages is required
- Saturable reactor controllers are to be used as auxiliary secondary-side regulators
- In hardware designs where the complexity of slope compensation and/or dual feedback loops needs to be avoided.

## 2.5.3 Proportional-integral-derivative (PID) controller

The PID controller is used in conjunction with either the voltage-mode control or the current-mode control. The PID controller calculates an error value as the difference between a measured parameter (value provided by the voltage/current-mode control) and a desired set point (desired output voltages of the SMPS). The controller then tries to minimise this error value by adjusting the process through the use of manipulated values. The PID controller will reduce the rise-time to reach the desired output, eliminate the steady-state error, increase system stability, reduce the overshoot and improve the transient response (Ibrahim, 2002). The PID algorithm is described by the following equation:

$$u(t) = K_{p}e(t) + \frac{K_{p}}{T_{i}} \int_{0}^{t} e(t)dt + K_{p}T_{d} \frac{de(t)}{dt}$$

$$\tag{4}$$

Where:

 $e(t) \equiv \text{Error signal}$   $T_i \equiv \text{Integral time constant}$   $K_p \equiv \text{Proportional gain}$ 

 $u(t) \equiv \text{Control input}$   $T_d \equiv \text{Derivative time constant}$ 

Refer to Figure 17. The PID controller is explained as follows: variable e represents the tracking error, the difference between the set point, which is the desired input value (r) and the actual measured output (y). This error signal (e) is sent to the PID controller. The controller then computes the control signal (u), which is the sum of three terms: the P-term (which is proportional to the error), the I-term (which is proportional to the integral of the error), and the D-term (which is proportional to the derivative of the terror). The controller parameters are proportional gain  $K_p$ , integral time  $T_i$ , and derivative time  $T_d$ . The control signal (u) is sent to the plant (which is the physical parts of the system), for error correction in order to obtain a new output (y). This process is repeated continuously through the feedback loop.

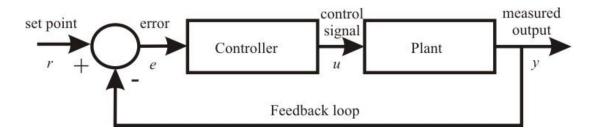


Figure 17 Unity feedback system (closed loop)

The characteristics of the P, I and D controllers are as follows:

- Proportional control (P): Reduce rise time (response time). Reduce but never eliminate the steady-state error. An increase in proportional gain will decrease the rise time but will also increase the overshoot.
- Integral control (I): Eliminating steady-state error, but may also decrease the transient response. Too much integral action will result in large overshoot and an oscillation at the output. Large integral action can also increase the system settling time and decrease rise time.
- Derivative control (D): Increases system stability, reduces the overshoot and improves the transient response. Increasing the derivative action will decrease both the system settling time and the overshoot.

The effects of each of the P, I and D controllers on a closed-loop system are summarised in Table 6.

Table 6 Effect of PID controllers on closed-loop system

Close-loop response	Rise time	Overshoot	Settling time	S-S error
P	Decrease	Increase	Small change	Decrease
I	Decrease	Increase	Increase	Eliminate
D	Small change	Decrease	Decrease	Small change

The P, I and D gains are dependent on each other, thus when changing one of these parameters has an effect on the other two. The process of setting the optimal gains for P, I and D to get an ideal response from the control system is called tuning. There are different methods of tuning but the two most popular methods are the trial and error method and the Ziegler-Nichols method.

### Trial and error method

First, the I and D parameters are set to zero and the P parameter is increased until the output of the loop oscillates. As the proportional gain is increased, the system becomes faster, but should not be so fast that the system becomes unstable. Once P has been set to obtain a desired fast response, the I parameter is increased to stop the oscillations. The I reduces the steady state error, but increases overshoot. Some amount of overshoot is always necessary for a fast system so that it could respond to changes immediately. The I parameter is tweaked to achieve a minimal steady state error. Once the P and I have been set to get the desired fast control system with minimal steady state error, the D parameter is increased until the loop is acceptably quick to its set point. Increasing the D parameter decreases overshoot and yields higher gain with stability but would cause the system to be highly sensitive to noise. Thus, a trade-off must be made to one of the characteristics of the control system for another in order to meet the requirements of the system (Goodwin *et al.*, 2001).

## **Ziegler-Nichols method**

This method of tuning is based on closed-loop test. Referring to Figure 18, the testing procedure is as follows (Webb and Reis, 2003):

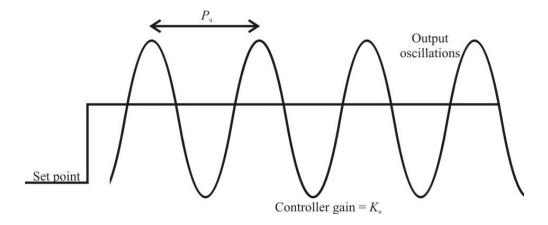


Figure 18 Ziegler-Nichols closed-loop tests

- Parameters I and D are set to zero and leave only P in action
- Make a set point step test and observe the response
- Repeat the above test with the added action of either increasing or decreasing the controller gain until the oscillation is stable. This gain is called the 'ultimate gain',  $K_{\rm u}$ .
- Note the period of this steady oscillation and let this be  $P_{\rm u}$ .
- Calculate the controller parameters according to Table 7 below.

Table 7 Ziegler-Nichols tuning, using the oscillation method

Control	P	I	D
P	$0,50K_{\rm u}$	-	-
PI	$0,45K_{\rm u}$	$P_{\rm u}/1,2$	-
PID	$0,60K_{\rm u}$	$P_{\rm u}/2$	$P_{\rm u}/8$

After considering all the aspects mentioned above, the voltage-mode control in conjunction with a PID controller is chosen as the best possible solution for this specific project (Webb and Reis, 2003). The PID controller will be implemented, not through hardware but through software, meaning the PID algorithm will be programmed onto the MCU. The algorithm is as follows:

pre\_error = 0; epsilon = 0,01; 
$$dt$$
 = 0,01;  $K_p$  = P;  $T_i$  = I;  $T_d$  = D

If error > epsilon

```
integral = integral+ error•dt;

derivative = (error- pre_error) / dt;

output = K_p•error+T_i•integral+T_d•derivative;

pre_error = error;

end;
```

The P, I and D characters will be replaced by the values calculated according to the Ziegler-Nichols tuning method.

# 2.6 Synchronous buck converter design equations

Before the SMPS can be designed, calculations need to be done in order to establish the correct component selections for the three synchronous buck converters according to the parameters of the system as a whole. The following component values need to be calculated:

- Inductor value in micro-Henry (µH)
- Input filter capacitor in micro-Farad (μF)
- Output capacitor in micro-Farad (μF)

The system parameters need to be established before any calculations can begin, and are as follows:

- $V_{\text{IN\_MIN}}$ : Minimum input to the converter in volt (V)
- $V_{\text{IN\_MAX}}$ : Maximum input to the converter in volt (V)
- $f_{SW}$  : Converter switching frequency (kHz)
- $V_{\text{OUT}}$ : Output voltage of the converter in volt (V)
- $I_{OUT}$ : Output current of the converter in amp (A)
- $P_{OUT}$ : Output power of the converter in watt (P)
- $D_{\text{max}}$  : Maximum duty cycle

First, the load resistance needs to be calculated in order to calculate the inductor value.

$$R = \frac{R_{\text{out}}}{I_{\text{out}}} \tag{5}$$

Where,

 $R \equiv \text{Load resistance in Ohms}(\Omega)$ 

Once the load resistance is calculated, the inductor value can be calculated as follows:

$$L_{\min} = \frac{(1-D)R}{2f_{\text{SW}}} \tag{6}$$

Where.

 $L_{\min} \equiv \text{Minimum inductor value in micro - Henry } (\mu \text{H})$ 

 $f_{\text{SW}} \equiv \text{Switching frequency in kilohertz (kHz)}$ 

 $D_{\text{max}} \equiv \text{Maximum duty cycle}$ 

To make sure the inductor current is continuous, choose an inductor value 25 percent larger than the minimum value. Thus,

$$L = 1,25 \times L_{\min} \tag{7}$$

Where,

 $L \equiv \text{Inductance in } \mu \text{H}$ 

For the change in the inductor current:

$$\Delta i_{\rm L} = \left(\frac{V_{\rm IN\_MAX} - V_{\rm out}}{L f_{\rm SW}}\right) D_{\rm max} \tag{8}$$

Where,

 $\Delta i_{\rm L} \equiv$  Change in inductor current

The average inductor current must be the same as the average current in the load resistor and since average capacitor current for steady-state operation is zero:

$$I_{\rm L} = I_{\rm R} = \frac{V_{\rm out}}{R} \tag{9}$$

Where,

 $I_{\rm L} \equiv \text{Inductor current in ampere (A)}$ 

For the maximum and minimum inductor current:

$$I_{\text{max}} = I_{\text{L}} + \frac{\Delta i_{\text{L}}}{2}$$

$$= \frac{V_{\text{out}}}{R} + \frac{1}{2} \left[ \frac{V_{\text{out}}}{L} (1 - D_{\text{max}}) T \right]$$

$$= V_{\text{out}} \left( \frac{1}{R} + \frac{1 - D_{\text{max}}}{2L f_{\text{SW}}} \right)$$
(10)

Where,

 $I_{\text{max}} \equiv \text{Maximum inductor current in A}$   $I_{\text{L}} \equiv \text{Inductor current A}$   $T \equiv 1/f_{\text{SW}}$ 

$$I_{\text{max}} = I_{\text{L}} - \frac{\Delta i_{\text{L}}}{2}$$

$$= \frac{V_{\text{out}}}{R} - \frac{1}{2} \left[ \frac{V_{\text{out}}}{L} (1 - D_{\text{max}}) T \right]$$

$$= V_{\text{out}} \left( \frac{1}{R} - \frac{1 - D_{\text{max}}}{2L f_{\text{SW}}} \right)$$
(11)

Where,

 $I_{\min} \equiv \text{Minimum inductor current A}$ 

The inductor must also be rated for rms current:

$$I_{\rm Lrms} = \sqrt{I_{\rm L}^2 + \left(\frac{\Delta i_{\rm L}}{2\sqrt{3}}\right)^2} \tag{12}$$

Where,

 $I_{Lrms} \equiv Inductor current root mean square$ 

The output-voltage ripple must also be considered and chosen.

$$\Delta V_{\text{out}} = \frac{V_{\text{out}} \left(1 - D_{\text{max}}\right)}{8LCf^2} \tag{13}$$

Where,

 $\Delta V_{\text{out}} \equiv \text{Peak} - \text{to-peak ripple voltage in volt (V)}$ 

The ripple voltage can also be expressed as a fraction of the output voltage:

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \frac{(1 - D_{\text{max}})}{8LCf^2}, \text{ expressed as a percentage (choose manually)}$$
 (14)

Once the ripple voltage is chosen, the output capacitor can be calculated as follows:

$$C_{\text{out}} = \frac{1 - D_{\text{max}}}{8L \left(\frac{\Delta V_{\text{out}}}{V_{\text{out}}}\right) f_{\text{SW}}^2}$$
(15)

Where,

 $C_{\text{out}} \equiv \text{Output capacitance in micro-Farad} (\mu \text{F})$ 

Peak capacitor current is  $\frac{\Delta i_{\rm L}}{2}$ 

Maximum equivalent series resistance (ESR) of the capacitor:

$$r_{\rm C} = \frac{\Delta V_{\rm out}}{\Delta i_{\rm C}} \tag{16}$$

Where,

 $r_{\rm C} \equiv {
m Capacitor\ series\ resistance\ in\ } \Omega$ 

 $\Delta i_{\rm C}$  = Change in capacitor current, which is the same as  $\Delta i_{\rm L}$ 

The input filter capacitor is calculated by the following equation:

$$C_{\rm in} = I_{\rm out} \frac{\sqrt{V_{\rm out} \left(V_{\rm IN\_MAX} - V_{\rm out}\right)}}{V_{\rm IN\_MAX}}$$
(17)

Where:

 $C_{\text{in}} \equiv \text{Input capacitance in } \mu \text{F}$ 

## 2.7 Summary

This chapter emphasised the need for an adaptable MPPT algorithm to be considered when choosing the algorithm, because of variable PV panel characteristics. The chapter differentiated between the different algorithm methods. The P&O algorithm was chosen based on certain aspects and then explained in detail. A brief overview of

the HOGEN® GC 300 was given followed by the operation of the DC-DC SMPS that is needed to supply the correct DC voltages to the HOGEN® GC 300. The different control-modes for the DC-DC SMPS are discussed. Also the design equations for the DC-DC SMPS where included.

In Chapter 3, the design, programming and simulation will be shown in regard to the literature review addressed in this chapter.

## CHAPTER 3 DESIGN, PROGRAMMING AND SIMULATION

The equations shown in Chapter 2 can now be used to design the DC-DC SMPS. The DC-DC SMPS is designed with the MPPT algorithm and PID algorithm embedded into the MCU.

To design the DC-DC SMPS, each section of the circuit has to be calculated first according to Section 2.6 in Chapter 2 for component selection and then the relevant schematic of the circuit can be drawn with Altium designer. The main sections of the design are the following:

- First is the **controller circuit**. It includes the MCU, which is a dsPIC (digital signal processing MCU), programming and debugging port, MCU reference voltage and LEDs for visual representation of certain functions.
- Second is the **supply circuit**. It includes the following sub-circuits: PV power in, dsPIC supply offline/online, battery charging, 5V and 3.3V regulation.
- Thirdly are the **three separate synchronous buck converters** for the three different output voltages required by the HG and their voltage and current sensing circuitry.
- Fourthly is the **current and voltage sensing circuit** of the PV array required by the MPPT algorithm to calculate and track the MPP.
- Lastly are **the three separate voltage-mode control circuits**. Each synchronous buck converter has to have its own control-mode in order to deliver the correct voltage to the HG.

## 3.1 Controller and supply circuits

For this circuit no calculations are done but rather the component selection is done by referring to various datasheets and choices. Figure 19 shows the complete controller circuit with all its relevant sub-circuits. Each sub-circuit has a specific purpose in the design, which will be discussed and explained thoroughly.

Watchdog is the external watchdog circuit. The watchdog will reset the MCU
whenever a problem occurs during the operation of the system. Once the

MCU is reset, normal operation will continue. The watchdog IC (integrated circuit) is a DS1832, which works with 3.3V.

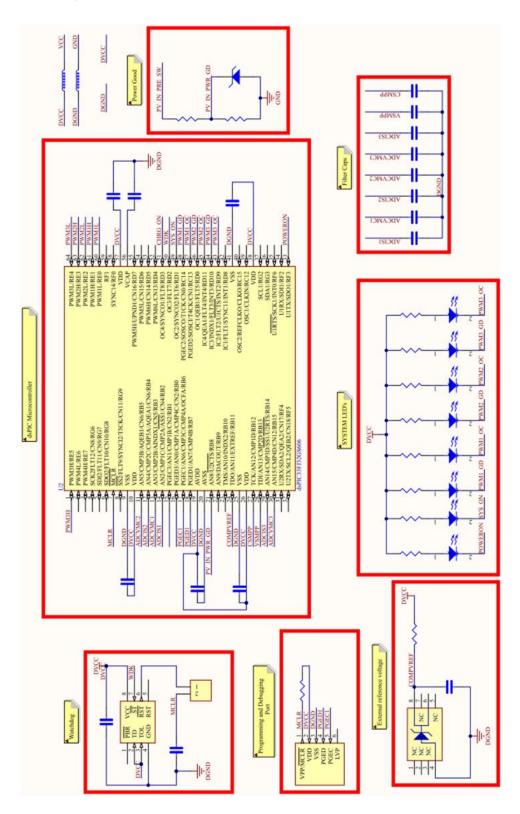


Figure 19 Controller circuit

- Programming and debugging port. The ICD 3 will load the C-code onto the MCU using the programming port. During programming of the C-code, the debugging feature will be used to load the C-code into the ICD 3 but not onto the MCU itself, thus enabling to test step by step if the C-code is working as it would when loaded onto the MCU.
- MCU reference voltage of 1.2V. The LT10041D-1V2 is a 1.2V reference IC.
   The reference voltage will be used by the comparator of the MCU in order to make certain calculations.
- The power good works in conjunction with the PV input, which is to monitor
  the incoming power from the PV array. The MCU will then calculate if the
  required power has been achieved and operation of the MPPT can begin.
- The system LEDs sub-circuit is for debugging purposes, but also for visual representation if the system is operational.
- The filter capacitors are to filter any noise on the analog-to-digital tracks.
- The dsPIC microcontroller section is the most important part because it is the intelligence of the whole system. A dsPIC33FJ32GS606 is used for all the calculations such as the PID control and MPPT algorithm handling. The dsPIC will perform the MPPT algorithm by continueosly sensing the voltage and current from the PV array through the sensing circuitry, which will be discussed. The dsPIC will then instruct the mosfet driver IC to switch the mosfets on/off according to the correct duty cycle and compute the voltage-mode control parameters along with the PID control so that the SMPS delivers the correct power. The capacitor values along with the inductor value connected to the dsPIC is provided by the datasheet.

Figure 20 is the supply circuitry. The circuitry consists of sub-circuits with each sub-circuit having a different purpose in the supply circuitry. Each sub-circuit is explained below:

PV power input sub-circuit is for the PV array input. The output of the PV array will go through a P-channel and N-channel mosfet. The P-channel mosfet serves as a small protection for the rest of the circuit for sudden influx

in power while the N-channel mosfet is for power-on monitoring. Only once the PV array reaches a certain output voltage will the system start up and perform the MPPT.

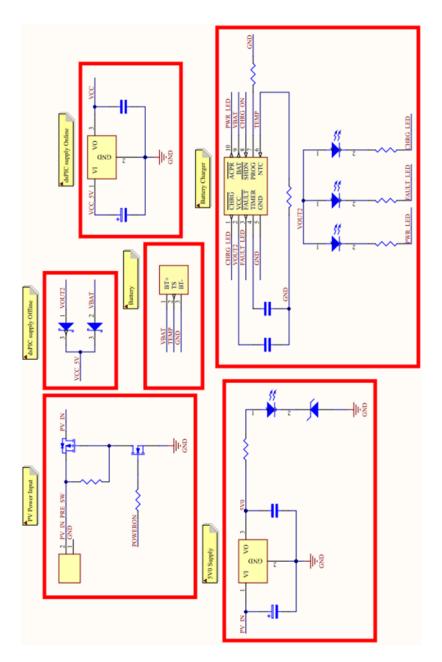


Figure 20 Supply circuit

The 5V0 sub-circuit provides the circuit where needed with 5V. The PV array voltage is connected to the VIN pin of the LM7805 and the output is a regulated 5V. The capacitor values and where to place them are provided by the datasheet of the IC.

The dsPIC supply online, dsPIC supply offline and battery charger subcircuits are an important part of the circuit. It provides the necessary 3.3V for the MCU to operate. When the power from the PV array reaches a certain value the MPPT will start to operate and the synchronous buck converters will output their selected output values. The output of the 5V synchronous buck converter is connected to a MIC5239 3.3V regulator IC. The IC will provide the MCU with the 3.3V in order to operate. However, during low PV array output power and no working converters, a small lithium battery is connected with the circuit to power the MCU and keep the MCU 'awake' so as to sense when PV array power has reached the desired power and normal SMPS functionality can begin again. During operation, the battery charger sub-circuit will charge the battery to the normal operating voltage. The capacitor values are provided by the datasheet.

## 3.2 The synchronous buck converter circuits

Each converter circuit will be calculated and designed separately but datasheet component values and the rule of thumb will also be used for certain component values. Each circuit uses a MCP14700 mosfet driver IC to drive the mosfets. All three circuits are identical except for their component values and output power. As stated in Chapter 2, all the converters are in the CCM.

The following values were decided upon before any calculations where started:

Table 8 Chosen SMPS parameter values for the calculations

Parameter	Value	
$V_{ m IN}$	14-40 V	
$V_{ m IN\_MIN}$	14 V	
$V_{ m IN\_MAX}$	40 V	
$f_{ m SW}$	600 kHz	
$V_{ m OUT1}$	12 V	
$I_{ m OUT1}$	4,2 A	
$P_{ m OUT1}$	50 W	
$V_{ m OUT2}$	7.5 V	
$I_{ m OUT2}$	20 A	
$P_{ m OUT2}$	150 W	
$V_{ m OUT3}$	5 V	
$I_{ m OUT3}$	10 A	
$P_{ m OUT3}$	50 W	

The values in Table 9 were calculated by substituting the values in Table 8 into the equations explained in Chapter 2.

**Parameters** 12 V, 4.2 A, 50 W 7.5 V, 20 A, 150 W 5 V, 10 A, 50 W Value Value Value  $2,857 \Omega$  $0,375 \Omega$ 0,857 0,536 D 0,357  $L_{\min}$ 34 µH  $14,5 \mu H$ 26,79 μΗ 42,5 μH  $18,13 \mu H$ 33,49 µH L 224 mA 67 mA 224 mA  $\Delta i_{\rm I}$ 4,2 A  $I_{\rm L}$ 20 A 10A I<sub>max</sub> 4,234 A 20,112 A 10,112 4,167 A 19,888 A 9,888  $I_{\min}$  $\frac{I_{\mathrm{Lrms}}}{\Delta V_{\mathrm{out}}}$ 4,2 A 20 A 10 A 0.5% 0.5% 0.5%  $V_{
m out}$  $600 \mu V$ 37,5 mV 0,025 μV 23,366 μF 1,777 μF 1,333 μF 8,955 mΩ 167,41 mΩ  $1,116 \Omega$  $r_{\rm C}$ 9,974 F

Table 9 Calculated values for the synchronous buck converters

Figure 21 shows the schematic circuit for the three synchronous buck converter circuits and where each component is placed within the circuit. By consulting the MCP14700 IC datasheet the values for two of the capacitors where inserted.

4,971 F

1,469 F

 $C_{\rm in}$ 

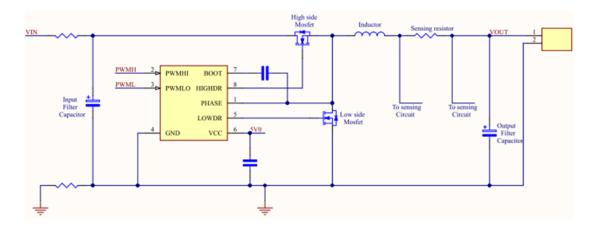


Figure 21 Synchronous buck converter schematic circuit

The 5V to the IC is provided by the 5V regulator IC of the supply circuit. The MCU provides the high-side and low-side outputs of the PWM and the IC will then switch the two mosfets on/off accordingly. The sensing resistor is connected to the corresponding sensing circuitry of each converter in order to sense the voltage and

current for the voltage-control mode and PID control and 'feed' those values to the MCU. The MCU will then calculate and adjust the duty cycle to keep the output power stable.

An important part in designing the converter circuit is the selection of the mosfets. When choosing the mosfets, there are three important parameters that need to be considered, namely:

- Drain to source voltage (V<sub>GS</sub>)
- V<sub>GS(th)</sub> (only according to the MCP14700 output voltage on the driver pins)
- $\bullet$  R<sub>DS(on)</sub>

Decisions based on known parameter values:

- ullet Choose a mosfet with a  $V_{GS}$  that is about two and a half times higher than the input voltage
- $\bullet$  Make sure the driver output is higher than the mosfet  $V_{GS(th)}$ . For the MCP14700 the driver output is 5V
- Choose a mosfet with a low R<sub>DS(on)</sub> value

The sensing resistor of Figure 21 is connected to the circuit showed in Figure 22 below.

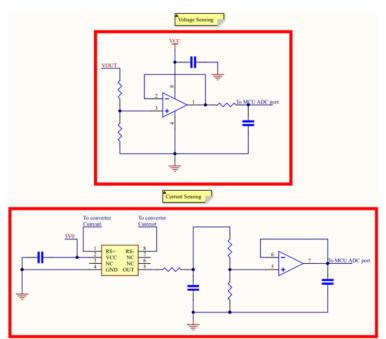


Figure 22 Synchronous buck converter sensing schematic circuit

The sensing resistor is connected to a MAX4080 current sensing IC. The IC uses an amplification of 20 in order to sense the current. The output from the IC is then 'fed' to and opamp with a certain analog value. Along with the current sense, there is a voltage-sensing circuit, which outputs a certain value. Both the voltage and the current sensing outputs are connected to the ADC ports of the MCU. The voltage-mode control will be implemented by the MCU using the values from the sensing circuitry.

# 3.3 The MPPT sensing circuit

Figure 23 is the voltage and current sensing circuitry for the PV array. This sensing circuit will measure the voltage and current from the PV array and 'feed' those values to the MCU. The MCU will then use these values in order to calculate the MPP. The MPPT algorithm will then set the correct duty cycle for each converter.

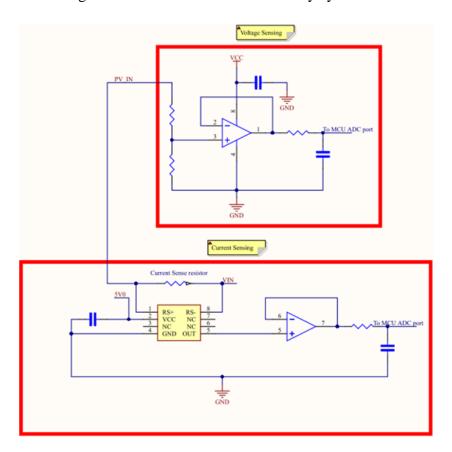


Figure 23 MPPT voltage and current sensing schematic circuit

Figures 24 and 25 show the PCB in a 3D view. The physical properties of the components such as lengths, widths, heights and outline are rendered in 3D, thus

allowing for a real-life perspective of the PCB. This allows for the designing of an enclosure around the PCB while it is still in the design process, without first having to manufacture the PCB and then design the enclosure.

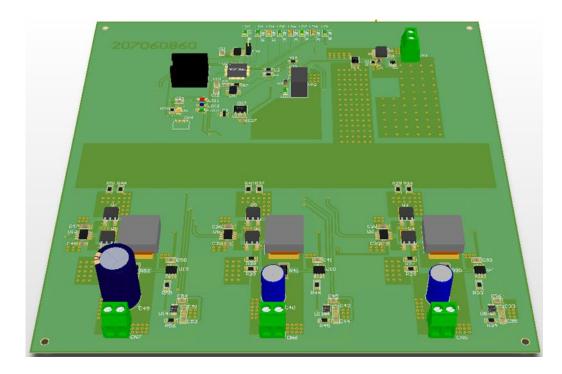


Figure 24 PCB 3D view - Top

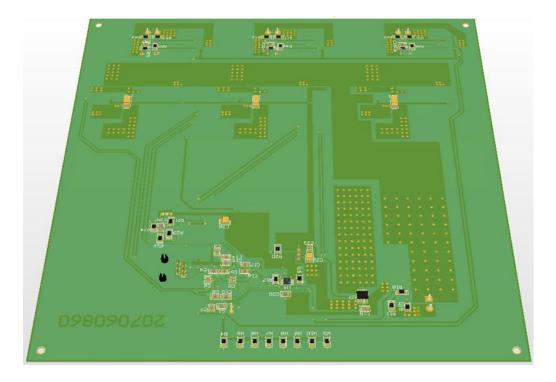


Figure 25 PCB 3D view - Bottom

### 3.4 Programming

The dsPIC was programmed with the Microchip MPLabX IDE software package. The c-code was developed specifically for this research by the author. The C-coding of the dsPIC consists of multiple aspects, which are as follows:

- Setting up the registers
- Setting up the I/O ports (Input/output ports)
- Defining variables
- Setting up the PWMs of the dsPIC
- Reading the PV array voltage and current
- Implementing the MPPT algorithm
- Measuring the output of the DC-DC SMPS
- Implementing the PID algorithm for stable outputs.

See Annexure C for the full dsPIC MCU author C-code.

## 3.5 Simulation setup

The previous sections considered the design of the DC-DC SMPS. The section is concerned with the simulation of the system as a whole. The simulation of the design is done in Simulink. Simulink is a graphical simulation extension of Matlab. The simulation will not have all the components that are present in the PCB design nor will it be designed in the exact same manner, but it will return results that will verify the design. The main Simulink model comprises of various structures. They are as follows, as seen in Figure 26:

- Irradiance and temperature input
- MPPT algorithm
- PV array
- Synchronous buck converter sections
- HG load section
- Scopes and measurements.

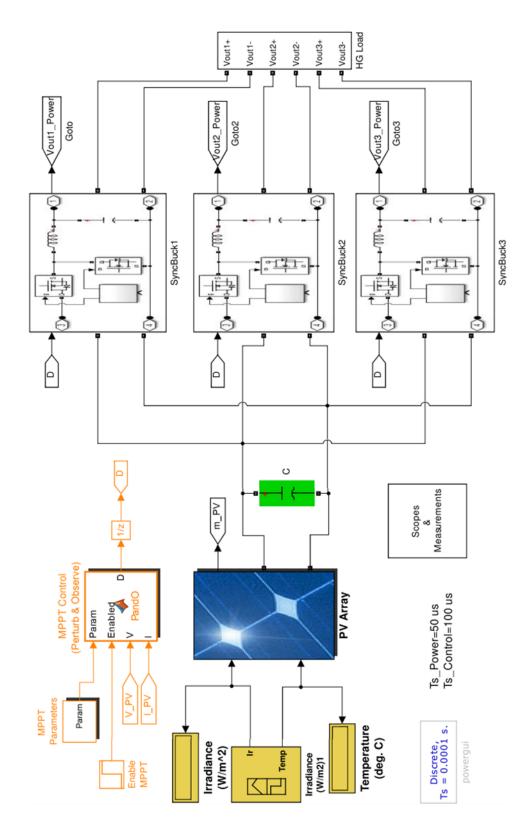


Figure 26 Main Simulink PV system model

The whole mode is broken down into subsections, which will be explained individually. The first section is the PV array input parameters as seen in Figure 27.

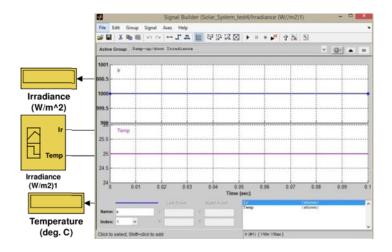


Figure 27 Signal builder blocks for irradiance and temperature

The signal builder will provide the PV array with the irradiance and temperature input. Figure 29, the MPPT section, is not in the form of physical components but in the form of switches and logic operators. Figure 28 contains the MPPT algorithm subsystem.

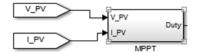


Figure 28 MPPT algorithm subsystem

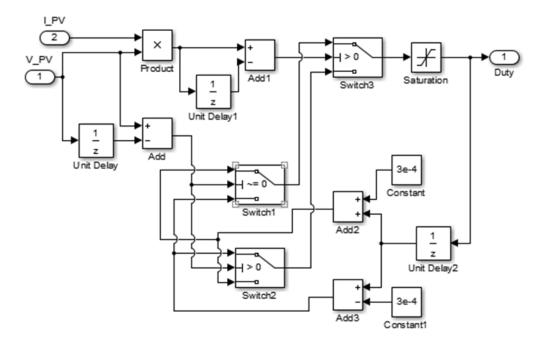


Figure 29 MPPT algorithm logic

Figure 29 shows the P&O MPPT algorithm logic as dictated by Figure 10 in Chapter 2. Figure 30 consists of all the equivalent circuits and mathematics that makes up the PV array. The capacitor acts as an input filter for the synchronous buck converters. The flag m\_PV consists of output parameters from the PV array model. Figures 30, 31 and 32 are what make up the bulk of the PV array. All the parameters that specify the behaviour of the PV array are entered into these models.

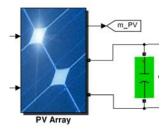


Figure 30 PV array subsystem

The PV module used in the simulation is a Kyocera KD205GX-LP. All the necessary parameters and values for the simulation are gathered from the datasheet as seen in Annexure A.

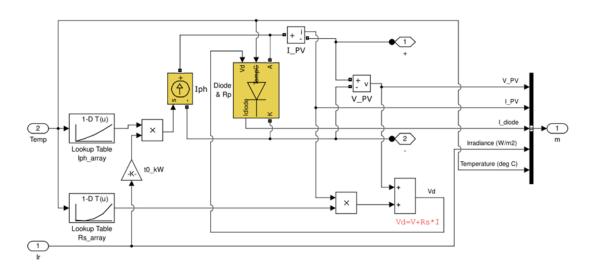


Figure 31 PV array model

Figure 31 is the PV array model, which holds parameter values gathered from the datasheet of the PV panel used. Figure 32 contains the mathematics relating to the diode model of the PV panel. The diode equation in Figure 32 is provided by the Matlab software help file.

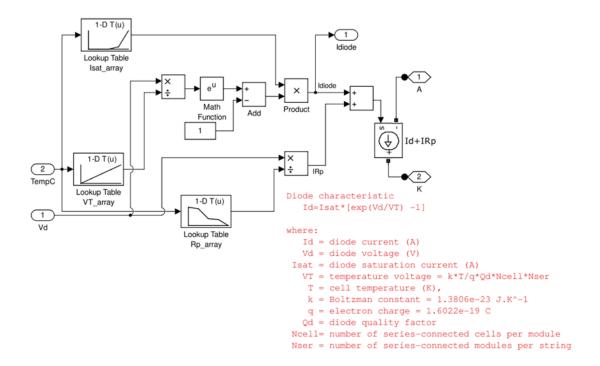


Figure 32 Diode and R<sub>p</sub> model

Figure 33 shows the characteristic curves of one PV panel.

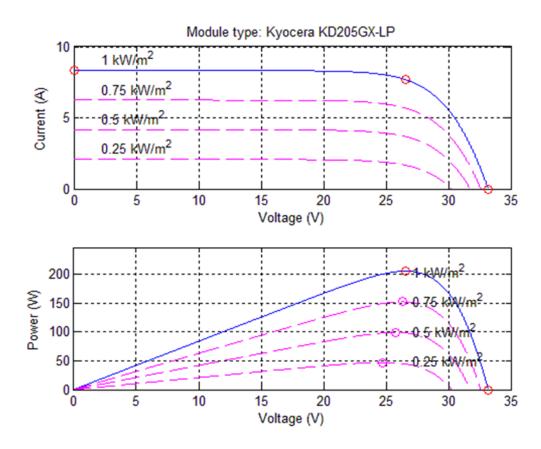


Figure 33 I-V and P-V characteristics of one module at 25°C

Figure 34 represents the synchronous buck converter subsystem. The structures of all three converters look the same except for the values used for the components. The flag D is the duty cycle input to the converter from the MPPT subsystem. Figure 35 shows the design of the converters in more detail.

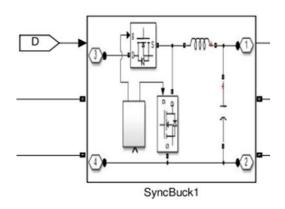


Figure 34 Synchronous buck converter subsystem block

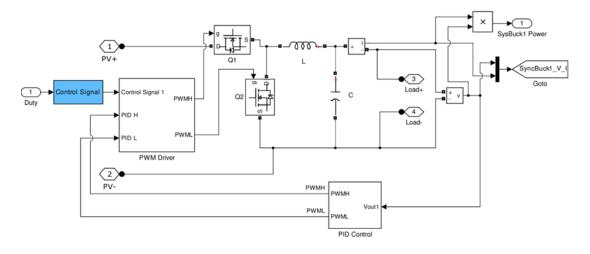


Figure 35 Synchronous buck converter subsystem detailed

The design consists of a PWM driver circuit, PID control and the components that make up a synchronous buck converter. Figure 36 consists of three resistors that will act as the load. The resistor values are set to the values that will simulate the inputs of the HG. The values of the resistors are the following:

• R1: 2,875  $\Omega$ 

• R2:  $0.5 \Omega$ 

• R3:  $0,375 \Omega$ 

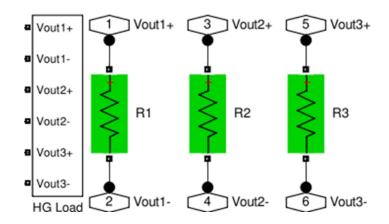


Figure 36 HG subsystem

The system is simulated only for 0.1s with a sample time of 100µs. The reason for this is that this is a complex system and the time it takes to simulate 0.1s in real-time is about one minute. Even though the simulation time is short, the full functionality of the system is simulated and results are obtained.

#### 3.6 Simulation measurements

The simulation of the model is repeated multiple times in order to evaluate the performance of the system. The results obtained are that of an ideal system with ideal component parameters. That being the case, the performance evaluation still illustrates how the system will respond in a practical setting. The simulation focuses on how many PV panels will be needed in order for the SMPS to supply the required output values to the HG according to the specifications given in Table 1 of Chapter 1. The simulation will also indicate what the minimum output power of the PV array should be in order for the SMPS to supply the correct output values.

Table 10 HOGEN® GC 300 power supply output voltages

Output	Voltage (V)	Current (A)	Power (P)
Output 1	7,5	20	150
Output 2	12	4,2	50
Output 3	5	10	50

First, it has to be established what the minimum number of PV panels should be for the system to operate properly. Thus, multiple repetitions at standard test conditions (STC) of the simulation are run in order to establish the minimum number of PV panels needed. The STC are 1000 W/m<sup>2</sup> irradiance and 25°C temperature. To see if

the SMPS is operating normally with the PV array, the total output power of the SMPS is observed.

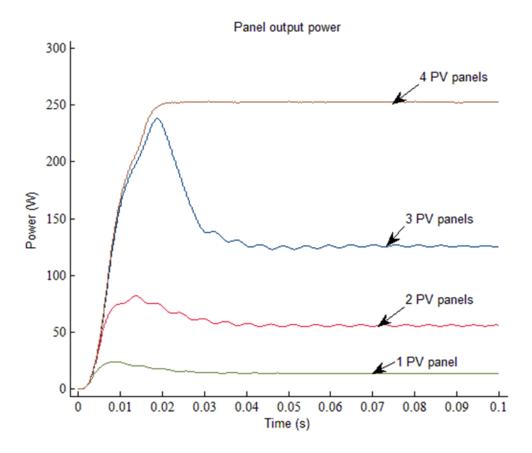


Figure 37 Number of PV panels needed for operation

The panels are connected in a parallel connection because a buck topology is used in the SMPS the voltage from the PV array must not be higher than needed otherwise the duty cycle will suffer and the SMPS will not be able to handle that low a duty cycle. The parallel connections will increase the current output from the PV array, which is more suited to this type of SMPS.

With the minimum number of PV panels established that are required in the array, the PV characteristic curves of the array can be simulated as indicated in Figure 38. When the irradiance decreases so will the output power of the PV array, therefore, it is necessary to determine the minimum irradiance at which the system will still be operational. Thus, starting the irradiance with  $1000 \text{ W/m}^2$  and then decrementing the irradiance with  $100 \text{ W/m}^2$  steps until the point where the PSU stops working, will indicate the estimated range.

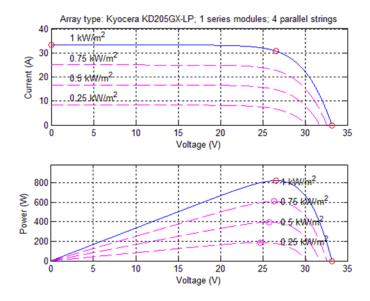


Figure 38 PV array characteristic curves

The process will be repeated, starting at  $700 \text{ W/m}^2$  and incrementing the irradiance with  $20 \text{ W/m}^2$  steps until the PSU is operational again. The process is repeated for the last time starting from  $760 \text{ W/m}^2$  and decrementing in  $1 \text{ W/m}^2$  steps. From the repetition of the above process, it is observed that the minimum irradiance required for the PSU to operate is  $756 \text{ W/m}^2$ . Figures 39-41 show the results for the process followed.

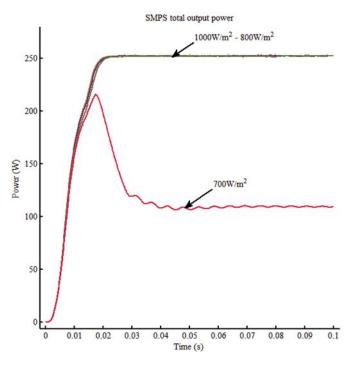


Figure 39 SMPS output power for the irradiance range of 700 W/m<sup>2</sup> - 1000 W/m<sup>2</sup>

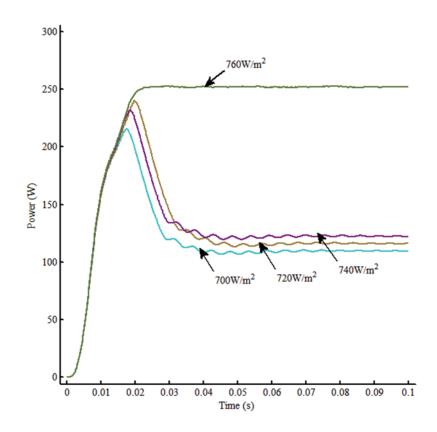


Figure 40 SMPS output power for the irradiance range of 700  $\mbox{W/m}^2$  - 760  $\mbox{W/m}^2$ 

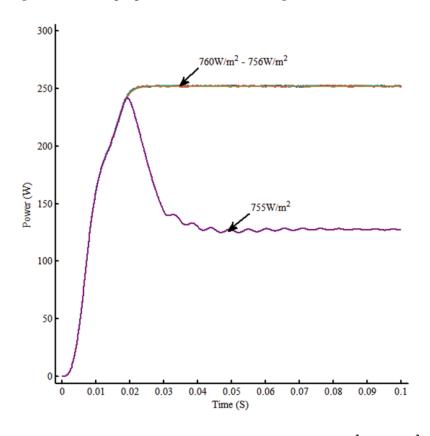


Figure 41 SMPS output power for the irradiance range of 755  $\ensuremath{W/m^2}$  - 760  $\ensuremath{W/m^2}$ 

After establishing the minimum irradiance level, the efficiency of the system can be measured. Setting the irradiance to the minimum, the PV array power is measured as indicated in Figure 42.

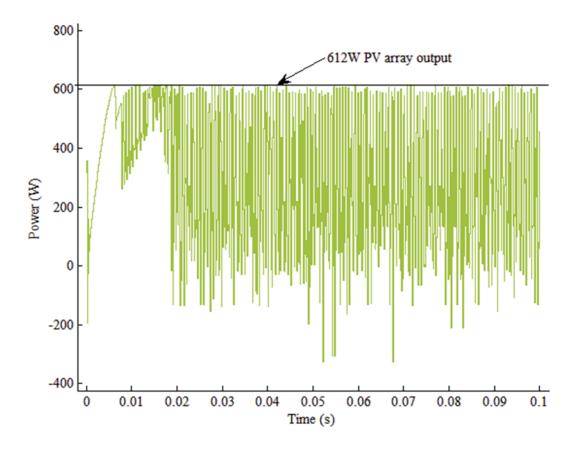


Figure 42 PC V array output power at minimum irradiance setting

The SMPS has a total output power of 250 W. With the PV array, output power of 612 W at a minimum irradiance setting the efficiency of the system is as follows:

$$eff = \frac{\text{SMPS power out}}{\text{PV array power out}} \times 100\%$$

$$= 40,84\%$$
(18)

When the system is operating normally between the irradiance range of 756 W/m<sup>2</sup> and 1000 W/m<sup>2</sup> the behaviour of the DC-DC SMPS when in operation will look like Figures 44-46. It can also be clearly seen in these figures where the start-up begins and ends as well as when the steady-state operation begins. The PID algorithm ensures a fast start-up with a quick transition to the steady-state operation of the DC-DC SMPS.

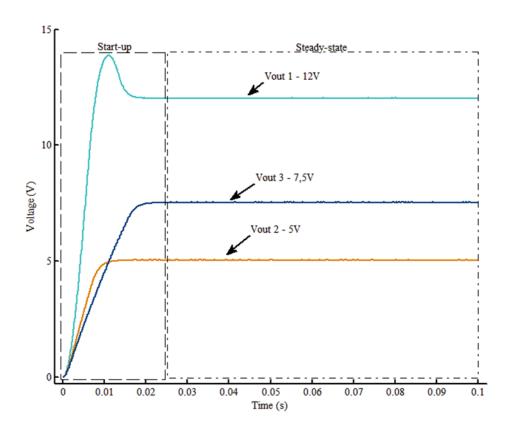


Figure 43 SMPS voltage output while in operation

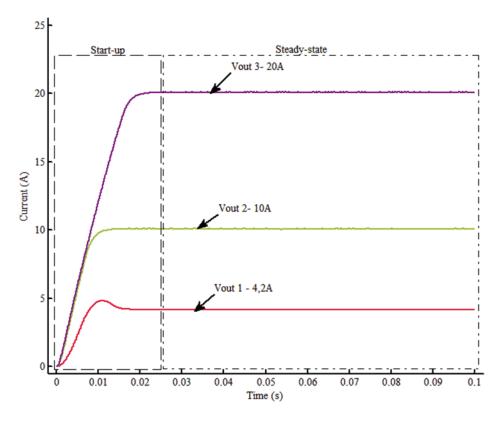


Figure 44 SMPS current output while in operation

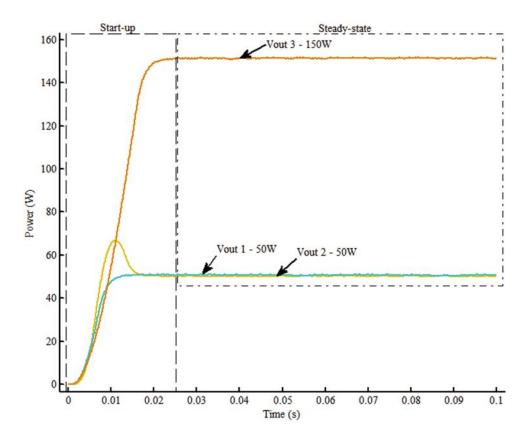


Figure 45 SMPS power output while in operation

#### 3.7 Summary

This chapter discussed the design of the controller, synchronous buck converters and sensing circuits where designed and implemented. Each section was discussed and explained how they function in the system. The parameters chosen were used in the calculations in order to find component values for the circuits. In addition, it was shown how the simulation model was set up and configured. The results obtained indicated how many PV panels where needed in the array for the system to operate. The results also indicated the irradiance range for which the system will operate normally. From the results, the efficiency of the system could be calculated.

Next, is the comparison of the results from the simulation to that of the DC-DC SMPS in a practical setup.

#### CHAPTER 4 MEASUREMENTS AND RESULTS

#### Introduction

This chapter gives an overview of practical results as well as additional results obtained from the simulation. The simulation and practical results were compared in order to make a conclusion.

#### 4.1 Simulation results

Additional simulations were carried out on the system by using different PV panels in the system. These results are important as to the functionality of the system. Table 10 outlines the parameter values of different PV panel models. The PV panels are connected in parallel in order to increase the current output of the PV array and not the voltage output. As indicated in Chapter 3, four PV panels are needed in order for the system to operate. Thus increasing the PV panel amount the current and power increases but not the voltage. The simulation was repeated multiple times with the irradiance set to 1000 W/m², and selecting a PV panel model as well as the number of PV panels used.

As seen in Table 11, the system only operates with four panels for any PV panel model except for the last PV panel model. After establishing the minimum amount of PV panels needed, the irradiance is lowered in order to find the minimum irradiance level at which the system will still operate for each PV model selection. Table 12 lists the results obtained. By inspecting Table 12, it will be noticed that the minimum PV array output current is not lower than 20,27 A with its respective minimum irradiance level. The efficiency of the system is also very low and can be contributed to the values of I<sub>MPP</sub> in Table 12. Even though all the converters are synchronous buck converters, which should step-up the current from a very low current value, it does not. The reason for this can be that the total amount of current drawn by the HG is 35 A as indicated in Table 1. Thus, the minimum amount of current needed to step-up from is very high. The system efficiency suffers because of this issue. It can be concluded that the power rating as well as the voltage rating is not that important when choosing a PV panel for this system but rather the current rating. The voltage should be at least 15 V in order to correctly step-down to 12 V, 5 V and 7,5 V, but

also the power should be no less than 250 W because the HG requires 250 W. Thus, when constructing the PV array the output current of the array should not be lower than 20,27A. The last PV panel does not have results because the system only starts operating when 15 panels are connected in parallel. Therefore, even though the voltage is very high and the power rating at four panels are correct, the current is too low for the DC-DC SMPS to properly step-up the current and operate.

Table 11 Simulation results for different PV panels

	No. panels	Voc	$I_{SC}$	V <sub>MPP</sub>	$I_{MPP}$	P <sub>MPP</sub>
	1 Panel	22,10	8,37	17,70	7,63	135,04
Kyocera KD135GX-	2 Panels	22,10	16,74	17,70	15,26	270,09
LP	3 Panels	22,10	25,11	17,70	22,89	405,13
	4 Panels	22,10	33,48	17,70	30,52	540,17
	1 Panel	33,20	8,36	26,60	7,71	205,08
Kyocera KD205GX-	2 Panels	33,20	16,72	26,60	15,42	410,15
LP	3 Panels	33,20	25,08	26,60	23,13	615,23
	4 Panels	33,20	33,44	26,60	30,84	820,30
	1 Panel	30,80	8,23	24,70	7,71	190,50
Mitsubishi PV-	2 Panels	30,80	16,47	24,70	15,43	381,01
UD190MF5	3 Panels	30,80	24,70	24,70	23,14	571,51
	4 Panels	30,80	32,93	24,70	30,85	762,01
	1 Panel	41,80	7,13	33,90	6,63	224,90
Sanyo HIP-	2 Panels	41,80	14,27	33,90	13,27	449,80
225HDE1	3 Panels	41,80	21,40	33,90	19,90	674,70
	4 Panels	41,80	28,54	33,90	26,54	899,60
	1 Panel	30,60	8,51	24,30	7,83	190,26
BP Solar SX3190	2 Panels	30,60	17,02	24,30	15,66	380,52
Dr Solai SA3190	3 Panels	30,60	25,53	24,30	23,49	570,77
	4 Panels	30,60	34,04	24,30	31,32	761,03
	1 Panel	94,57	1,18	70,56	1,01	71,33
First Solar FS-272	2 Panels	94,57	2,36	70,56	2,02	142,65
1 II St Solai 1 3-272	3 Panels	94,57	7,09	70,56	3,03	213,98
	4 Panels	94,57	2,36	70,56	4,04	285,30

Table 12 DC-DC SMPS running at 1000  $\mbox{W/m}^2$ 

	1 Pa	nel	2 Par	nels	3 Par	nels	4 Pai	nels
	YES	NO	YES	NO	YES	NO	YES	NO
Kyocera KD135GX-LP		X		X		X	X	
Kyocera KD205GX-LP		X		X		X	X	
Mitsubishi PV- UD190MF5		X		X		X	X	
Sanyo HIP- 225HDE1		X		X		X	X	
BP Solar SX3190		X		X		X	X	
First Solar FS- 272		X		X		X		X

Table 13 DC-DC SMPS running for various irradiances with four PV panels

	Irradiance (W/m²)	Irradiance in %	V <sub>MPP</sub>	$I_{MPP}$	P <sub>MPP</sub>	Efficiency (%)
Kyocera KD135GX-LP	860	86,00%	17,70	26,25	464,55	53,82%
Kyocera KD205GX-LP	728	72,80%	26,60	22,45	597,18	41,86%
Mitsubishi PV- UD190MF5	750	75,00%	24,70	23,14	571,51	43,74%
Sanyo HIP- 225HDE1	764	76,40%	33,90	20,27	687,29	36,37%
BP Solar SX3190	736	73,60%	24,30	23,05	560,12	44,63%
First Solar FS- 272	n/r	n/r	n/r	n/r	n/r	n/r

When carrying out the practical setup, the PV panels used must meet the requirements established above.

## 4.2 Experimental setup

The experimental setup was connected as indicated in Figure 46 below.

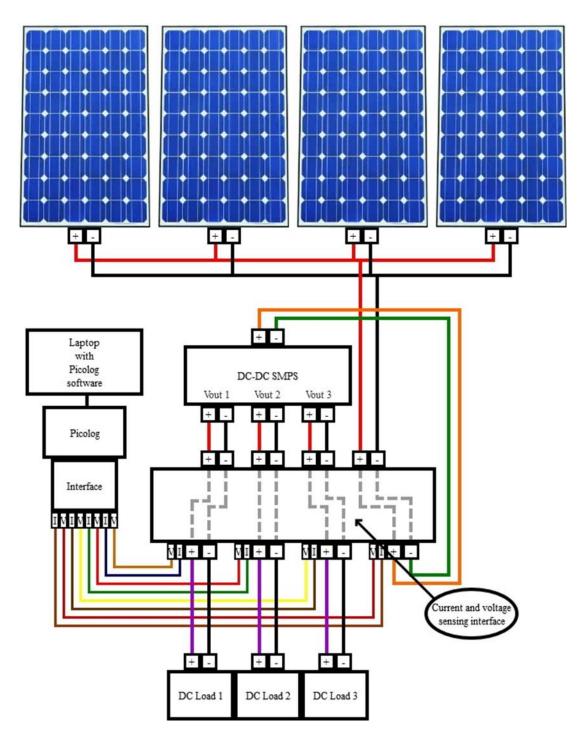


Figure 46 Experimental setup

The PV array as well as the outputs of the DC-DC SMPS is connected to the current and voltage-sensing interface (I&V interface) input connectors. This will allow for

current and voltage measurements as well as logging these measurements with the Picolog hardware. The output of the I&V interface is connected to DC loads that together act as the HG load. The V and I connecters on the I&V interface are connected to another interface connected to the Picolog. The PV array output from the I&V interface is then connected to the input of the DC-DC SMPS. The system is now a closed-loop system. The PV panel chosen for the practical is the Sunmodule SW 220 poly (see Annexure A) because they are the panels that are used by the Telkom Centre of Excellence for all research purposes. The PV panels meet the requirements as mentioned previously. The DC loads are set to the values so as to act as the HG load.

The irradiance and temperature parameters could not be kept constant as in the simulation environment but the results obtained where nonetheless acceptable.

#### 4.3 Measurement results

Figure 47 shows the PV array power of the system for a time period during testing. During this time period, the system was running multiple times. An average of the results was calculated and the data was plotted in Figures 48-50. Figure 48 is the output voltage of the DC-DC SMPS. It can be seen that the form of the graphs are the same as that of the simulation. The voltage outputs are slightly higher than the preferred 12V, 5V and 7,5V and fluctuate more often. The only major difference is the time period for which the system was operating. The DC-DC SMPS takes a bit longer than the simulation to reach a steady-state. The reason for this is that there are delays from the PCB itself, for instance capacitors that need to be charged and discharged. In addition, the speed of the MCU needs to be taken into account.

Figure 39 shows the current waveforms. Again, the shapes of the waveforms are the same as that of the simulation waveform but with slightly lower values than the preferred 20A, 10A and 4,2A. With real components, there will be differences to that of the simulation because the simulation uses ideal components. That is why the output of the DC-DC SMPS is not exactly the same as that of the simulation. The current output is also a bit lower than expected but still within an acceptable operating range. Figure 40 is the power output of the DC-DC SMPS. Because the

voltage and current is a bit lower than expected the output power is also a little lower but still acceptable.

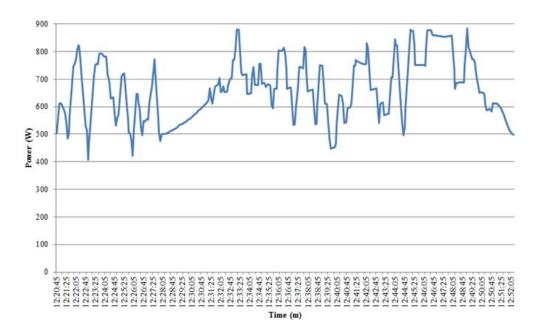
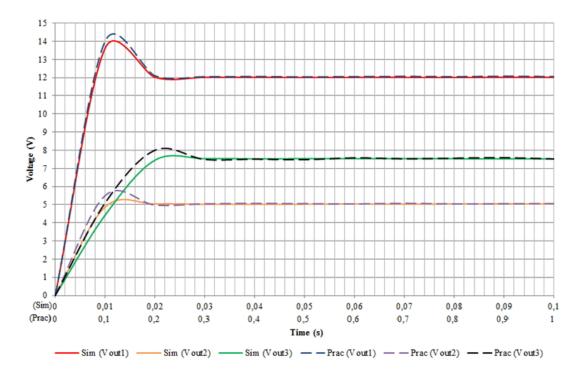


Figure 47 Practical PV array power

The average power is around 660 W. Thus, with the output power around 250 W the total efficiency of the system is 38%. The efficiency is lower than expected.



 $Figure\ 48\ Simulation\ and\ practical\ results\ compared\ for\ output\ voltage$ 

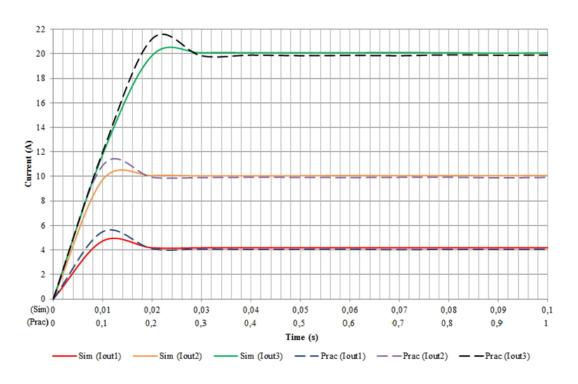


Figure 49 Simulation and practical results compared for output current

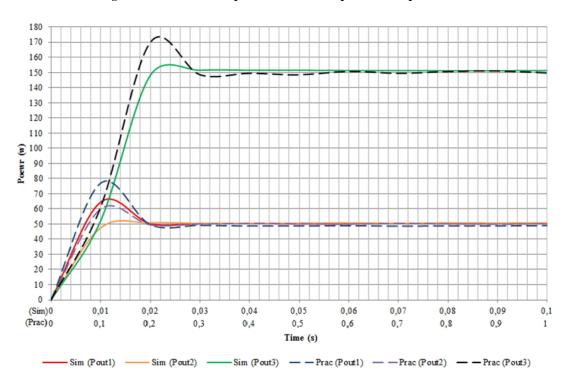


Figure 50 Simulation and practical results compared for output power

The output power for practical  $P_{\text{out3}}$  in Figure 50 is more unstable than the rest of the output power. It can be reasoned that the DC-DC SMPS has more difficulty at such a high output power than for the rest.

### 4.4 Summary

In this chapter, the system was tested and measured in a practical environment. The results obtained were compared to that of the simulation results. The results showed that the DC-DC SMPS in a practical setup has the same waveforms as the simulation but with a different time period as well as different output values.

Chapter 5 is the final section in this dissertation. It will contain the conclusions made from the research as well as recommendations for further research on the DC-DC SMPS.

#### CHAPTER 5 CONCLUSIONS AND RECOMMENDATIONS

#### Introduction

The aim was to design a solar driven (PV) power supply unit for a regenerative fuel cell hydrogen generator. The conclusions have been made based on the results obtained. The recommendations for future research will also be discussed.

#### **5.1 Conclusions**

It was found that PV energy is an important alternative energy source. By combining PV energy with a hydrogen generator, an independent solar/hydrogen system can be constructed. However, in order for the hydrogen generator to operate from PV energy a power supply unit had to be designed according to the hydrogen generator specifications. In addition, to make sure the PV panels operate at their own maximum efficiency a MPPT algorithm has to be implemented into the power supply unit.

#### 5.1.1 Design and simulation

Research into different MPPT algorithms revealed that the perturb and observe algorithm will be the best option for the design of the DC-DC SMPS. The P&O algorithm was chosen because it is easy to implement and has a reputation for being able to track the MPP with very high efficiency. The other advantage of the P&O algorithm is that it can be programmed onto a MCU instead of being hardware based. This makes it easier to modify the algorithm as needed and is faster than that of hardware based algorithms.

The voltage and current requirements of the hydrogen generator showed that a buck converter topology was needed for the design of the DC-DC SMPS. Therefore, further research was done in order to optimise the design to fit the system. It was found that a synchronous buck converter topology was the improved version of the normal buck converter topology, meaning that the efficiency is higher. The research also indicated that to stabilise the output of the DC-DC SMPS, a control method was needed. It was found that the voltage-mode control along with a PID controller was needed to best stabilise the output of the DC-DC SMPS. The voltage-mode control

will try to correct the output voltage to that which is required. On its own, the voltage-mode control cannot be used and, therefore, the PID controller was used in conjunction with the voltage-mode control. The PID controller will minimise the error of the output and the output will be more stable and more accurate. The PID controller makes very fast adjustments because it is programmed onto the MCU. The voltage-mode control is hardware based.

After designing the DC-DC SMPS, the whole system was simulated. The reason for simulation is to be able to observe the system behaviour before manufacturing. The simulation helped by indicating how many PV panels are needed in the array in order for the DC-DC SMPS to operate normally. The simulation results also clarified a very important aspect of the design, which is how big a role the current of the PV panels play in the choosing of the PV panels. The simulation showed that the current of the PV array cannot be lower than 20,27A. If the current is lower than this value the DC-DC SMPS will not operate. With this indication, the system efficiency is very much lower and not desirable. The power has to be more than 250 W because that is what is required from the hydrogen generator. The voltage has to be more than 15V for the synchronous buck converter to correctly step-down the voltage. The simulation, however, does not indicate how the system will behave in a practical environment.

#### **5.1.2** Practical environment

The practical environment gives precedence to factors not included in the theory or simulation. The PCB was designed and manufactured keeping in mind how much current will be conducted along the PCB tracks. The results obtained showed that both the output current and voltage was slightly lower than that of the simulation but still within the tolerance range. There was a slight delay in the response of the system but that is because of the real components used on the PCB and the processing speed of the MCU. It was also observed and noted that the mosfet driver and mosfets got very hot after only a few seconds of operation and made the system unstable afterwards. The efficiency of the system, which is at 38%, is also lower than that of the simulation efficiency, which is 40%.

#### **5.2 Recommendations**

The following recommendations regarding further research of the hydrogen generator DC-DC SMPS are made:

- Further research needs to be done to improve the MPPT algorithm and optimise it so that it will be able to track the MPP successfully when there is partial shading.
- Further research needs to be done to improve the converter efficiency and be able to work with a lower current input from the PV array.
- The simulation needs to be optimised with components that better reflect their real world counterparts instead of ideal components in order to more accurately simulate the system.
- The PCB needs to be redesigned with fans included to be able to dissipate the heat from the components so that the components do not overheat.

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## ANNEXURE INDEX

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- Quick and easy to install dramatically reduces installation time
- Lower system costs can cut rooftop installation costs in half
- Aesthetic seamless appearance low profile with auto leveling and alignment
- Built-in hyper-bonded grounding system if it's mounted, it's grounded
- · Theft resistant hardware
- Ultra-low parts count 3 parts for the mounting and grounding system
- 6 years product warranty (materials and workmanship); 25 years module power output warranty
- Industry leading PLUS ONLY power tolerance: +5W (+2.0%)
- Backward compatibility with all standard rooftop and ground mounting systems





# NewEdge CS6P

220/225/230/235/240/245/250PX

Preliminary Version

#### **Next Generation Solar Module**

NewEdge, the next generation module designed for multiple types of mounting systems, offers customers the added value of minimal system costs, aesthetic seamless appearance, auto grounding and theft resistance.

The CS6P-PX is a robust 60 cell solar module incorporating the groundbreaking Zep Compatible frame. The specially designed frame allows for rail-free, fast installation with the industry's most reliable grounding system. The CS6P-PX is the perfect choice for customers who are looking for a high quality, aesthetic module with the lowest system costs.

#### **Applications**

- · On-grid residential roof-tops
- On-grid commercial/industrial roof-tops
- Solar power stations
- Other on-grid applications

#### **Quality Certificates**

- UL 1703(pending), CE
- ISO9001:2008: Standards for quality management systems
- ISO/TS16949:2009: The automotive quality management system
   QC080000 HSPM: The Certification for
- QC080000 HSPM: The Certification for Hazardous Substances Regulations



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#### CS6P-220/225/230/235/240/245/250PX

#### **Electrical Data**

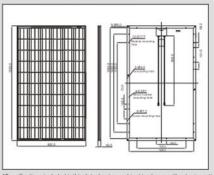
Electrical Data		CS6P-220PX	CS6P-225PX	CS6P-230PX	CS6P-235PX	CS6P-240PX	CS6P-245PX	CS6P-250PX
Nominal Maximum Power at	lominal Maximum Power at STC (Pmax)		225W	230W	235W	240W	245W	250W
Optimum Operating Voltage	Optimum Operating Voltage (Vmp)		29.4V	29.6V	29.8V	29.9V	30.0V	30.1V
<b>Optimum Operating Current</b>	(Imp)	7.53A	7.65A	7.78A	7.90A	8.03A	8.17A	8.30A
Open Circuit Voltage (Voc)	7.07	36.6V	36.7V	36.8V	36.9V	37.0V	37.1V	37.2V
Short Circuit Current (Isc)		8.09A	8.19A	8.34A	8.46A	8.59A	8.74A	8.87A
Operating Temperature		-40℃~+85℃						
Maximum System Voltage					600V (UL)			
Maximum Series Fuse Rating	)				15A			
Power Tolerance					+5W			
	Pmax				-0.43%/C			
Temperature Coefficient	Voc	-0.34 %/C						
remperature coefficient	Isc				0.065 %/C			
	NOCT		45°C					

<sup>\*</sup>Under Standard Test Conditions (STC) of irradiance of 1000W/m, spectrum AM 1.5 and cell temperature of 250

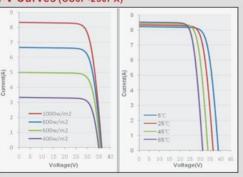
#### **Mechanical Data**

Cell Type	Poly-crystalline
Cell Arrangement	60 (6 x 10)
Dimensions	1638 x 982 x 40mm (64.5 x 38.7 x 1.57in)
Weight	20kg (44.1 lbs)
Front Cover	Tempered glass
Frame Material	Anodized aluminium alloy
Standard Packaging (Modules per Pallet)	20pcs

#### **Engineering Drawings**



#### I-V Curves (CS6P-250PX)



cifications included in this datasheet are subject to change without prior

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Canadian Solar Inc. is one of the world's largest solar companies. As a leading vertically-integrated manufacturer of ingots, wafers, cells, solar modules and solar systems. Canadian Solar delivers solar power was 325.5 MWwith a module capacity of 820MW.

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Headquarters | 650 Riverbend Drive, Suite B Kitchener, Ontario | Canada N2K3S2 Tel; +1-519-954-2057 Fax: +1-519-954-2597 inquire. ca@canadiansolar.com www.canadiansolar.com

# SHARP

solar electricity

# **235 WATT**

RESIDENTIAL MODULE





ND-F2Q235 SunSnap

RESIDENTIAL 235 WATT SUNSNAP™ MODULE FROM THE WORLD'S TRUSTED SOURCE FOR SOLAR.

The 235 Watt SunSnap™ module is the power generating component of the new SunSnap™ solar appliance. This powerful residential module is the perfect combination of high performance and design. Sharp's robust Zep Compatible frame design enables rail-free mounting, drastically reducing installation hassles. Everything from the positioning, to the mounting, to the wiring has been streamlined and simplified, so it all comes together quickly and easily, substantially reducing labor costs. Versatile enough to permit installation on nearly any kind of roof, the 235 Watt SunSnap™ module is the newest innovation in Sharp's residential product offerings.

The next evolution in frame design makes installation a snap, literally....

#### NO NEED FOR MOUNTING RAILS

With a series of drop-in and quarter-turn connections, the 235 Watt SunSnap™ module installs faster than conventional modules. The robust Zep Compatible frame avoids the need for mounting rails and enables theft resistant, auto grounding connections.

#### ADVANCED AESTHETICS

Sleek, black frame and matching black backskin provides an elegant appearance that blends beautifully with your home's roofline.

#### POSITIVE POWER TOLERANCE

Count on Sharp to deliver all the watts you pay for with a positive only power tolerance of +5% (+11.75 W).

#### RELIABLE

The 235 Watt SunSnap™ module is covered by both the Sharp 10-year limited warranty on materials o workmanship as well as the 25-year limited warranty on power output.

#### "BUY AMERICAN"

Designed in Camas, WA and manufactured in Memphis, TN from imported and domestic parts.





#### SHARP: THE NAME TO TRUST

When you choose Sharp, you get more than well engineered products. You also get Sharp's proven reliability, outstanding customer service and the assurance of both our 10-year limited warranty on materials or workmanship as well as the 25-year limited warranty on power output. With over 50 years experience in solar and over 4.3 GW of installed capacity, Sharp has a proven legacy as a trusted name in solar.

BECOME POWERFUL

# **235 WATT**

#### ND-F20235

Module output cables: 12 AWG PV Wire (per UL Subject 4703)

Maximum Power (Pmax)*	235 W
Tolerance of Pmax	+5%/-0%
Type of Cell	Polycrystalline silicon
Cell Configuration	60 in series
Open Circuit Voltage (Voc)	37.4 V
Maximum Power Voltage (Vpm)	29.2 V
Short Circuit Current (Isc)	8.59 A
Maximum Power Current (Ipm)	8.05 A
Module Efficiency (%)	14.4%
Maximum System (DC) Voltage	600 V
Series Fuse Rating	15 A
NOCT	47.5°C
Temperature Coefficient (Pmax)	-0.485%/°C
Temperature Coefficient (Voc)	-0.351%/°C
Temperature Coefficient (Isc)	0.053%/°C

"illumination of 1 kW/m" (1 sun) at spectral distribution of AM 1,5 (ASTM E892 global spectral irradiance) at a cell temperature of 25°C.

#### MECHANICAL CHARACTERISTICS

"Intertex recognized for mating with MC-4 connectors (part numbers PV-KST4; PV-KBT4

#### QUALIFICATIONS

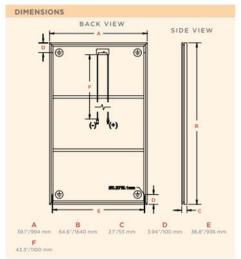
UL Listed UL 1703
Fire Rating Class C

#### WARRANTY

25-year limited warranty on power output Contact Sharp for complete warranty information

Design and specifications are subject to change without notice. Sharp is a registered trademark of Sharp Corporation. All other trademarks are property of their respective owners.





Contact Sharp for tolerance specifications

#### ISO QUALITY & ENVIRONMENTAL MANAGEMENT

Sharp solar modules are manufactured in ISO 9001:2000 and ISO 14001:2004 certified facilities.

#### "BUY AMERICAN"

Sharp solar modules are manufactured in the United States and Japan, and qualify as "American" goods under the "Buy American" clause of the American Recovery and Reinvestment Act (ARRA).









SHARP ELECTRONICS CORPORATION
5700 NW Pacific Rim Boulevard, Camas, WA 98607
1-800-SOLAR-06 • Email: sharpsolar@sharpusa.com

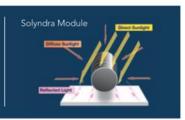
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12F-107 • PC-06-12



Solar photovoltaic systems comprised of panels and mounting hardware for low slope, commercial rooftops.

Proprietary cylindrical modules optimize the collection of sunlight and enable Solyndra panels to achieve the highest rooftop coverage without the need for costly mounting hardware or rooftop penetrations. By significantly reducing installation costs and increasing the electricity generated per rooftop, Solyndra delivers electricity at low cost per kilowatt hour.





# **Product Specifications**



#### **Electrical Data**

Measured at Standard Test Conditions (STC) irradiance of 1000 W/m², air mass 1.5, and cell temperature 25° C

Model Number		SL-001-150	SL-001-157	SL-001-165	SL-001-173	SL-001-182	SL-001-191	SL-001-200 Release Date TBD
PowerRating (Pso)	Wp	150 Wp	157 Wp	165 Wp	173 Wp	182 Wp	191 Wp	200 Wp
Power Tolerance (%)	%/Wp	+4, -5	+/-4	+/-4	+/-4	+/-4	+/-4	+/-4
V <sub>mp</sub> (Voltage at Maximum Power)	Volts	65.7 V	67.5 V	69.6 V	71.7 V	73.9 V	76.1 V	78.3 V
Imp (Current at Maximum Power)	Amps	2.28 A	2.33 A	2.37 A	2.41 A	2.46 A	2.51 A	2.55 A
Voc (Open Circuit Voltage)	Volts	91.4 V	92.5 V	93.9 V	95.2 V	96.7 V	98.2 V	99.7 V
Isc (Short Ciruit Current)	Amps	2.72 A	2.73 A	2.74 A	2.75 A	2.76 A	2.77 A	2.78 A
Temp. Coefficient of V∞	%/°C				29			
Temp. Coefficient of Isc	%/°C				02			
Temp. Coefficient of Power	%/°C				38			

# System Information

Cell type	Cylindrical CIGS
Maximum System Voltage	Universal design: 1000V (IEC) & 600V (UL) system:
Dimensions	Panel: 1.82 m x 1.08 m x 0.05 m Height: 0.3 m to top of panel on mounts
Mounts	Non-penetrating, powder-coated Aluminum
Connectors	4 Tyco Solarlok; 0.20 m cable
Series Fuse Rating	23 Amps
Roof Load	16 kg/m² (3.3 lb/ft²) panel and mounts
Panel Weight	31 kg (68 lb) without mounts
Snow Load Maximum	2,400 Pa (50.1 lb/ft²)
Hailstone Impact	25 mm, 7.53 g at 23 m/s per IEC 61646
Wind Performance	208 km/h (130 mph) maximum Self-ballasting with no attachments
Operating and Storage Temp	-40°C to +85°C
Normal Operating Cell Temperature (NOCT)	41.7°C at 800 W/m², Temp = 20°C, Wind = 1m/s
Certifications/Listings	UL1703, IEC 61646, CEC listing IEC 61730, CE Mark, Fire Class C Application Class A per IEC 61730-2
Warranty	25 year limited power warranty 5 year limited product warranty



Solyndra's panels come with all of the mounts, grounding connectors, lateral clips, and fasteners required to build a standard array.

Solyndra, Inc. 47700 Kato Road Fremont, CA www.solyndra.com



Specifications subject to change without notice. Specification is only valid when using the product in accordance with

© 2010 SOLYNDRIA, INC. ALL RIGHTS RESERVED CAUTION, READ SAFETY AND INSTALLATION INSTRUCTIONS BEFORE USING THE PRODUCT.

Revision: 7 / Released: 06/02/10

# Wherever there is SUN, there is **SUNGEN**



## SG-HN-GG Series 95W/100W/105W

SUNGEN Amorphous Silicon Solar Modules

#### **Product Features**

- High performance and energy yield photovoltaic modules made of amorphous silicon
- Integrated bypass diode in the junction box reduces the power loss effect in a string caused by events such as shading
- PVB film with high quality TCO glass
- Module is glass to glass laminated
- Water-protected connector system
- Easy for installation

#### **Quality and Safety**

- Product warranty: Free from defects in material and workmanship for 10 years
- Power warranty: Maintain more than 90% minimum rated power for 10 years and 80% minimum rated power for 25 years
- EN/IEC 61646 certified
- EN/IEC 61730 certified
- UL1703 certified

### **Applications**

- On-grid PV Systems
- Off-grid PV Systems
- Residential Roof Top Systems
- Commercial Roof Top Systems
- Ground Installations

ase read the SUNGEN installation guide book for the step-by-step installation guidelines.)



PV CYCLE ERGO

(Tii√) c(U)us (€





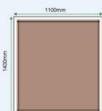


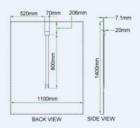




#### SG-HN-GG Series 95W/100W/105W

#### SUNGEN Amorphous Silicon Solar Modules



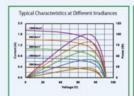


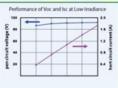
## **Specifications**

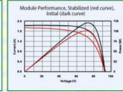
Model	SG-HN95-GG	SG-HN100-GG	SG-HN105-GG			
Maximum power (Pmax)	95W	100W	105W			
Open- circuit voltage (Voc)	92.0V	92.0V	92.5V			
Short- circuit current (Isc)	1.67A	1.74A	1.81A			
Voltage at maximum power (Vpmax)	70.0V	70.5V	71.0V			
Current at maximum power (Ipmax)	1.35A	1.42A	1.48A			
Temperature coefficient-open circuit voltage (β)		-0.36%/K				
Temperature coefficient-short circuit current (α)	0.13%/K					
Temperature coefficient-power (γ)	-0.268%/K					
Cell	a-Si single junction					
Dimensions	1400mm × 1100mm × 7.1mm (55.1 inches × 43.3 inches × 0.3 inches)					
Weight	26.0Kg (57.3 lbs)					
Frame	None					
Front glass	3.2mm thickness					
Back glass		3.2mm thickness				
Junction box type	٨	Aulti-Contact Type 4 complian	nt			
Maximum system voltage	1000V	DC (TÜV-EN/IEC61646) / 600V	DC(UL)			
Maximum mechanical load	Snow load: 5400Pa	(IEC Standard); Wind load: 24	100Pa(IEC Standard)			
Series fuse rating		3A				
Fire rating		Class C				
Nominal Operating Cell Temperature (NOCT)		40.28°C (104.50°F)				
Operating temperature (cell)	-4	10°C to +85°C (-40°F to +185°	F)			
Storage temperature	-4	10°C to +85°C (-40°F to +185°	(F)			
Storage air humidity		<85% relative humidity				

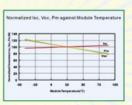
The electrical data applied under standard test conditions (STC): irradiance of 1000 W/m² with an AM1.5 spectrum at a cell temperature of 25°C. The power output is subject to a manufacturing tolerance of  $\pm 3\%$ ; Electrical parameter tolerance  $\pm 10\%$ .

#### Characteristic Curves(SG-HN100-GG)









Design and specifications are subject to change without notice.

#### SUNGEN INTERNATIONAL LIMITED

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WWW.SUNGEN.COM





# Monocrystalline Solar Modules

#### SUNGEN SGM-D Series 185W/190W/195W

#### **Product Features**

- High conversion efficiency photovoltaic modules made of mono-crystalline silicon solar cells.
- Integrated bypass diodes in the junction box reduce the power loss effect in a string caused by events such as shading.
- Module is glass to back sheet laminated.
- Water-protected connector system, easy for installation.

#### **Quality and Safety**

- Power warranty : Maintain more than 90% of minimum rated power for 10 years. Maintain more than 80% minimum rated power for 25 years.
- According to IEC 61215.
- According to IEC 61730.
- According to UL 1703.
- TUV, UL certified.







#### **Brief Information**

- 125mm x 125mm (4.92inches x 4.92inches) mono-crystalline solar cells.
- 72 cells in series (6X12).
- 2,400N/m²(50psf)mechanical load-bearing capacity 245kg/m² (50pounds/foot²).
- ■1000VDC(IEC)/600VDC(UL) maximum system voltage.

### **Applications**

- On-grid PV Systems.
- Off-grid PV Systems.
- Residential Roof Top Systems.
- Commercial Roof Top Systems.
- Ground Installations.

Please read our extensive installation guide carefully prior to installing the photovoltaic modules.

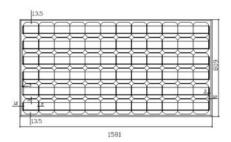


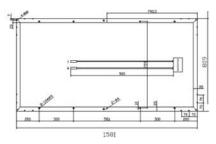


# Monocrystalline Solar Modules









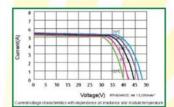
#### Characteristics

Model	SGM-185D	SGM-190D	SGM-195D		
Max-power Voltage (Vmp)	38.6V	38.6V	38.6V		
Max-power Current (Imp)	4.79A	4.92A	5.05A		
Open-circuit Voltage (Voc)	46.1V	46.2V	46.1V		
Short-circuit Current (Isc)	5.27A	5.42A	5.56A		
Max-power (Pm)	185W	190W	195W		
Temperature Coefficient of Pm	-0.4667%/K				
Temperature Coefficient of Voc		-0.345%/K			
Temperature Coefficient of Isc		0.1055%/K			
NOCT		48°C+/-2°C(118.4°F+/-3.6°F)			
Operating Temperature		40°C ~ +85°C(-40°F ~ +185°F	)		
Maximum System Voltage		1000V(IEC)/600V(UL)			

### **Specifications**

Cell	125mm x 125mm (4.92 inches x 4.92 inches)	Dimension of Module	1581mm x 809mm x 40mm (62.24 inches x 31.85 inches x 1.57 inches)
Tolerance	-1%~+3%	Weight	15.5kg (34.16lbs)
No. of Cells	72 (12 x 6)		

#### **Characteristic Curves**



Please note the graphs above will have a tolerance.

SUNGEN International Ltd. March 2010

SUNGEN reserves the rights to modify these specifications and warranties without notice.









# KD205GX-LP

HIGH EFFICIENCY MULTICRYSTAL PHOTOVOLTAIC MODULE



#### HIGHLIGHTS OF

#### KYOCERA PHOTOVOLTAIC MODULES

Kyocera's advanced cell processing technology and automated production facilities produce a highly efficient multicrystal photovoltaic module.

The conversion efficiency of the Kyocera solar cell is over 16%. These cells are encapsulated between a tempered glass cover and a pottant with back sheet to provide efficient protection

from the severest environmental conditions.

The entire laminate is installed in an anodized aluminum frame to provide structural strength and ease of installation. Equipped with plug-in connectors.



#### **APPLICATIONS**

#### KD205GX-LP is ideal for grid tie system applications.

- Residential roof top systems
   Large commercial grid tie systems
- Water Pumping systems
   High Voltage stand alone systems

#### QUALIFICATIONS

MODULE : UL1703 listed

• FACTORY : ISO9001 and ISO 14001

#### **QUALITY ASSURANCE**

Kyocera multicrystal photovoltaic modules have passed the following tests.

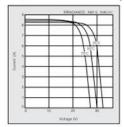
- Thermal cycling test Thermal shock test Thermal / Freezing and high humidity cycling test Electrical isolation test Hail impact test Mechanical, wind and twist loading test Salt mist test Light and water-exposure test Field exposure test

#### LIMITED WARRANTY

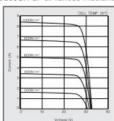
(Long term output warranty half by Module(s) exhibits power output of least than 50% of the original minimum rated power specified at the time of sale within 10 years and leas than 50% within 20 years after the date of sale to the Customer. The power output values shall be those measured under Kyocera's standard measurement conditions. Regarding the warranty conditions in detail, please refer to Valuranty issued by Kyocera's

#### **ELECTRICAL CHARACTERISTICS**

Current-Voltage characteristics of Photovoltaic Module KD205GX-LP at various cell temperatures



Current-Voltage characteristics of Photovoltaic Module KD205GX-LP at various irradiance levels

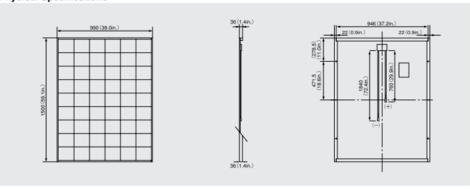


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**SPECIFICATIONS** KD205GX-LP

#### ■ Physical Specifications

Unit : mm (in.)



#### ■ Specifications

Electrical Performance under Standard Test Conditions (*STC)		
205W (+5%/-5%)		
26.6V		
7.71A		
33.2V		
8.36A		
600V		
−0.120 V/°C		
5.02×10 <sup>-3</sup> A/°C		
֡		

Electrical Performance at 800W/m <sup>2</sup> ,*NOCT, AM1.5		
Maximum Power (Pmax)	145W	
Maximum Power Voltage (Vmpp)	23.5V	
Maximum Power Current (Impp)	6.17A	
Open Circuit Voltage (Voc)	29.9V	
Short Circuit Current (Isc)	6.82A	

Cells	
Number per Module	54
Module Characteristics	
Length $\times$ Width $\times$ Depth	1500mm(59.1in) v.990mm(39.0in) v.36mm(1.4in)
Weight	18.5kg(40.8lbs.)
Cable	(+)760mm(29.9in).(-)1840mm(72.4in)
Junction Box Characteristics	
Length × Width × Depth	100mm(3.9in)×108mm(4.3in)×15mm(0.6in
IP Code	IP65
	IP65
Others	,
	IP65 -40°C∼90°C

Please contact our office for further information



### **KYOCERA Corporation**

■ KYOCERA Corporation Headquarters

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• KYOCERA Solar do Brasil Ltda.

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KYOCERA Solar Pty Ltd.

Level 3, 6-10 Talavera Road, North Ryde N.S.W. 2113, Australia TEL:(61)2-9870-3948 FAX:(61)2-9888-9588 http://www.kyocerasolar.com.au/

KYOCERA Fineceramics GmbH

Fritz-Muller-Strasse 107, 73730 Esslingen German TEL:(49)711-93934-999 FAX:(49)711-93934-950 http://www.kyocerasolar.de/ solar@kyocera.de

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TEL:(82)2-3463-3539 FAX:(82)2-3463-3539
http://www.kyocera.co.kr/

Kyocera reserves the right to modify these specifications without notice

LIE/I10B0711-SAGM



World-class quality
Fully-automated production lines and seamless monitoring of the process and material
ensure the quality that the company sets as its benchmark for its sites worldwide.

**SolarWorld Plus-Sorting**Plus-Sorting guarantees highest system efficiency. SolarWorld only delivers modules that have greater than or equal to the nameplate rated power.

25 years linear performance guarantee and extension of product warranty to 10 years SolarWorld guarantees a maximum performance degression of 0.7% p.a. in the course of 25 years, a significant added value compared to the two-phase warranties common in the industry. In addition, SolarWorld is offering a product warranty, which has been extended to 10 years.\*

"in accordance with the applicable SolarWorld Limited Warranty at purchase www.solarworld.com/warranty

















We turn sunlight into power.

www.solarworld.com

# Sunmodule

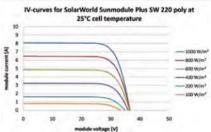
# SW 220 poly / Version 2.0 and 2.5 Frame

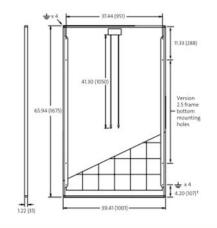
#### PERFORMANCE UNDER STANDARD TEST CONDITIONS (STC)\*

		SW 220
Maximum power	Pman	220 Wp
Open circuit voltage	V <sub>oc</sub>	36.6 V
Maximum power point voltage	V <sub>mpe</sub>	29.2 V
Short circuit current	I <sub>sc</sub>	8.08 A
Maximum power point current	I <sub>mpp</sub>	7.54 A
*****		

#### THERMAL CHARACTERISTICS

46 °C
0.081 %/K
-0.37 %/K
-0.45 %/K
-40°C to 85°C





#### PERFORMANCE AT 800 W/m², NOCT, AM 1.5

		SW 220
Maximum power	Pmar	157.3 Wp
Open circuit voltage	V <sub>ec</sub>	33.1 V
Maximum power point voltage	V <sub>res</sub>	26.2 V
Short circuit current	I,	6.68 A
Maximum power point current	I <sub>mon</sub>	6.01 A
Minor reduction in efficiency under partial I (+/-3%) of the STC efficiency (1000 W/m²) is		at 200W/m², 95%

#### COMPONENT MATERIALS

Cells per module	60
Cell type	Poly crystalline
Cell dimensions	6.14 in x 6.14 in (156 mm x 156 mm)
Front	tempered glass (EN 12150)
Frame	Clear anodized aluminum
Weight	46.7 lbs (21.2 kg)

#### SYSTEM INTEGRATION PARAMETERS

Maximum system volta	ige SC II	1000 V
Max. system voltage USA NEC		600 V
Maximum reverse curr	ent	16 A
Number of bypass diod	es	3
UL Design Loads*	Two rail system	113 psf downward 64 psf upward
UL Design Loads*	Three rail system	170 psf downward 64 psf upward
IEC Design Loads*	Two rail system	113 psf downward 50 psf upward

 ${}^\bullet \text{Please refer to the Sunmodule installation instructions for the details associated with these load cases.}$ 

#### ADDITIONAL DATA

Power tolerance <sup>3)</sup>	-0 Wp / +5 Wp
J-Box	IP65
Connector	MC4
Module efficiency	13.12 %
Fire rating (UL 790)	Class C





SolarWorld AG reserves the right to make specification changes without notice.

<sup>1)</sup> Summodules dedicated for the United States and Canada are tested to UL 1703 Standard and listed by a third party laboratory. The laboratory may vary by product and region. Check with your SolarWorld representative to confirm which laboratory has a listing for the product.

2) Measuring tolarance traceable to TUY Sheinland. 4°-728 (TUY Power Controlled).

3) All units provided are imperial. 51 units provided in parentheses.

### **ANNEXURE B**



PRODUCT SPECIFICATIONS	HOGEN GC 300	HOGEN GC 600	HOGEN GC 4800	
PURE HYDROGEN OUTPUT RATE*	300 cc / min	600 cc / min	4800 cc / min	
ELECTROLYTE SYSTEM	Proton Exchange Membrane (PEM) solid electrolyte, maintenance and caustic-free			
HYDROGEN PURIFICATION TECHNOLOGY	Palladium membrane, maintenance-free PSA, Molecular sieve		PSA, Molecular sieve	
HYDROGEN INVENTORY AT FULL CAPACITY	< 0.1 gram		< 2 grams	
DELIVERY PRESSURE PSIG (BAR)	Adjustable, 45 to 2	Adjustable, 45 to 200 psig (13.8 bar) ± 5%		
PURITY (ASSAY, %)		99.99999+%		
IMPURITIES BY SPECIES	<1 ppm water,	<1 ppm water, <1 ppm total N <sub>2</sub> & O <sub>2</sub> , <1 ppb hydrocarbons/halocarbons		
AUTO-FILL WATER REPLENISHMENT		Standard		
MANUAL FILL WATER CAPACITY	1	.9 liters	N/A (Automatic fill)	
WATER QUALITY REQUIRED (MINIMUM)	Deionized, ASTM Type II	Deionized, ASTM Type II Deionized Water (<1 micro Siemen/cm, >1 MegOhm-cm)		
ELECTRICAL SUPPLY REQUIRED	110 to 220 VAC, single phase, 50 or 60 Hz		205 to 240 VAC, single phase, 50 or 60 Hz	
ELECTRICAL SERVICE RATING	<1000 watts	<1200 watts	4KVA	
CORDSET	US and Internati	onal cordsets available	Hard wired connection	
OPERATING ENVIRONMENT	Indoor, non-classified, 40°F to 95°F (5°C to 35°C), < 90% RH, ventilated			
DUTY CYCLE	100% (24/7/365)			
DIMENSIONS (W x D x H) (Product / Est. Shipping)	14.5" x 20.5" x 9" (37 x 52 x 23 cm) / 23" x 28" x 16" (58 x 71 x 41 cm)		31" x 38" x 42" (79x 97x 107 cm) / 38" x 45" x 52" (97 x 114 x 132 cn	
WEIGHT (Product / Est. Shipping)	50 lbs (23 kg) / 65 lbs (30 kg)		625 lbs (284 kg) / 625 lbs (284 kg)	
PRODUCT CERTIFICATIONS	cTUVus (UL and CSA equivalent), CE (PED, ATEX, LVD, PED, EMC) NYFD Approval			
CONTROLS AND AUTOMATION	LED high visibility display; Adjustable pressure output; Remote alarm terminal/output; Switchable psi/kPa pressure reading (Ethernet and RS232, 4800 only)			
DIAGNOSTICS AND WARNINGS	Water quality, water level, comprehensive self-diagnostics, leak sensing			
MAINTENANCE	Replace one water quality	Replace one water quality resin bag every six months Annual filter changes		
OPTIONS	Deionized water supply system, Auto-crossover manifold for backup gas supply, Pressure reducing regulator			
WARRANTY	2 years parts	2 years parts and factory labor 1 year parts only		
	-			

<sup>\*</sup>Output measurement at 21°C and 1 atmosphere

Consult Proton Onsite Applications and Department for proper installation guidelines. Specifications subject to change.



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```
// Main file
// File: MPPT DC-DC.c
// Author: Neil J.v Rensburg
#include <33FJ32GS606.h>
#define USE PWM1
#define USE PWM2
#define USE PWM3
#define _SINGLE_CLK
// FUSES
// DSPIC33FJ64GS606 Configuration Bit Settings
#fuses NOWRTB, NOBSS
#fuses NOWRT, NOPROTECT
#fuses NOIESO
#fuses NOPR,OSCIO
#fuses NOWINDIS, NOWDT
#fuses PUT32,SS1NORM,QEINORM
#use delay(clock=80MHz, internal=4MHz)
#include <stdio.h>
#include <stdlib.h>
#include <MATH.H>
#include "MPPT PWM.h"
#include "pid.c"
#define MAX_OUTPUTS
                       (3)
WORD wCurLimTimer[3] = \{0,0,0\};
BYTE bCurrentLimitFlg[3] = \{0,0,0\};
BYTE bADCDone
                 = 0:
BYTE bMainIncomerADDone = 0;
WORD wStartIncomingADTimer = cINTER_ADC_CHN_DELAY;
sPIDSTRUCT sPidMem[MAX_OUTPUTS];
float fMPPTDuty = 0.0;
WORD wFilter1[cFILTER CNT] = \{0\};
WORD wFilter2[cFILTER CNT] = {0};
WORD wFilter3[cFILTER_CNT] = \{0\};
WORD wFilter4[cFILTER_CNT] = \{0\};
WORD wIFilter1[cFILTER_CNT] = {0};
WORD wIFilter2[cFILTER CNT] = {0};
WORD wIFilter3[cFILTER_CNT] = {0};
WORD wFilter0[cFILTER CNT] = \{0\};
WORD wIFilter0[cFILTER_CNT] = {0};
```

```
int8 iwFilterIdx1 = 0;
int8 iwFilterIdx2 = 0;
int8 iwFilterIdx3 = 0;
int8 iwFilterIdx4 = 0;
int8 iwFilterIdx0 = 0;
int8 iwFilterIdxI0 = 0;
float fDuty[3] = \{10.0, 10.0, 10.0\};
float output;
float fVInFiltered;
float fIInFiltered;
int8 iFilterDone = 0;
BYTE bSecTgl = 0, bPwmOn = 0;
sANAENG sAnaVals[10];
int main(int argc, char** argv)
  int8 iIdx:
  vKickWdt
                ();
  delay_cycles (100);
  vKickWdt
                ();
  vSetupBoard
                ();
  vKickWdt
                ();
  delay_cycles
               (100);
  vKickWdt
                ();
  vSwitchPower (1);
  output_bit
              (LED_SYS,bSecTgl);
  while (1)
    vKickWdt ();
    delay_us (1);
    if ((bADCDone \& 0x0F) == 0x0F){
         vKickWdt
                        (&bADCDone);
         vDoEngConv
         vDoMPPTControl ();
      for (iIdx = 0; iIdx < 3; iIdx++)
         vDoPwmVOutControl\\
                                 (iIdx);
      }
      PWMCON2FLTIEN = 0;
      PWMCON2CLIEN = 0;
      PWMCON2TRGIEN = 0;
      PWMCON1FLTIEN = 0;
      PWMCON1CLIEN = 0;
      PWMCON1TRGIEN = 0;
      PWMCON3FLTIEN = 0:
      PWMCON3CLIEN = 0;
      PWMCON3TRGIEN = 0;
```

```
}
    if ((fVInFiltered > (cVIN_MIN_SW_ON + cVIN_MIN_SW_ON_HYST)) &&
(bPwmOn==0))
      int i;
      for (i = 0; i < 3; i++)
        vClearPidNvStruct (&sPidMem[i]);
      vStartPWM
                    ();
      bPwmOn
                    = 1;
    if ((fVInFiltered < (cVIN_MIN_SW_ON - cVIN_MIN_SW_ON_HYST)) &&
(bPwmOn==1)
      vStopPWM
                     ();
      bPwmOn
                    = 0;
    if (0)
    { // if PV_IN_PRE_SW is above VIN_MIN_SW_ON, it is safe to switch on VIN.
      if (sAnaVals[8].fConverted >= cVIN_MIN_SW_ON) vSwitchPower(1);
                                  vSwitchPower(0);
      else
      bMainIncomerADDone = 0;
    output_bit(LED_SYS,bSecTgl);
 return (0);//EXIT_SUCCESS);
void vSetupBoard
                      (void)
  vStopPWM
                 ();
 delay_cycles (100);
  vInitClock
              ();
 delay_cycles
              (100);
  vSetupPins
               ();
 delay_cycles
               (100);
  vSetupPWM
                 ():
 delay_cycles
               (100);
 delay cycles
               (100);
 vKickWdt
               ();
  vSetupADC
                ();
 delay_cycles (100);
  vSetupTimers ();
 delay_cycles (100);
  vSetupInterrupts();
  vSetupStruct();
void vSwitchPower (int8 bState)
 if (bState) output_bit
                       (POWERON,1);
```

```
else
          output_bit
                      (POWERON,0);
void vSetupStruct(void)
 int i;
 memset (sAnaVals,0,sizeof(sANAENG)*10);
 sAnaVals[0].wRawHigh = 373;
 sAnaVals[0].fEngHigh = 4.2;
 sAnaVals[1].wRawHigh = 1024;
 sAnaVals[1].fEngHigh = 30.932;
 sAnaVals[2].wRawHigh = 373;
 sAnaVals[2].fEngHigh = 10.0;
 sAnaVals[3].wRawHigh = 1024;
 sAnaVals[3].fEngHigh = 13.062;
 sAnaVals[4].wRawHigh = 1024;
 sAnaVals[4].fEngHigh = 17.719;
 sAnaVals[5].wRawHigh = 373;
 sAnaVals[5].fEngHigh = 20.0;
 sAnaVals[6].wRawHigh = 1024;
 sAnaVals[6].fEngHigh = 42.786;
 sAnaVals[7].wRawHigh = 1024;
 sAnaVals[7].fEngLow = -0.100;
 sAnaVals[7].fEngHigh = 28.406;
 sAnaVals[8].wRawHigh = 1024;
 sAnaVals[8].fEngHigh = 42.9;
 sAnaVals[9].wRawHigh = 1024;
 sAnaVals[9].fEngHigh = 0.0;
  for (i = 0; i < 3; i++)
    vClearPidNvStruct (&sPidMem[i]);
 //PID P, I, D values
 sPidMem[0].fKp
                    = 0.4;
 sPidMem[0].fKi
                    = 0.05;
                    = 0.1;
 sPidMem[0].fKd
 sPidMem[1].fKp
                    = 0.35;
                    = 0.015;
 sPidMem[1].fKi
 sPidMem[1].fKd
                    = 0.05;
 sPidMem[2].fKp
                    = 0.33;
 sPidMem[2].fKi
                    = 0.005;
 sPidMem[2].fKd
                    = 0.07;
void vInitClock
                    (void)
{
  setup_oscillator(OSC_INTERNAL);
  delay_cycles (100);
  ACLKCONASRCSEL = 0;
  FRCSEL = 1:
  delay_cycles (100);
  ENAPLL = 1;
```

```
delay_cycles (100);
  SELACLK = 1;
 delay_cycles (100);
  APSTSCLR2 = 1; APSTSCLR1 = 1; APSTSCLR0 = 0;
 delay_cycles (100);
  while (APLLCK == 0);
 delay_cycles (100);
}
void
     vSetupPins
                  (void)
  ADPCFGPCFG0 = ADPCFGPCFG1 = ADPCFGPCFG2 = ADPCFGPCFG3 =
ADPCFGPCFG4 = ADPCFGPCFG5 = ADPCFGPCFG8 = 0;
  ADPCFGPCFG12 = ADPCFGPCFG13 = ADPCFGPCFG14 = ADPCFGPCFG15 = 0;
 set_tris_b
            (0xFFFF);
 set_tris_c
            (0xFFFF);
 set tris d
            (0xF9F0);
 set tris e
            (0xFFC0);
 set_tris_f
            (0xFFF7);
            (0xFFFF);
 set_tris_g
 output_high
              (LED_PWM1_OC);
 output_high
              (LED_PWM2_OC);
 output_high
              (LED_PWM3_OC);
              (LED PWM1 GD);
 output high
  output high
              (LED PWM2 GD);
 output_high
              (LED_PWM3_GD);
 output_high
              (LED_SYS);
              (DEBUG_PIN);
 output_high
}
void vSetupPWM
                   (void)
// General PWM Registers
 PTCON2 = 0;
  delay_cycles(100);
  PTPER = PWM PERIOD;
 SEVTCMP = 0;
 PTCONPTSIDL = 0;
 PWMCON1MDCS = 0;
// PWM1
#ifdef USE PWM1
  delay_cycles(100);
  PWMCON1FLTIEN = 0;
 PWMCON1CLIEN = 0;
 PWMCON1TRGIEN = 0;
 PWMCON1MTBS = 0;
 PWMCON1CAM = 0:
  PWMCON1XPRES = 0;
#ifdef SINGLE_CLK
```

```
PWMCON1ITB = 0;
 PWMCON1ITB = 1;
#endif
  PWMCON1MDCS = 0;
 PWMCON1DTC1 = 0; PWMCON1DTC0 = 0;
 PWMCON1IUE = 0;
 PDC1 = (PWM PERIOD/10);
#ifndef SINGLE_CLK
 PHASE1 = PWM PERIOD+100;
 SPHASE1 = PWM_PERIOD+100;
#endif
 DTR1 = 120;
  ALTDTR1 = 150;
 delay_cycles(100);
 IOCON1 = 0;
 IOCON1PMOD1 = IOCON1PMOD0 = 0;
 delay cycles(100);
 IOCON1POLH = 0;
 IOCON1POLL = 0;
 delay_cycles(100);
 IOCON1PENH = 1;
 IOCON1PENL = 1;
 delay_cycles(100);
#endif
 // PWM2
#ifdef USE_PWM2
  PWMCON2FLTIEN = 0;
 PWMCON2CLIEN = 0;
 PWMCON2TRGIEN = 0;
 PWMCON2MTBS = 0;
 PWMCON2CAM = 0;
 PWMCON2XPRES = 0;
 PWMCON2ITB = 0;
 PWMCON2MDCS = 0;
 PWMCON2DTC1 = 0; PWMCON2DTC0 = 0;
 PWMCON2IUE = 0;
 PDC2 = (PWM\_PERIOD/10);
 PHASE2 = 0;
 SPHASE2 = 0;
 DTR2 = 180;
 ALTDTR2 = 120;
 delay_cycles (100);
// IOCON1 = 0;
  IOCON2PMOD1 = IOCON2PMOD0 = 0;
  delay_cycles(100);
 IOCON2POLH = 0;
 IOCON2POLL = 0;
 delay cycles(100):
 IOCON2PENH = 1;
 IOCON2PENL = 1;
```

```
delay_cycles(100);
#endif
 // PWM3
#ifdef USE_PWM3
 PWMCON3FLTIEN = 0;
 PWMCON3CLIEN = 0;
 PWMCON3TRGIEN = 0;
 PWMCON3MTBS = 0;
 PWMCON3CAM = 0;
 PWMCON3XPRES = 0;
 PWMCON3ITB = 0;
 PWMCON3MDCS = 0;
 PWMCON3DTC1 = 0; PWMCON3DTC0 = 0;
 PWMCON3IUE = 0;
 PDC3 = (PWM\_PERIOD/10);
 DTR3 = 180;
 ALTDTR3 = 150;
 delay_cycles (100);
 IOCON3PMOD1 = IOCON3PMOD0 = 0;
 delay_cycles (100);
 IOCON3POLH = 0;
 IOCON3POLL = 0;
 delay_cycles (100);
 IOCON3PENH = 1;
 IOCON3PENL = 1;
 delay_cycles (100);
#endif
 //Additional registers
 PTCONPTSIDL = 0;
 PTCONSYNCOEN = 1;
 delay_cycles(255);
}
void vStartPWM
                (void)
 IOCON1PENH
                 = 1;
                = 1;
 IOCON1PENL
 IOCON2PENH
                = 1;
 IOCON2PENL
                = 1;
 IOCON3PENH
                = 1;
 IOCON3PENL
                = 1;
                                      // Enable the PWM Module
 PTCONPTEN
                = 1;
}
void vStopPWM
                (void)
 PTCON
                                      // Disable the PWM Module
 IOCON1PENH
                = 0;
                = 0:
 IOCON1PENL
 IOCON2PENH
                = 0;
 IOCON2PENL
                = 0;
```

```
IOCON3PENH
                 = 0;
  IOCON3PENL
                 = 0;
}
void vSetupADC
                  (void)
 setup_high_speed_adc (ADC_OFF);
 setup_high_speed_adc_pair(0, INDIVIDUAL_SOFTWARE_TRIGGER);
 setup_high_speed_adc_pair(1, INDIVIDUAL_SOFTWARE_TRIGGER);
 setup_high_speed_adc_pair(2, INDIVIDUAL_SOFTWARE_TRIGGER);
 setup_high_speed_adc_pair(6, INDIVIDUAL_SOFTWARE_TRIGGER);
 setup_high_speed_adc_pair(7, INDIVIDUAL_SOFTWARE_TRIGGER);
  setup_adc_ports
(sAN0|sAN1|sAN2|sAN3|sAN4|sAN5|sAN12|sAN13|sAN14|sAN15);
 ADCONORDER = 0:
 ADCONASYNCSAMP = 0;
 ADCONSEQSAMP = 1;
 setup_high_speed_adc (ADC_CLOCKED_BY_PRI_PLL|ADC_CLOCK_DIV_6);
}
void vSetupTimers (void)
    setup_timer1 (TMR_INTERNAL|TMR_DIV_BY_64,625);
void vSetupInterrupts (void)
 enable_interrupts(INT_TIMER1);
 enable_interrupts(INTR_GLOBAL);
}
#define cMS RELOAD VAL
                           (1)
#define cSEC_RELOAD_VAL
                           (1000)
BYTE bMsCntr = cMS RELOAD VAL;
WORD wSecCntr = cSEC_RELOAD_VAL;
//
#INT_TIMER1
void vT1_ISR (void)
  if (bMsCntr) {--bMsCntr;return;}
 bMsCntr
             = cMS_RELOAD_VAL;
 // millisecond code
 if (wCurLimTimer[0]) wCurLimTimer[0]--;
 if (wCurLimTimer[0] == 1) bCurrentLimitFlg[0] = 0;
```

```
if (wCurLimTimer[1]) wCurLimTimer[1]--;
  if (wCurLimTimer[1] == 1) bCurrentLimitFlg[1] = 0;
  if (wCurLimTimer[2]) wCurLimTimer[2]--;
  if (wCurLimTimer[2] == 1) bCurrentLimitFlg[2] = 0;
  if (wStartIncomingADTimer) wStartIncomingADTimer--;
  if (wStartIncomingADTimer == 1)
    IFS6ADCP0IF = 0;
    ADCP0IE = 1;
    ADCPC0SWTRG0 = 1;
#endif
  // one second code
  if (wSecCntr) {--wSecCntr;return;}
               = cSEC_RELOAD_VAL;
  wSecCntr
  bSecTgl
              ^{\sim} 0x01;
unsigned int32 ulWaitForPair0= 0;
#INT_ADCP0
void vADCP0_ISR (void)
  static int8 bState = 0;
  int16 wTmp;
  if (ADCPC0PEND1!=0)
    ADCP0IE = 1;
    ADCPC0SWTRG0 = 1;
    ulWaitForPair0++;
    output_high(LED_PWM3_GD);
    return;
  wTmp = (unsigned int16)ADCBUF0;
  wTmp = (unsigned int16)ADCBUF1;
    switch (bState)
  {
    case 0:
      IFS7ADCP2IF = 0;
      ADCP2IE = 1;
      ADCPC1SWTRG2 = 1;
      bState++;
      break;
    case 1:
      IFS6ADCP1IF = 0;
      ADCP1IE = 1:
      ADCPC0SWTRG1 = 1;
      bState++;
```

```
break;
    case 2:
      IFS7ADCP7IF = 0;
      ADCP7IE = 1;
      ADCPC3SWTRG7 = 1;
      bState++;
      break;
    case 3:
      IFS7ADCP6IF = 0;
      ADCPC3SWTRG6 = 1;
      ADCP6IE = 1;
      bState = 0;
      break;
  IFS6ADCP0IF = 0;
  ADCP0IE = 0;
  ADCPC0SWTRG0 = 0;
  output_high(LED_PWM3_GD);
}
unsigned int32 ulWaitForPair1= 0;
#INT_ADCP1
void vADCP1_ISR (void)
{
  int16 wVoltTmp,wTmp;
  if (ADCPC0PEND1!=0)
    ADCP1IE = 1;
    ADCPC0SWTRG1 = 1;
    ulWaitForPair1++;
    output_high(LED_PWM1_GD);
    return;
  wVoltTmp = (unsigned int16)ADCBUF2;
  if (sAnaVals[0].sRawVal == 0)
    wIFilter1[iwFilterIdx1] = wVoltTmp;
  else
    wTmp = sAnaVals[0].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wIFilter1[iwFilterIdx1] = wVoltTmp;
    else
      wIFilter1[iwFilterIdx1] = wTmp;
  }
```

```
wVoltTmp = (unsigned int16)ADCBUF3;
 if (sAnaVals[1].sRawVal == 0)
    wFilter1[iwFilterIdx1] = wVoltTmp;
 else
    wTmp = sAnaVals[1].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wFilter1[iwFilterIdx1] = wVoltTmp;
    else
      wFilter1[iwFilterIdx1] = wTmp;
  }
 if (++iwFilterIdx1 > cFILTER\_CNT) iwFilterIdx1 = 0;
 bADCDone |= cADCP1DONE;
 IFS6ADCP1IF = 0;
  ADCP1IE = 0;
 output_high(LED_PWM1_GD);
unsigned int32 ulWaitForPair2= 0;
#INT_ADCP2
void vADCP2_ISR (void)
 int16 wVoltTmp,wTmp;
 if (ADCPC1PEND2!=0)
    ADCP2IE = 1;
    ADCPC1SWTRG2 = 1;
    ulWaitForPair2++;
    return;
  wVoltTmp = (unsigned int16)ADCBUF5;
 if (sAnaVals[3].sRawVal == 0)
    wFilter2[iwFilterIdx2] = wVoltTmp;
 else
    wTmp = sAnaVals[3].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wFilter2[iwFilterIdx2] = wVoltTmp;
    else
      wFilter2[iwFilterIdx2] = wTmp;
  }
  wVoltTmp = (unsigned int16)ADCBUF4;
 if (sAnaVals[2].sRawVal == 0)
    wIFilter2[iwFilterIdx2] = wVoltTmp;
 else
```

```
wTmp = sAnaVals[2].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wIFilter2[iwFilterIdx2] = wVoltTmp;
    else
      wIFilter2[iwFilterIdx2] = wTmp;
  }
  if (++iwFilterIdx2 > cFILTER_CNT) iwFilterIdx2 = 0;
  bADCDone |= cADCP2DONE;
  IFS7ADCP2IF = 0;
  ADCP2IE = 0;
unsigned int32 ulWaitForPair4= 0;
#INT ADCP4
void vADCP4_ISR (void)
  if (ADCPC2PEND4!=0)
    ADCP4IE = 1;
    ADCPC2SWTRG4 = 1;
    ulWaitForPair4++;
    output_high(LED_PWM3_GD);
    return;
  wFilter4[iwFilterIdx4] = (unsigned int16)ADCBUF8;
  if (++iwFilterIdx4 > cFILTER_CNT) iwFilterIdx4 = 0;
  bADCDone |= cADCP4DONE;
  IFS7ADCP4IF = 0;
  ADCP4IE = 0;
  output_high(LED_PWM3_GD);
unsigned int32 ulWaitForPair6= 0;
#INT_ADCP6
void vADCP6_ISR (void)
  int16 wVoltTmp,wTmp;
  if (ADCPC3PEND6!=0)
    ADCP6IE = 1;
    ADCPC3SWTRG6 = 1;
    ulWaitForPair6++;
    return;
```

```
}
#ifdef BRD_V2
  wVoltTmp = (unsigned int16)ADCBUF13;
  if (sAnaVals[6].sRawVal == 0)
    wFilter0[iwFilterIdx0] = wVoltTmp;
  else
    wTmp = sAnaVals[6].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wFilter0[iwFilterIdx0] = wVoltTmp;
    else
      wFilter0[iwFilterIdx0] = wTmp;
  }
  wVoltTmp = (unsigned int16)ADCBUF12;
  if (sAnaVals[7].sRawVal == 0)
    wIFilter0[iwFilterIdx0] = wVoltTmp;
  else
         wTmp = sAnaVals[7].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wIFilter0[iwFilterIdxI0] = wVoltTmp;
    else
      wIFilter0[iwFilterIdxI0] = wTmp;
#endif
  if (++iwFilterIdx0 > cFILTER_CNT) iwFilterIdx0 = 0;
  if (++iwFilterIdxI0 > cFILTER_CNT) iwFilterIdxI0 = 0;
  bADCDone |= cADCP6DONE;
  IFS7ADCP6IF = 0;
  ADCP6IE = 0;
}
unsigned int32 ulWaitForPair7= 0;
#INT ADCP7
void vADCP7_ISR (void)
  int16 wVoltTmp,wTmp;
  if (ADCPC3PEND7!=0)
    ADCP7IE = 1;
    ADCPC3SWTRG7 = 1;
    ulWaitForPair7++;
    return;
```

```
wVoltTmp = (unsigned int16)ADCBUF15;
  if (sAnaVals[4].sRawVal == 0)
    wFilter3[iwFilterIdx3] = wVoltTmp;
  else
    wTmp = sAnaVals[4].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wFilter3[iwFilterIdx3] = wVoltTmp;
    else
      wFilter3[iwFilterIdx3] = wTmp;
  }
  wVoltTmp = (unsigned int16)ADCBUF14;
  if (sAnaVals[5].sRawVal == 0)
    wIFilter3[iwFilterIdx3] = wVoltTmp;
  else
    wTmp = sAnaVals[5].sRawVal +10;
    if (wVoltTmp < wTmp)</pre>
      wIFilter3[iwFilterIdx3] = wVoltTmp;
    else
      wIFilter3[iwFilterIdx3] = wTmp;
  }
  if (++iwFilterIdx3 > cFILTER_CNT) iwFilterIdx3 = 0;
  bADCDone |= cADCP7DONE;
  ADCP7IE = 0;
  IFS7ADCP7IF = 0;
}
void vDoMPPTControl (void)
  float fPIn,fPDiff,fVDiff,fVInFilteredLoc;
  static float fStepAdj = PWM_MPPT_STEP;
  static float fPInLast = 0.0;
  static float fVInLast = 0.0;
  int8 bSign;
  static int8 bSignLast;
  fVInFilteredLoc = floor(fVInFiltered);
  fPIn = fVInFilteredLoc * fIInFiltered;
  fPDiff = fPIn - fPInLast;
  fVDiff = fVInFilteredLoc - fVInLast:
  output_toggle(LED_PWM3_OC);
```

```
if ((fPDiff == 0.0) && (fVDiff == 0.0)) return;
 // Do P&O
 output_toggle(LED_PWM2_OC);
 if (fPDiff > 0.0)
    if (fVDiff > 0.0)
                      bSign = 1;
                  bSign = -1;
    else
 else
    if (fVDiff > 0.0)
                      bSign = -1;
                   bSign = 1;
    else
 // dynamically adjust the step size for as long as sign stays the same
  if (bSign == bSignLast)
    fStepAdj = fStepAdj + PWM MPPT STEP;
    if (fStepAdj > cP_O_MAX_ADJ) fStepAdj = cP_O_MAX_ADJ;
 else
    fStepAdj = PWM_MPPT_STEP;
 bSignLast = bSign;
  fMPPTDuty += fStepAdj * (float)bSign;
 if (fMPPTDuty < cP_O_MIN_ADJ) fMPPTDuty = cP_O_MIN_ADJ;
 if (fMPPTDuty > cP_O_MAX_ADJ) fMPPTDuty = cP_O_MAX_ADJ;
 fPInLast = fPIn;
  fVInLast = fVinFiltered;
void vDoPwmVOutControl (int8 iIdx)
  float fVInNom,fIInMax,fCurrentV,fCurrentI,fTmp,fIOvr;
 float output; //PID Variable
  unsigned int16 wLed;
  if (!iFilterDone) return;
 switch (iIdx)
    default: return;
#ifdef USE_PWM1
    case 0:
      fVInNom = 12.0; fIInMax = 4.2;
      fCurrentI = sAnaVals[0].fConverted;
      fCurrentV = sAnaVals[1].fConverted;
               = LED PWM1 GD:
      wLed
      fIOvr
              = c4_2A_OVR_CUR;
      break;
```

```
#endif
#ifdef USE_PWM2
    case 1:
      fVInNom = 5.0;
                        fIInMax = 10.0;
      fCurrentI = sAnaVals[2].fConverted;
      fCurrentV = sAnaVals[3].fConverted;
              = LED_PWM2_GD;
      wLed
      fIOvr
              = c10A_OVR_CUR;
      break;
#endif
#ifdef USE_PWM3
    case 2:
      fVInNom = 7.5;
                        fIInMax = 20.0;
      fCurrentV = sAnaVals[4].fConverted;
      fCurrentI = sAnaVals[5].fConverted;
      wLed = LED_PWM3_GD;
      fIOvr = c20A OVR CUR;
      iFilterDone = 0:
      break;
#endif
  if (fCurrentV == 0.0) fCurrentV = 0.1;
  disable_interrupts(GLOBAL);
#ifdef DO PID CONTROL
#ifdef USE MPPT
  sPidMem[iIdx].setpoint = fVInNom + (fVInNom * (fMPPTDuty/100.0));
  sPidMem[iIdx].setpoint = fVInNom;
#endif //USE_MPPT
  output = PIDcal(&sPidMem[iIdx], fCurrentV);
  fDuty[iIdx] = fDuty[iIdx] + output;
#endif //DO PID CONTROL
  enable_interrupts(GLOBAL);
  if (fDuty[iIdx] < PWM MIN) fDuty[iIdx] = PWM MIN;
  if (fDuty[iIdx] > PWM_MAX) fDuty[iIdx] = PWM_MAX;
  fTmp = fDuty[iIdx];
  if ( fTmp < 3.0) fTmp = 3.0;
  if (fTmp > 97.0) fTmp = 97.0;
  if ((iIdx < 0) \&\& (iIdx > 2)) return;
  if (bPwmOn == 0)
    fDuty[iIdx] = 1.0;
    vSetDuty (iIdx,fDuty[iIdx]);
    return;
  vSetDuty(iIdx, fTmp);
  switch (iIdx)
           wLed = LED_PWM1_OC; break;
   case 0:
```

```
wLed = LED_PWM1_OC; break;
   case 1:
   case 2:
           wLed = LED_PWM1_OC; break;
unsigned int16 wRunFilter (WORD *wFilterData)
 int8 iCnt;
 int32 1Tmp = 0;
  WORD wFilteredVal;
 for (iCnt = 0; iCnt < cFILTER_CNT; iCnt++,wFilterData++)
    lTmp += *wFilterData;
  wFilteredVal = lTmp / cFILTER_CNT;
 iFilterDone = 1;
 return wFilteredVal;
}
void vDoEngConv
                     (BYTE *bPairsDone)
 if (*bPairsDone & cADCP1DONE)
    sAnaVals[0].sRawVal = wRunFilter(wIFilter1);
    vCalcEng(0);
    sAnaVals[1].sRawVal = wRunFilter(wFilter1);
     vCalcEng(1);
    *bPairsDone &= ~cADCP1DONE;
 if (*bPairsDone & cADCP2DONE)
    sAnaVals[2].sRawVal = wRunFilter(wIFilter2);
    vCalcEng(2);
    sAnaVals[3].sRawVal = wRunFilter(wFilter2);
    vCalcEng(3);
    *bPairsDone &= ~cADCP2DONE;
 if (*bPairsDone & cADCP6DONE)
    sAnaVals[6].sRawVal = wRunFilter(wFilter0);
    vCalcEng(6);
    fVInFiltered = sAnaVals[6].fConverted;
    sAnaVals[7].sRawVal = wRunFilter(wIFilter0);
    vCalcEng(7);
    fIInFiltered = sAnaVals[7].fConverted;
    *bPairsDone &= ~cADCP6DONE;
    bMainIncomerADDone = 1;
```

```
if (*bPairsDone & cADCP7DONE)
    sAnaVals[4].sRawVal = wRunFilter(wFilter3);
    vCalcEng(4);
    sAnaVals[5].sRawVal = wRunFilter(wIFilter3);
    vCalcEng(5);
    *bPairsDone &= ~cADCP7DONE;
  if (*bPairsDone & cADCP4DONE)
 }
    sAnaVals[8].sRawVal = wRunFilter(wFilter4);
    vCalcEng(8);
    *bPairsDone &= ~cADCP7DONE;
    bMainIncomerADDone = 1:
 return;
void vCalcEng (int8 iIdx)
  WORD wRawSpan,wTmpVal,wRawVal;
  float fEngSpan,fTmpVal;
 // Do Eng Conv on 2 consecutive channels
  wRawVal = sAnaVals[iIdx].sRawVal;
  wRawSpan = sAnaVals[iIdx].wRawHigh - sAnaVals[iIdx].wRawLow;
  if (wRawSpan == 0)wRawSpan = 1024;
  fEngSpan = sAnaVals[iIdx].fEngHigh - sAnaVals[iIdx].fEngLow;
  if (fEngSpan \le 0.0) fEngSpan = 100.0;
  if (sAnaVals[iIdx].sRawVal <= sAnaVals[iIdx].wRawLow) {sAnaVals[iIdx].fConverted
=sAnaVals[iIdx].fEngLow;return;}
  wTmpVal = (sAnaVals[iIdx].sRawVal - sAnaVals[iIdx].wRawLow);
  fTmpVal = (float)wTmpVal * fEngSpan;
  fTmpVal /= (float)wRawSpan;
  fTmpVal += sAnaVals[iIdx].fEngLow;
 if (fTmpVal < 0.0) fTmpVal = 0.0;
 sAnaVals[iIdx].fConverted = fTmpVal;
 return;
#ifdef USE HIST
WORD wPrevPDCVal[3][HIST COUNT] = \{0,0,0\};
WORD wPrevValTemp[HIST_COUNT+1] = \{0,0,0\};
WORD bHistValIdx[3]
                           = \{0,0,0\};
```

```
WORD wAddHistVal (BYTE bldx, WORD wVal)
  int8 bTmp;
 unsigned long ulAveVal = 0;
  if (bHistValIdx[bIdx] < HIST_COUNT)
    wPrevPDCVal[bIdx][bHistValIdx[bIdx]] = wVal;
    bHistValIdx[bIdx]++;
    return wVal;
 memcpy (wPrevValTemp,&wPrevPDCVal[bIdx][0],HIST_COUNT<<1);</pre>
  wPrevValTemp[HIST COUNT] = wVal;
  memcpy (&wPrevPDCVal[bIdx][0],wPrevValTemp+1,HIST_COUNT<<1);</pre>
  for (bTmp = 0; bTmp < HIST_COUNT; bTmp++)
                += wPrevPDCVal[bIdx][bTmp];
    ulAveVal
 ulAveVal
                = ulAveVal / HIST COUNT;
              ((WORD)ulAveVal);
 return
#endif
void vSetDuty (BYTE bIdx,float fVal)
  WORD wTmp,wDtMax;
  switch (bIdx)
    case 0:
      wDtMax = (DTR1 > ALTDTR1 ? DTR1 : ALTDTR1);
      wTmp = (WORD)((float)(PWM PERIOD) * (fVal/100.0));
      if (wTmp \le wDtMax + 30) wTmp = wDtMax + 30;
      if (wTmp >= PWM PERIOD - wDtMax - 60) wTmp = PWM PERIOD - wDtMax -
60;
#ifdef USE_HIST
      wTmp
                    = wAddHistVal (bIdx,wTmp);
#endif
      PDC1 = wTmp;
      break;
    case 1:
      wDtMax = (DTR2 > ALTDTR2 ? DTR2 : ALTDTR2);
      wTmp = (WORD)((float)(PWM\_PERIOD) * (fVal/100.0));
      if (wTmp \le wDtMax + 10) wTmp = wDtMax + 10;
      if (wTmp >= PWM_PERIOD - wDtMax - 10) wTmp = PWM_PERIOD - wDtMax -
10;
#ifdef USE_HIST
      wTmp
                    = wAddHistVal (bIdx,wTmp);
#endif
      PDC2 = wTmp;
```

```
break;
    case 2:
      wDtMax = (DTR3 > ALTDTR3 ? DTR3 : ALTDTR3);
      wTmp = (WORD)((float)(PWM\_PERIOD) * (fVal/100.0));
      if (wTmp \le wDtMax + 10) wTmp = wDtMax + 10;
      if (wTmp >= PWM_PERIOD - wDtMax - 10) wTmp = PWM_PERIOD - wDtMax -
10;
#ifdef USE_HIST
      wTmp
                   = wAddHistVal (bIdx,wTmp);
#endif
      PDC3 = wTmp;
      break;
  }
}
void vSetPwmOff (unsigned int8 bIdx)
 switch (bIdx)
    case 0:
      IOCON1PENH = IOCON1PENL = 0;
      output_high (PWM1H);
      output_low
                  (PWM1L);
      break;
    case 1:
      IOCON2PENH = IOCON2PENL = 0;
                 (PWM2H);
      output_high
      output low
                  (PWM2L);
      break;
    case 2:
      IOCON3PENH = IOCON3PENL = 0;
                 (PWM3H);
      output_high
                  (PWM3L);
      output low
      break;
  }
}
void vSetPwmOn (unsigned int8 bIdx)
 switch (bIdx)
    case 0: IOCON1PENH = IOCON1PENL = 1;
                                                 break;
    case 1: IOCON2PENH = IOCON2PENL = 1:
                                                 break:
    case 2: IOCON3PENH = IOCON3PENL = 1;
                                                 break;
```

```
}
#INT_CMP1
void vISR_Comp1 (void)
  wCurLimTimer[0] = cCURRENT_LIMIT_TIME;
  bCurrentLimitFlg[0] = 1;
#INT_CMP2
void vISR_Comp2 (void)
  wCurLimTimer[1] = cCURRENT_LIMIT_TIME;
  bCurrentLimitFlg[1] = 1;
#INT CMP3
void vISR_Comp3 (void)
  wCurLimTimer[2] = cCURRENT_LIMIT_TIME;
  bCurrentLimitFlg[2] = 1;
//Header file
// File: MPPT DC-DC.h
// Author: Neil J.v Rensburg
#ifndef MPPT_PWM
#define MPPT_PWM
#ifdef __cplusplus
extern "C" {
#endif
#define BRD_V2
#define USE_HIST
#define NEW_AD_RES_VALS
#define USE_MPPT
#define DO_PID_CONTROL
#define cONE SEC
                         (300)
#define cINTER_ADC_CHN_DELAY (10)
#define cOVER_CURRENT_DELAY
                                  (1000)
#define c4_2A_OVR_CUR
                            (4.8)
#define c10A_OVR_CUR
                            (11.0)
#define c20A_OVR_CUR
                            (22.0)
#define START PAIR1
                          (0)
#define WAIT_PAIR2
                          (1)
#define START_PAIR2
                          (2)
```

```
#define WAIT PAIR3
                       (3)
#define START_PAIR3
                        (4)
#define WAIT_PAIR4
                       (5)
#define START_PAIR4
                        (6)
#define WAIT_PAIR5
                       (7)
#define START PAIR5
                        (8)
#define WAIT_PAIR1
                       (9)
 #ifdef BRD V2
#define ADCIS1
                 PIN B2
#define ADCVMC1
                   PIN_B3
#define ADCIS2
                 PIN B4
                   PIN_B5
#define ADCVMC2
#define VIN_PWR_GOOD PIN_B8
#define ADCCSMPP
                   PIN B12
#define ADCVSMPP
                   PIN B13
                 PIN_B14
#define ADCIS3
#define ADCVMC3
                   PIN_B15
#define LED_PWM1_OC
                      PIN_C13
#define LED_PWM1_GD
                      PIN_C14
#define LED PWM2 GD
                      PIN D0
#define LED SYS
                  PIN D1
#define CHRG_ON
                   PIN D3
#define LED_PWM3_OC
                     PIN_D9
#define LED_PWM3_GD
                      PIN_D10
#define LED_PWM2_OC
                      PIN_D11
#define DEBUG PIN
                   PIN B0
#define COMPVREF
                    PIN B11
#define WDK
                PIN_D2
#define POWERON
                   PIN<sub>F3</sub>
#define PWM1L
                  PIN E0
#define PWM1H
                  PIN_E1
#define PWM2L
                 PIN E2
#define PWM2H
                  PIN<sub>E3</sub>
#define PWM3L
                  PIN E4
#define PWM3H
                  PIN_E5
#WORD PLLFBD
                 = 0x0746
#WORD CLKDIV
                 = 0x0744
#BIT PLLPOST1
                = CLKDIV.6
#BIT PLLPOST0
               = CLKDIV.5
```

= CLKDIV.4

= CLKDIV.3

#BIT PLLPRE4

#BIT PLLPRE3

```
#BIT PLLPRE2
              = CLKDIV.2
#BIT PLLPRE1
              = CLKDIV.1
#BIT PLLPRE0
             = CLKDIV.0
#WORD ACLKCON
                = 0x0750
#BIT FRCSEL
            = ACLKCON.6
             = ACLKCON.7
#BIT SELACLK
#BIT APSTSCLR0 = ACLKCON.8
#BIT APSTSCLR1 = ACLKCON.9
#BIT APSTSCLR2 = ACLKCON.10
#BIT ENAPLL
             = ACLKCON.15
              = ACLKCON.14
#BIT APLLCK
#WORD OSCCON
              = 0x0742
#BIT OSWEN
            = OSCCON.0
             = OSCCON.5
#BIT LOCK
#BIT NOSC2
            = OSCCON.10
#BIT NOSC1
             = OSCCON.9
#BIT NOSCO
             = OSCCON.8
#BIT COSC2
             = OSCCON.14
#BIT COSC1
           = OSCCON.13
             = OSCCON.12
#BIT COSCO
#WORD ACLKCON
                  = 0x0750
#BIT ACLKCONENAPLL
                     = ACLKCON.15
#BIT ACLKCONAPLLCK
                      = ACLKCON.14
#BIT ACLKCONSELACLK = ACLKCON.13
#BIT ACLKCONAPSTSCLR2 = ACLKCON.10
#BIT ACLKCONAPSTSCLR1 = ACLKCON.9
#BIT ACLKCONAPSTSCLR0 = ACLKCON.8
#BIT ACLKCONASRCSEL = ACLKCON.7
#BIT ACLKCONFRCSEL
                     = ACLKCON.6
#WORD CLKDIV = 0x0744
#BIT CLKDIVPLLPOST1 = CLKDIV.7
#BIT CLKDIVPLLPOST0 = CLKDIV.6
#BIT CLKDIVPLLPRE4
                    = CLKDIV.4
#BIT CLKDIVPLLPRE3
                    = CLKDIV.3
#BIT CLKDIVPLLPRE2
                    = CLKDIV.2
#BIT CLKDIVPLLPRE1
                    = CLKDIV.1
#BIT CLKDIVPLLPRE0
                    = CLKDIV.0
#WORD OSCCON
                  = 0x0742
#BIT OSCCONLOCK
                   = OSCCON.5
               = 0x0400
#word PTCON
#BIT PTCONPTEN
                 = PTCON.15
#BIT PTCONPTSIDL = PTCON.13
#BIT PTCONSYNCOEN = PTCON.8
#BIT PTCONSEVTPS3 = PTCON.3
#BIT PTCONSEVTPS2 = PTCON.2
```

```
#BIT PTCONSEVTPS1 = PTCON.1
#BIT PTCONSEVTPS0 = PTCON.0
#word PTCON2
               = 0x0402
#word PTPER
              = 0x0404
#word SEVTCMPL = 0x0406
#word SEVTCMPH = 0x0407
#word SEVTCMP
               = 0x0406
#word MDC
              = 0x040A
#word STCON
              = 0x040E
#BIT STCONSEIEN = STCON.11
#BIT STCONSYNCOEN = STCON.8
#BIT STCONSYNCEN = STCON.7
#BIT STCONSEVTPS3 = STCON.3
#BIT STCONSEVTPS2 = STCON.2
#BIT STCONSEVTPS1 = STCON.1
#BIT STCONSEVTPS0 = STCON.0
#word STCON2
              = 0x0410
#word STPER
              = 0x0412
#word SSEVTCMP = 0x0414
#word CHOP = 0x041A
// PWM1
//
#word PWMCON1
                = 0x0420
#BIT PWMCON1FLTSTAT = PWMCON1.15
#BIT PWMCON1CLSTAT = PWMCON1.14
#BIT PWMCON1TRGSTAT = PWMCON1.13
#BIT PWMCON1FLTIEN = PWMCON1.12
#BIT PWMCON1CLIEN = PWMCON1.11
#BIT PWMCON1TRGIEN = PWMCON1.10
#BIT PWMCON1ITB = PWMCON1.9
#BIT PWMCON1MDCS = PWMCON1.8
#BIT PWMCON1DTC1 = PWMCON1.7
#BIT PWMCON1DTC0 = PWMCON1.6
#BIT PWMCON1DTCP = PWMCON1.5
#BIT PWMCON1MTBS = PWMCON1.3
#BIT PWMCON1CAM = PWMCON1.2
#BIT PWMCON1XPRES = PWMCON1.1
#BIT PWMCON1IUE = PWMCON1.0
#word IOCON1
             = 0x0422
#bit IOCON1PENH = IOCON1.15
#bit IOCON1PENL = IOCON1.14
#bit IOCON1POLH = IOCON1.13
#bit IOCON1POLL = IOCON1.12
#bit IOCON1PMOD1 = IOCON1.11
#bit IOCON1PMOD0 = IOCON1.10
```

```
#bit IOCON1OVRENH = IOCON1.9
#bit IOCON1OVRENL = IOCON1.8
#bit IOCON1OVRDAT1 = IOCON1.7
#bit IOCON1OVRDAT0 = IOCON1.6
#bit IOCON1FLTDAT1 = IOCON1.5
#bit IOCON1FLTDAT0 = IOCON1.4
#bit IOCON1CLDAT1 = IOCON1.3
#bit IOCON1CLDAT0 = IOCON1.1
#bit IOCON1OSYNC = IOCON1.0
#word FCLCON1
                 = 0x0424
#bit FCLCON1IFLTMOD = FCLCON1.15
#bit FCLCON1CLSRC4 = FCLCON1.14
#bit FCLCON1CLSRC3 = FCLCON1.13
#bit FCLCON1CLSRC2 = FCLCON1.12
#bit FCLCON1CLSRC1 = FCLCON1.11
#bit FCLCON1CLSRC0 = FCLCON1.10
#bit FCLCON1CLPOL = FCLCON1.9
#bit FCLCON1CLMOD = FCLCON1.8
#bit FCLCON1FLTSRC4 = FCLCON1.7
#bit FCLCON1FLTSRC3 = FCLCON1.6
#bit FCLCON1FLTSRC2 = FCLCON1.5
#bit FCLCON1FLTSRC1 = FCLCON1.4
#bit FCLCON1FLTSRC0 = FCLCON1.3
#bit FCLCON1FLTPOL = FCLCON1.2
#bit FCLCON1FLTMOD1 = FCLCON1.1
#bit FCLCON1FLTMOD0 = FCLCON1.0
#word PDC1
             = 0x0426
             = 0x0428
#word PHASE1
#word DTR1
             = 0x042A
#word ALTDTR1 = 0x042C
#word SDC1
            = 0x042E
#word SPHASE1 = 0x0430
#word TRIG1
             = 0x0432
#word TRGCON1
               = 0x0434
#bit TRGCON1TRGDIV3 = TRGCON1.15
#bit TRGCON1TRGDIV2 = TRGCON1.14
#bit TRGCON1TRGDIV1 = TRGCON1.13
#bit TRGCON1TRGDIV0 = TRGCON1.12
#bit TRGCON1TRGSTRT5 = TRGCON1.5
#bit TRGCON1TRGSTRT4 = TRGCON1.4
#bit TRGCON1TRGSTRT3 = TRGCON1.3
#bit TRGCON1TRGSTRT2 = TRGCON1.2
#bit TRGCON1TRGSTRT1 = TRGCON1.1
#bit TRGCON1TRGSTRT0 = TRGCON1.0
#word STRIG1
              = 0x0436
#word PWMCAP1
                = 0x0438
#word LEBCON1
                = 0x043A
```

#word LEBDLY1

= 0x043C

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```
#word AUXCON1 = 0x043E
// PWM2
//
#word PWMCON2
                 = 0x0440
#BIT PWMCON2FLTSTAT = PWMCON2.15
#BIT PWMCON2CLSTAT = PWMCON2.14
#BIT PWMCON2TRGSTAT = PWMCON2.13
#BIT PWMCON2FLTIEN = PWMCON2.12
#BIT PWMCON2CLIEN = PWMCON2.11
#BIT PWMCON2TRGIEN = PWMCON2.10
#BIT PWMCON2ITB = PWMCON2.9
#BIT PWMCON2MDCS = PWMCON2.8
#BIT PWMCON2DTC1 = PWMCON2.7
#BIT PWMCON2DTC0 = PWMCON2.6
#BIT PWMCON2DTCP = PWMCON2.5
#BIT PWMCON2MTBS = PWMCON2.3
#BIT PWMCON2CAM = PWMCON2.2
#BIT PWMCON2XPRES = PWMCON2.1
#BIT PWMCON2IUE = PWMCON2.0
#word IOCON2
              = 0x0442
#bit IOCON2PENH = IOCON2.15
#bit IOCON2PENL = IOCON2.14
#bit IOCON2POLH = IOCON2.13
#bit IOCON2POLL = IOCON2.12
#bit IOCON2PMOD1 = IOCON2.11
#bit IOCON2PMOD0 = IOCON2.10
#bit IOCON2OVRENH = IOCON2.9
#bit IOCON2OVRENL = IOCON2.8
#bit IOCON2OVRDAT1 = IOCON2.7
#bit IOCON2OVRDAT0 = IOCON2.6
#bit IOCON2FLTDAT1 = IOCON2.5
#bit IOCON2FLTDAT0 = IOCON2.4
#bit IOCON2CLDAT1 = IOCON2.3
#bit IOCON2CLDAT0 = IOCON2.2
#bit IOCON2SWAP = IOCON2.1
#bit IOCON2OSYNC = IOCON2.0
#word FCLCON2
               = 0x0444
#bit FCLCON2IFLTMOD = FCLCON2.15
#bit FCLCON2CLSRC4 = FCLCON2.14
#bit FCLCON2CLSRC3 = FCLCON2.13
#bit FCLCON2CLSRC2 = FCLCON2.12
#bit FCLCON2CLSRC1 = FCLCON2.11
#bit FCLCON2CLSRC0 = FCLCON2.10
#bit FCLCON2CLPOL = FCLCON2.9
#bit FCLCON2CLMOD = FCLCON2.8
#bit FCLCON2FLTSRC4 = FCLCON2.7
```

#bit FCLCON2FLTSRC3 = FCLCON2.6

```
#bit FCLCON2FLTSRC2 = FCLCON2.5
#bit FCLCON2FLTSRC1 = FCLCON2.4
#bit FCLCON2FLTSRC0 = FCLCON2.3
#bit FCLCON2FLTPOL = FCLCON2.2
#bit FCLCON2FLTMOD1 = FCLCON2.1
#bit FCLCON2FLTMOD0 = FCLCON2.0
#word PDC2
             = 0x0446
#word PHASE2
              = 0x0448
#word DTR2
             = 0x044A
#word ALTDTR2
              = 0x044C
             = 0x044E
#word SDC2
#word SPHASE2
               = 0x0450
            = 0x0452
#word TRIG2
#word TRGCON2
               = 0x0454
#bit TRGCON2TRGDIV3 = TRGCON2.15
#bit TRGCON2TRGDIV2 = TRGCON2.14
#bit TRGCON2TRGDIV1 = TRGCON2.13
#bit TRGCON2TRGDIV0 = TRGCON2.12
#bit TRGCON2TRGSTRT5 = TRGCON2.5
#bit TRGCON2TRGSTRT4 = TRGCON2.4
#bit TRGCON2TRGSTRT3 = TRGCON2.3
#bit TRGCON2TRGSTRT2 = TRGCON2.2
#bit TRGCON2TRGSTRT1 = TRGCON2.1
#bit TRGCON2TRGSTRT0 = TRGCON2.0
#word STRIG2
              = 0x0456
#word PWMCAP2
              = 0x0458
#word LEBCON2
               = 0x045A
#word LEBDLY2
               = 0x045C
#word AUXCON2
              = 0x045E
// PWM3
#word PWMCON3
                 = 0x0460
#BIT PWMCON3FLTSTAT = PWMCON3.15
#BIT PWMCON3CLSTAT = PWMCON3.14
#BIT PWMCON3TRGSTAT = PWMCON3.13
#BIT PWMCON3FLTIEN = PWMCON3.12
#BIT PWMCON3CLIEN = PWMCON3.11
#BIT PWMCON3TRGIEN = PWMCON3.10
#BIT PWMCON3ITB = PWMCON3.9
#BIT PWMCON3MDCS = PWMCON3.8
#BIT PWMCON3DTC1 = PWMCON3.7
#BIT PWMCON3DTC0 = PWMCON3.6
#BIT PWMCON3DTCP = PWMCON3.5
#BIT PWMCON3MTBS = PWMCON3.3
#BIT PWMCON3CAM = PWMCON3.2
#BIT PWMCON3XPRES = PWMCON3.1
#BIT PWMCON3IUE = PWMCON3.0
```

```
#word IOCON3
               = 0x0462
#bit IOCON3PENH = IOCON3.15
#bit IOCON3PENL
                = IOCON3.14
#bit IOCON3POLH = IOCON3.13
#bit IOCON3POLL = IOCON3.12
#bit IOCON3PMOD1 = IOCON3.11
#bit IOCON3PMOD0 = IOCON3.10
#bit IOCON3OVRENH = IOCON3.9
#bit IOCON3OVRENL = IOCON3.8
#bit IOCON3OVRDAT1 = IOCON3.7
#bit IOCON3OVRDAT0 = IOCON3.6
#bit IOCON3FLTDAT1 = IOCON3.5
#bit IOCON3FLTDAT0 = IOCON3.4
#bit IOCON3CLDAT1 = IOCON3.3
#bit IOCON3CLDAT0 = IOCON3.2
#bit IOCON3SWAP = IOCON3.1
#bit IOCON3OSYNC = IOCON3.0
#word FCLCON3
                 = 0x0464
#bit FCLCON3IFLTMOD = FCLCON3.15
#bit FCLCON3CLSRC4 = FCLCON3.14
#bit FCLCON3CLSRC3 = FCLCON3.13
#bit FCLCON3CLSRC2 = FCLCON3.12
#bit FCLCON3CLSRC1 = FCLCON3.11
#bit FCLCON3CLSRC0 = FCLCON3.10
#bit FCLCON3CLPOL = FCLCON3.9
#bit FCLCON3CLMOD = FCLCON3.8
#bit FCLCON3FLTSRC4 = FCLCON3.7
#bit FCLCON3FLTSRC3 = FCLCON3.6
#bit FCLCON3FLTSRC2 = FCLCON3.5
#bit FCLCON3FLTSRC1 = FCLCON3.4
#bit FCLCON3FLTSRC0 = FCLCON3.3
#bit FCLCON3FLTPOL = FCLCON3.2
#bit FCLCON3FLTMOD1 = FCLCON3.1
#bit FCLCON3FLTMOD0 = FCLCON3.0
#word PDC3
             = 0x0466
#word PHASE3
              = 0x0468
#word DTR3
             = 0x046A
              = 0x046C
#word ALTDTR3
#word SDC3
             = 0x046E
#word SPHASE3 = 0x0470
#word TRIG3
              = 0x0472
#word TRGCON3
              = 0x0474
#bit TRGCON3TRGDIV3 = TRGCON3.15
#bit TRGCON3TRGDIV2 = TRGCON3.14
#bit TRGCON3TRGDIV1 = TRGCON3.13
#bit TRGCON3TRGDIV0 = TRGCON3.12
#bit TRGCON3TRGSTRT5 = TRGCON3.5
#bit TRGCON3TRGSTRT4 = TRGCON3.4
```

#bit TRGCON3TRGSTRT3 = TRGCON3.3

```
#bit TRGCON3TRGSTRT2 = TRGCON3.2
#bit TRGCON3TRGSTRT1 = TRGCON3.1
#bit TRGCON3TRGSTRT0 = TRGCON3.0
#word STRIG3
            = 0x0476
#word PWMCAP3
              = 0x0478
#word LEBCON3 = 0x047A
#word LEBDLY3 = 0x047C
#word AUXCON3 = 0x047E
//ADC SFR's
#WORD ADCON
                 = 0x0300
#BIT ADCONADON = ADCON.15
#BIT
    ADCONADSIDL = ADCON.13
    ADCONSLOWCLK = ADCON.12
#BIT
#BIT
    ADCONGSWTRG
                      = ADCON.10
#BIT
    ADCONFORM
                             = ADCON.8
                      = ADCON.7
#BIT
    ADCONEIE
#BIT
    ADCONORDER
                      = ADCON.6
     ADCONSEQSAMP = ADCON.5
#BIT
     ADCONASYNCSAMP = ADCON.4
#BIT
\#BIT ADCONADCS2 = ADCON.2
#BIT ADCONADCS1
                      = ADCON.1
#BIT ADCONADCS0
                      = ADCON.0
#WORD IFS5
               = 0x008E
#BIT IFS5PWM2IF = IFS5.15
     IFS5PWM1IF = IFS5.14
#BIT
#BIT IFS5ADCP12IF = IFS5.13
#BIT IFS5ADCP11IF = IFS5.4
#BIT IFS5ADCP10IF = IFS5.3
#BIT IFS5ADCP9IF = IFS5.2
#BIT IFS5ADCP8IF = IFS5.1
#WORD IFS6
             = 0x0090
#BIT IFS6ADCP1IF = IFS6.15
#BIT
    IFS6ADCP0IF = IFS6.14
\#BIT IFS6AC4IF = IFS6.9
#BIT IFS6AC3IF = IFS6.8
\#BIT IFS6AC2IF = IFS6.7
#BIT IFS6PWM9IF = IFS6.6
#BIT IFS6PWM8IF = IFS6.5
#BIT
    IFS6PWM7IF = IFS6.4
```

#WORD IFS7 = 0x0092 #BIT IFS7ADCP7IF = IFS7.5

#BIT IFS6PWM5IF = IFS6.2 #BIT IFS6PWM4IF = IFS6.1 #BIT IFS6PWM3IF = IFS6.0

IFS6PWM6IF = IFS6.3

#BIT

- #BIT IFS7ADCP6IF = IFS7.4
- #BIT IFS7ADCP5IF = IFS7.3
- #BIT IFS7ADCP4IF = IFS7.2
- #BIT IFS7ADCP3IF = IFS7.1
- #BIT IFS7ADCP2IF = IFS7.0
- #WORD IPC27 = 0x00DA
- #BIT IPC27ADCP1IP2 = IPC27.14
- #BIT IPC27ADCP1IP1 = IPC27.13
- #BIT IPC27ADCP1IP0 = IPC27.12
- #BIT IPC27ADCP0IP2 = IPC27.10
- #BIT IPC27ADCP0IP1 = IPC27.9
- #BIT IPC27ADCP0IP0 = IPC27.8
- #WORD IPC28 = 0x00DC
- #BIT IPC28ADCP5IP2 = IPC28.14
- #BIT IPC28ADCP5IP1 = IPC28.13
- #BIT IPC28ADCP5IP0 = IPC28.12
- #BIT IPC28ADCP4IP2 = IPC28.10
- #BIT IPC28ADCP4IP1 = IPC28.9
- #BIT IPC28ADCP4IP0 = IPC28.8
- #BIT IPC28ADCP3IP2 = IPC28.6
- #BIT IPC28ADCP3IP1 = IPC28.5
- #BIT IPC28ADCP3IP0 = IPC28.4
- #BIT IPC28ADCP2IP2 = IPC28.2
- #BIT IPC28ADCP2IP1 = IPC28.1
- #BIT IPC28ADCP2IP0 = IPC28.0
- #WORD IPC29 = 0x00DE
- #BIT IPC29ADCP7IP2 = IPC29.6
- #BIT IPC29ADCP7IP1 = IPC29.5
- #BIT IPC29ADCP7IP0 = IPC29.4
- #BIT IPC29ADCP6IP2 = IPC29.2
- #BIT IPC29ADCP6IP1 = IPC29.1
- #BIT IPC29ADCP6IP0 = IPC29.0
- #WORD IEC6 = 0x00A0
- #BIT IEC6ADCP0IE = IEC6.15
- #BIT IEC6ADCP1IE = IEC6.14
- #WORD IEC7 = 0x00A2
- #BIT IEC7ADCP4IE = IEC7.2
- #WORD ADPCFG = 0x0302
- #BIT ADPCFGPCFG0 = ADPCFG.0
- #BIT ADPCFGPCFG1 = ADPCFG.1
- #BIT ADPCFGPCFG2 = ADPCFG.2
- #BIT ADPCFGPCFG3 = ADPCFG.3
- #BIT ADPCFGPCFG4 = ADPCFG.4
- #BIT ADPCFGPCFG5 = ADPCFG.5

```
#BIT ADPCFGPCFG8 = ADPCFG.8
```

- #BIT ADPCFGPCFG9 = ADPCFG.9
- #BIT ADPCFGPCFG12 = ADPCFG.12
- #BIT ADPCFGPCFG13 = ADPCFG.13
- #BIT ADPCFGPCFG14 = ADPCFG.14
- #BIT ADPCFGPCFG15 = ADPCFG.15

#### #WORD ADPCFG2 = 0x0304

### #WORD ADSTAT = 0x0306

- #BIT ADSTATPORDY = ADSTAT.0
- #BIT ADSTATP1RDY = ADSTAT.1
- #BIT ADSTATP2RDY = ADSTAT.2
- #BIT ADSTATP4RDY = ADSTAT.4
- #BIT ADSTATP6RDY = ADSTAT.6
- #BIT ADSTATP7RDY = ADSTAT.7

### #WORD ADCPC0 = 0x030A

- #BIT ADCPC0IROEN0 = ADCPC0.7
- #BIT ADCPC0SWTRG0 = ADCPC0.5
- #BIT ADCPC0TRGSRC04 = ADCPC0.4
- #BIT ADCPC0TRGSRC03 = ADCPC0.3
- #BIT ADCPC0TRGSRC02 = ADCPC0.2
- #BIT ADCPC0TRGSRC01 = ADCPC0.1
- #BIT ADCPC0TRGSRC00 = ADCPC0.0
- #BIT ADCPC0IRQEN1 = ADCPC0.15
- #BIT ADCPC0PEND1 = ADCPC0.14 #BIT ADCPC0SWTRG1 = ADCPC0.13
- #BIT ADCPC0TRGSRC14 = ADCPC0.12
- #BIT ADCPC0TRGSRC14 = ADCPC0.11
- #BIT ADCPC0TRGSRC12 = ADCPC0.10
- #BIT ADCPC0TRGSRC11 = ADCPC0.9
- #BIT ADCPC0TRGSRC10 = ADCPC0.8

# #WORD ADCPC1 = 0x030C

- #BIT ADCPC1IRQEN2 = ADCPC1.7
- #BIT ADCPC1PEND2 = ADCPC1.6
- #BIT ADCPC1SWTRG2 = ADCPC1.5
- #BIT ADCPC1TRGSRC24 = ADCPC1.4
- #BIT ADCPC1TRGSRC23 = ADCPC1.3
- #BIT ADCPC1TRGSRC22 = ADCPC1.2
- #BIT ADCPC1TRGSRC21 = ADCPC1.1 #BIT ADCPC1TRGSRC20 = ADCPC1.0

## #WORD ADCPC2 = 0x030E

- #BIT ADCPC2IRQEN4 = ADCPC2.8
- #BIT ADCPC2PEND4 = ADCPC2.6
- #BIT ADCPC2SWTRG4 = ADCPC2.5
- #BIT ADCPC2TRGSRC44 = ADCPC2.4
- #BIT ADCPC2TRGSRC43 = ADCPC2.3
- #BIT ADCPC2TRGSRC42 = ADCPC2.2

```
#BIT ADCPC2TRGSRC41 = ADCPC2.1
#BIT ADCPC2TRGSRC40 = ADCPC2.0
#WORD ADCPC3
                 = 0x0310
#BIT ADCPC3IRQEN7 = ADCPC3.15
#BIT
     ADCPC3PEND7 = ADCPC3.14
#BIT
     ADCPC3SWTRG7 = ADCPC3.13
#BIT
    ADCPC3TRGSRC74 = ADCPC3.12
#BIT
    ADCPC3TRGSRC73 = ADCPC3.11
#BIT
    ADCPC3TRGSRC72 = ADCPC3.10
#BIT
    ADCPC3TRGSRC71 = ADCPC3.9
#BIT
    ADCPC3TRGSRC70 = ADCPC3.8
#BIT
     ADCPC3IROEN6 = ADCPC3.7
#BIT
     ADCPC3PEND6 = ADCPC3.6
#BIT
     ADCPC3SWTRG6 = ADCPC3.5
    ADCPC3TRGSRC64 = ADCPC3.4
#BIT
#BIT
    ADCPC3TRGSRC63 = ADCPC3.3
#BIT
    ADCPC3TRGSRC62 = ADCPC3.2
#BIT
    ADCPC3TRGSRC61 = ADCPC3.1
#BIT ADCPC3TRGSRC60 = ADCPC3.0
#WORD ADCBUF0 = 0x0340
#WORD ADCBUF1 = 0x0342
#WORD ADCBUF2 = 0x0344
#WORD ADCBUF3 = 0x0346
#WORD ADCBUF4 = 0x0348
#WORD ADCBUF5 = 0x034A
#WORD ADCBUF6 = 0x034C
#WORD ADCBUF7 = 0x034E
#WORD ADCBUF8 = 0x0350
#WORD ADCBUF9 = 0x0352
#WORD ADCBUF10 = 0x0354
#WORD ADCBUF11 = 0x0356
#WORD ADCBUF12 = 0x0358
#WORD ADCBUF13 = 0x035A
#WORD ADCBUF14 = 0x035C
#WORD ADCBUF15 = 0x035E
#WORD ADCBUF24 = 0x0370
#WORD ADCBUF25 = 0x0372
#WORD IEC6 = 0x00A0
#BIT ADCP1IE = IEC6.15
#BIT ADCP0IE = IEC6.14
#WORD IEC7 = 0x00A2
#BIT ADCP7IE = IEC7.5
#BIT
    ADCP6IE = IEC7.4
#BIT
    ADCP5IE = IEC7.3
#BIT
    ADCP4IE = IEC7.2
#BIT ADCP3IE = IEC7.1
```

#BIT ADCP2IE = IEC7.0

### //Comparator SFR's

```
#byte CMPCON1
                = 0x0540
#bit CMPCON1CMPON = CMPCON1.15
#bit CMPCON1CMPSIDL = CMPCON1.13
#bit CMPCON1DACOE = CMPCON1.8
#bit CMPCON1INSEL1 = CMPCON1.7
#bit CMPCON1INSEL0 = CMPCON1.6
#bit CMPCON1EXTREF = CMPCON1.5
#bit CMPCON1CMPSTAT = CMPCON1.3
#bit CMPCON1CMPPOL = CMPCON1.1
#bit CMPCON1RANGE = CMPCON1.0
#byte CMPDAC1
                = 0x0542
#byte CMPCON2
                =0x0544
#bit CMPCON2CMPON = CMPCON2.15
#bit CMPCON2CMPSIDL = CMPCON2.13
#bit CMPCON2DACOE = CMPCON2.8
#bit CMPCON2INSEL1 = CMPCON2.7
#bit CMPCON2INSEL0 = CMPCON2.6
#bit CMPCON2EXTREF = CMPCON2.5
#bit CMPCON2CMPSTAT = CMPCON2.3
#bit CMPCON2CMPPOL = CMPCON2.1
#bit CMPCON2RANGE = CMPCON2.0
#byte CMPDAC2
                = 0x0546
#byte CMPCON3
                =0x0548
#bit CMPCON3CMPON = CMPCON3.15
#bit CMPCON3CMPSIDL = CMPCON3.13
#bit CMPCON3DACOE = CMPCON3.8
#bit CMPCON3INSEL1 = CMPCON3.7
#bit CMPCON3INSEL0 = CMPCON3.6
#bit CMPCON3EXTREF = CMPCON3.5
#bit CMPCON3CMPSTAT = CMPCON3.3
#bit CMPCON3CMPPOL = CMPCON3.1
#bit CMPCON3RANGE = CMPCON3.0
#byte CMPDAC3
                = 0x054A
#byte CMPCON4
                = 0x054c
#bit CMPCON4CMPON = CMPCON4.15
#bit CMPCON4CMPSIDL = CMPCON4.13
#bit CMPCON4DACOE = CMPCON4.8
#bit CMPCON4INSEL1 = CMPCON4.7
#bit CMPCON4INSEL0 = CMPCON4.6
#bit CMPCON4EXTREF = CMPCON4.5
#bit CMPCON4CMPSTAT = CMPCON4.3
```

#bit CMPCON4CMPPOL = CMPCON4.1

```
#bit CMPCON4RANGE = CMPCON4.0
#byte CMPDAC4
                  = 0x054E
#define cADCP1DONE
                    (0x01)
#define cADCP2DONE
                    (0x02)
                    (0x04)
#define cADCP6DONE
#define cADCP7DONE
                    (0x08)
#define cADCP4DONE
                    (0x10)
#define cCURRENT_LIMIT_TIME
                               (1000)
#define cINCOMER_TIMER_VAL
                               (1000)
#define PWM_PERIOD 1580
#define PWM MIN
                   (3.0)
#define PWM_MAX
                   (97.0)
#define PWM_MPPT_STEP (1.0)
#ifdef NEW_AD_RES_VALS
#define cP_O_MIN_ADJ (-30.0)
#define cP_O_MAX_ADJ (30.0)
#else
#define cP_O_MIN_ADJ (-10.0)
#define cP_O_MAX_ADJ (10.0)
#endif
#define cVIN MIN SW ON
                          (8.0)
#define cVIN_MIN_SW_ON_HYST
                            (cVIN_MIN_SW_ON / 10.0)
#define cFILTER_CNT
                    (55)
#define HIST_COUNT
typedef unsigned int16 WORD;
typedef struct
  WORD wRawLow;
  WORD wRawHigh;
 float fEngLow;
 float fEngHigh;
  float fConverted;
 float fFiltered;
  unsigned int16 sRawVal;
} sANAENG,*psANAENG;
```

```
typedef struct
              // constants for PID
  float fKp;
  float fKd;
  float fKi;
  //
  float pre_error;
  float integral;
  float error;
  float derivative;
  float output;
  float setpoint;
} sPIDSTRUCT, *psPIDSTRUCT;
vSetupBoard
void
                       (void);
void
      vInitClock
                     (void);
void
      vSwitchPower
                       (int8 bState);
void
      vSetupStruct
                      (void);
void
      vSetupPins
                      (void);
void
      vSetupPWM
                        (void);
      vStartPWM
void
                       (void);
void
      vStopPWM
                       (void);
      vSetupADC
void
                       (void);
      vInitADC
                      (void);
void
void
      vSetupTimers
                       (void);
      vSetupInterrupts
void
                       (void);
      vDoPwmVOutControl (int8 iIdx);
void
      vDoMPPTControl
void
                          (void);
                        (BYTE *bPairsDone);
void
      vDoEngConv
void
      vCalcEng
                     (int8 iIdx);
void
      vKickWdt
                      (void);
      vSetDuty
void
                     (BYTE bldx,float fVal);
void
      vDoFiltering
                      (psANAENG psEngTbl);
      vSetPwmOn
                       (unsigned int8 bIdx);
void
void
      vSetPwmOff
                       (unsigned int8 bIdx);
float PIDcal
                 (psPIDSTRUCT sPidMem,float actual_position);
#ifdef __cplusplus
#endif
#endif
```





### NRF NEXUS SEARCH RESULTS

# TO WHOM IT MAY CONCERN

This letter serves to inform that a literature search has been performed on behalf of Mr Neil Jansen Van Rensburg student number 207060860 on the topic:

Technology development of a maximum power point tracker for regenerative fuel cells

Currently there are no records retrieved on the above research topic on NRF NEXUS DATABASE.

The search was conducted by Mr Mluleki Siguntu: Gold-Fields Academic Library on the 29<sup>th</sup> August 2012.

I thank you

Signed...

Vaal University of Technology Your world to a better future

Mluleki Siguntu

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**Gold Fields Academic Information Services: Client Services** 

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